

# CS8126

## 5.0 V, 750 mA Low Dropout Linear Regulator with Delayed RESET

The CS8126 is a low dropout, high current 5.0 V linear regulator. It is an improved replacement for the CS8156. Improvements include higher accuracy, tighter saturation control, better supply rejection, and enhanced  $\overline{\text{RESET}}$  circuitry. Familiar PNP regulator features such as reverse battery protection, overvoltage shutdown, thermal shutdown, and current limit make the CS8126 suitable for use in automotive and battery operated equipment. Additional on-chip filtering has been included to enhance rejection of high frequency transients on all external leads.

An active microprocessor  $\overline{\text{RESET}}$  function is included on-chip with externally programmable delay time. During power-up, or after detection of any error in the regulated output, the  $\overline{\text{RESET}}$  lead will remain in the low state for the duration of the delay. Types of errors include short circuit, low input voltage, overvoltage shutdown, thermal shutdown, or others that cause the output to become unregulated. This function is independent of the input voltage and will function correctly with an output voltage as low as 1.0 V. Hysteresis is included in both the reset and Delay comparators for enhanced noise immunity. A latching discharge circuit is used to discharge the Delay capacitor, even when triggered by a relatively short fault condition. This circuit improves upon the commonly used SCR structure by providing full capacitor discharge (0.2 V type).

Note: The CS8126 is lead compatible with the LM2927 and LM2926.

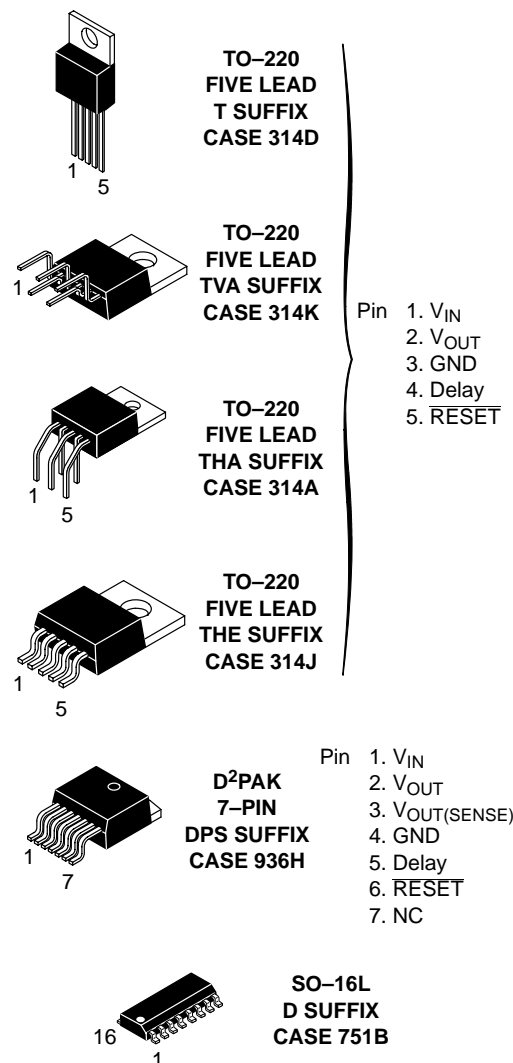
### Features

- Low Dropout Voltage (0.6 V at 0.5 A)
- 3.0% Output Accuracy
- Active  $\overline{\text{RESET}}$
- External  $\overline{\text{RESET}}$  Delay for Reset
- Protection Circuitry
  - Reverse Battery Protection
  - +60 V, -50 V Peak Transient Voltage
  - Short Circuit Protection
  - Internal Thermal Overload Protection



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### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

### DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 9 of this data sheet.

# CS8126

## PIN CONNECTIONS

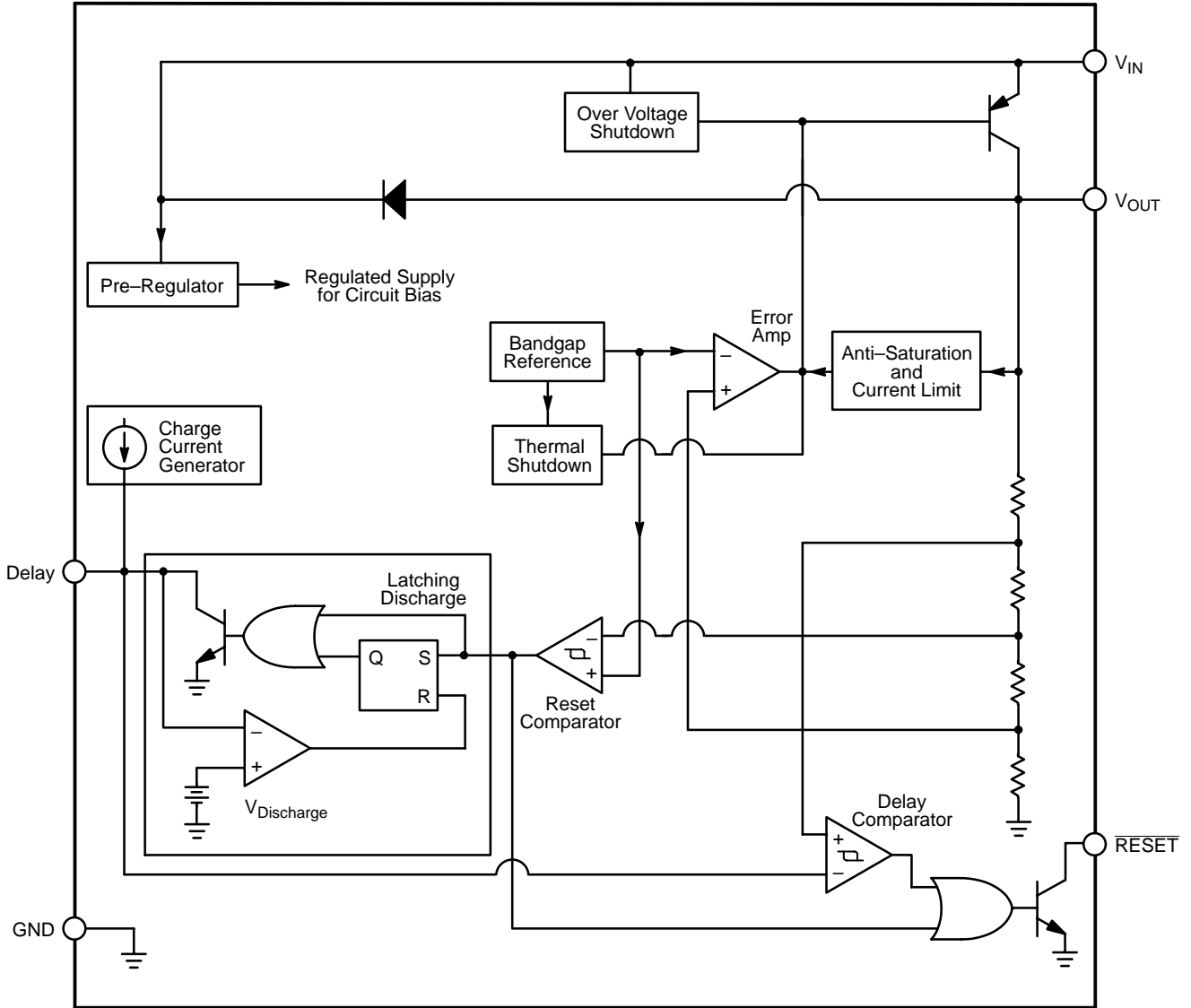
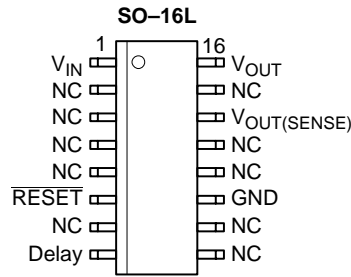


Figure 1. Block Diagram

**ABSOLUTE MAXIMUM RATINGS\***

Rating	Value	Unit
Power Dissipation	Internally Limited	–
Peak Transient Voltage (46 V Load Dump)	–50, 60	V
Output Current	Internally Limited	–
ESD Susceptibility (Human Body Model)	4.0	kV
Junction Temperature Range	–40 to +150	°C
Storage Temperature Range	–55 to +150	°C
Lead Temperature Soldering:	Wave Solder (through hole styles only) (Note 1.) Reflow (SMD styles only) (Note 2.)	260 peak 230 peak °C

1. 10 second maximum.

2. 60 second maximum above 183°C.

\*The maximum package power dissipation must be observed.

**ELECTRICAL CHARACTERISTICS** ( $T_A = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $T_J = -40^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$ ,  $V_{IN} = 6.0$  to  $26\text{ V}$ ,  $I_O = 5.0$  to  $500\text{ mA}$ ,  $R_{RESET} = 4.7\text{ k}\Omega$  to  $V_{CC}$ , unless otherwise noted.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
<b>Output Stage (<math>V_{OUT}</math>)</b>					
Output Voltage	–	4.85	5.00	5.15	V
Dropout Voltage	$I_{OUT1} = 500\text{ mA}$	–	0.35	0.60	V
Supply Current	$I_{OUT} \leq 10\text{ mA}$ $I_{OUT} \leq 100\text{ mA}$ $I_{OUT} \leq 500\text{ mA}$	– – –	2.0 6.0 55	7.0 12 100	mA mA mA
Line Regulation	$V_{IN} = 6.0$ to $26\text{ V}$ , $I_{OUT} = 50\text{ mA}$	–	5.0	50	mV
Load Regulation	$I_{OUT} = 50$ to $500\text{ mA}$ , $V_{IN} = 14\text{ V}$	–	10	50	mV
Ripple Rejection	$f = 120\text{ Hz}$ , $V_{IN} = 7.0$ to $17\text{ V}$ , $I_{OUT} = 250\text{ mA}$	54	75	–	dB
Current Limit	–	0.75	1.20	–	A
Overvoltage Shutdown	–	32	–	40	V
Maximum Line Transient	$V_{OUT} \leq 5.5\text{ V}$	–	95	–	V
Reverse Polarity Input Voltage DC	$V_{OUT} \geq -0.6\text{ V}$ , $10\ \Omega$ Load	–15	–30	–	V
Reverse Polarity Input Voltage Transient	1.0% Duty Cycle, $T < 100\text{ ms}$ , $10\ \Omega$ Load	–	–80	–	V
Thermal Shutdown	Note 3.	150	180	210	°C

3. Guaranteed By Design

# CS8126

**ELECTRICAL CHARACTERISTICS (continued)** ( $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$ ,  $V_{IN} = 6.0$  to  $26\text{ V}$ ,  $I_O = 5.0$  to  $500\text{ mA}$ ,  $R_{RESET} = 4.7\text{ k}\Omega$  to  $V_{CC}$ , unless otherwise noted.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
<b>RESET and Delay Functions</b>					
Delay Charge Current	$V_{Delay} = 2.0\text{ V}$	5.0	10	15	$\mu\text{A}$
RESET Threshold	$V_{OUT}$ Increasing, $V_{RT(ON)}$ $V_{OUT}$ Decreasing, $V_{RT(OFF)}$	4.65 4.50	4.90 4.70	$V_{OUT} - 0.01$ $V_{OUT} - 0.15$	V V
RESET Hysteresis	$V_{RH} = V_{RT(ON)} - V_{RT(OFF)}$	150	200	250	mV
Delay Threshold	Charge, $V_{DC(HI)}$ Discharge, $V_{DC(LO)}$	3.25 2.85	3.50 3.10	3.75 3.35	V V
Delay Hysteresis	–	200	400	800	mV
RESET Output Voltage Low	$1.0\text{ V} < V_{OUT} < V_{RTL}$ , $3.0\text{ k}\Omega$ to $V_{OUT}$	–	0.1	0.4	V
RESET Output Leakage Current	$V_{OUT} > V_{RT(ON)}$	–	0	10	$\mu\text{A}$
Delay Capacitor Discharge Voltage	Discharge Latched "ON", $V_{OUT} > V_{RT}$	–	0.2	0.5	V
Delay Time	$C_{Delay} = 0.1\text{ }\mu\text{F}^*$ . Note 4.	16	32	48	ms

\* Delay Time =  $\frac{C_{Delay} \times V_{Delay\text{Threshold Charge}}}{I_{Charge}} = C_{Delay} \times 3.2 \times 10^5$  (typ)

4. Assumes Ideal Capacitor

## PACKAGE LEAD DESCRIPTION

PACKAGE LEAD #			LEAD SYMBOL	FUNCTION
TO-220 5 LEAD	D <sup>2</sup> PAK 7-PIN	SO-16L		
1	1	1	$V_{IN}$	Unregulated supply voltage to IC.
2	2	16	$V_{OUT}$	Regulated 5.0 V output.
3	4	11	GND	Ground connection.
4	5	8	Delay	Timing capacitor for RESET function.
5	6	6	RESET	CMOS/TTL compatible output lead. RESET goes low after detection of any error in the regulated output or during power up.
–	3	14	$V_{OUT(SENSE)}$	Remote sensing of output voltage.
–	7	2, 3, 4, 5, 7, 9, 10, 12, 13, 15	NC	No Connection.

TYPICAL PERFORMANCE CHARACTERISTICS

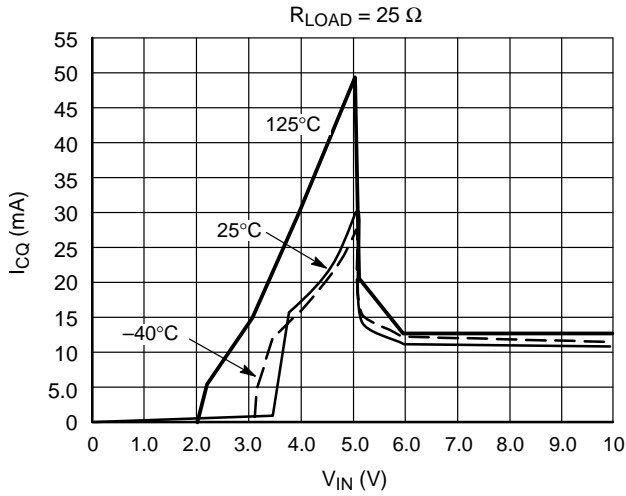


Figure 2.  $I_{CQ}$  vs.  $V_{IN}$  Over Temperature

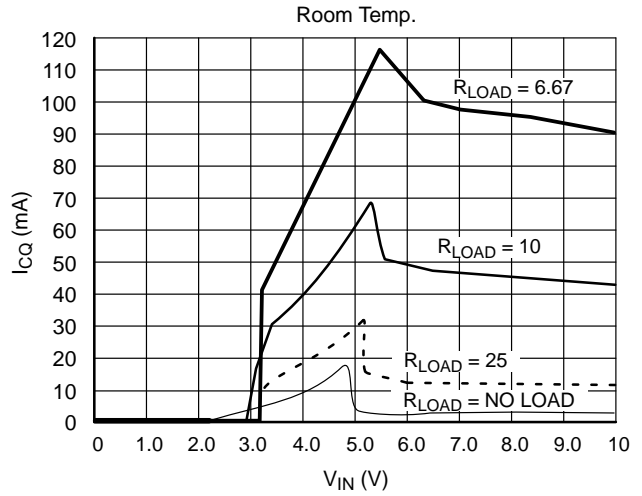


Figure 3.  $I_{CQ}$  vs.  $V_{IN}$  Over  $R_{LOAD}$

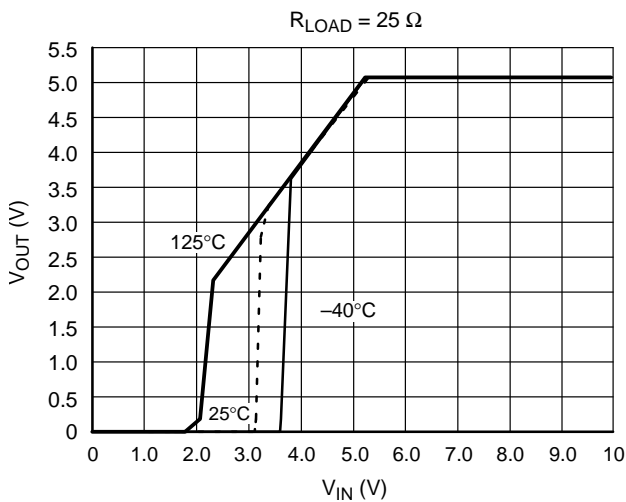


Figure 4.  $V_{OUT}$  vs.  $V_{IN}$  Over Temperature

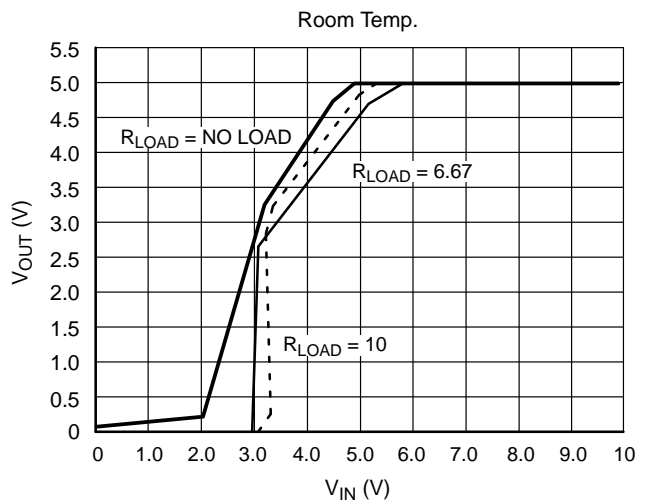


Figure 5.  $V_{OUT}$  vs.  $V_{IN}$  Over  $R_{LOAD}$

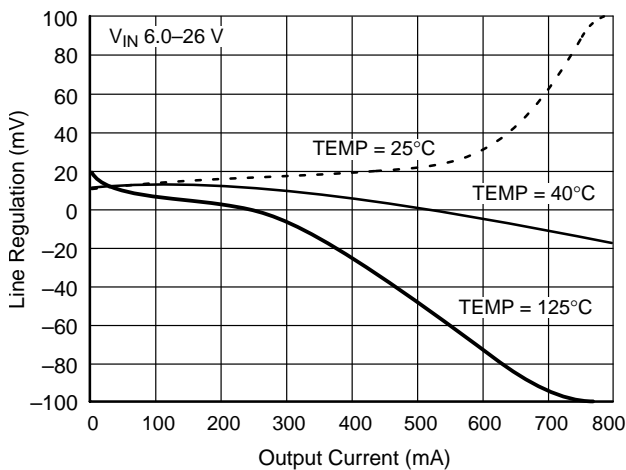


Figure 6. Line Regulation vs. Output Current Over Temperature

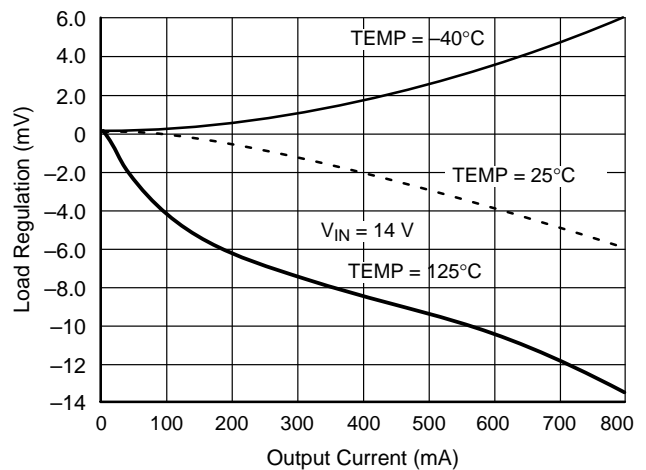


Figure 7. Load Regulation vs. Output Current Over Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

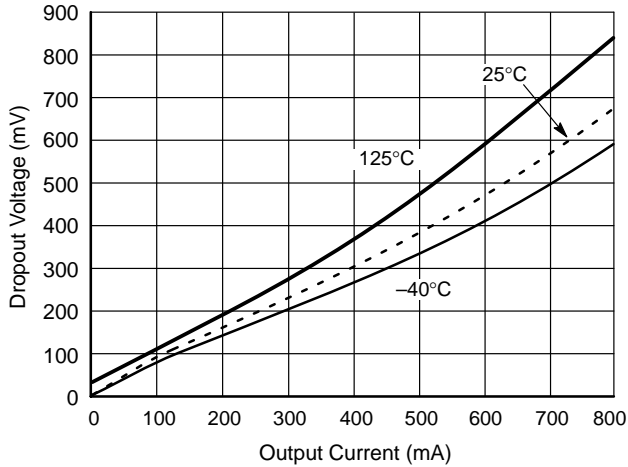


Figure 8. Dropout Voltage vs. Output Current Over Temperature

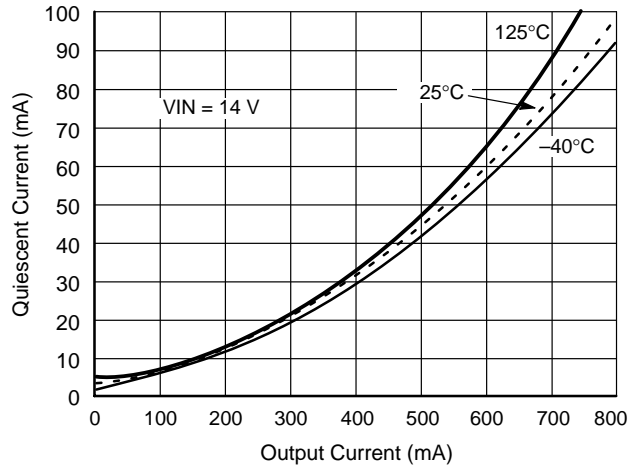


Figure 9. Quiescent Current vs. Output Current Over Temperature

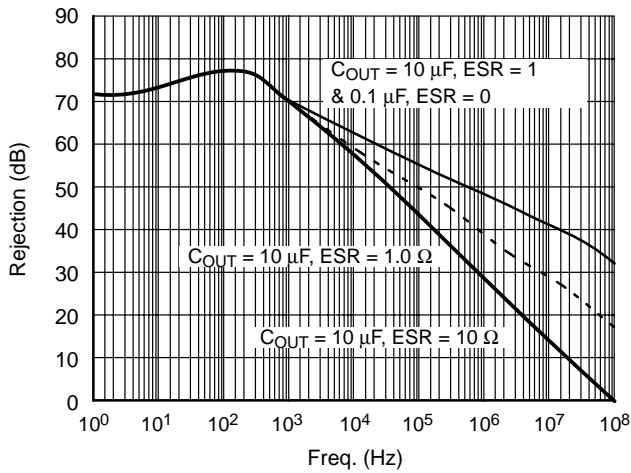


Figure 10. Ripple Rejection

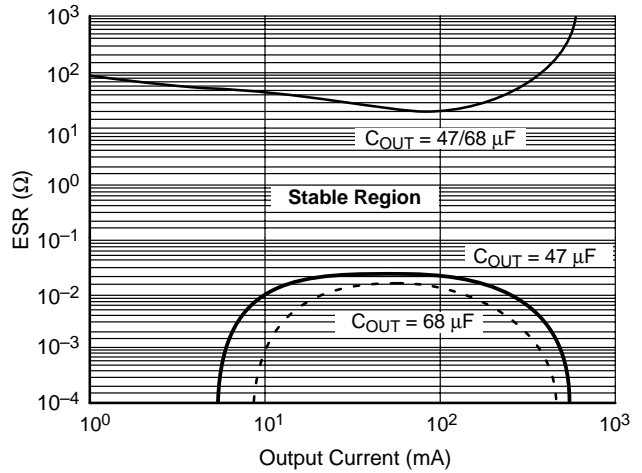


Figure 11. Output Capacitor ESR

RESET CIRCUIT WAVEFORM

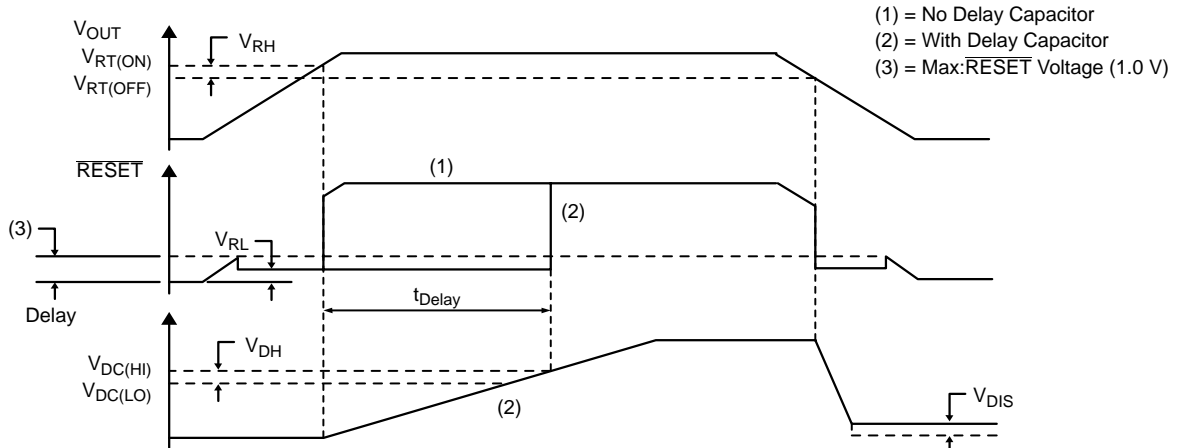


Figure 12. RESET Circuit Waveform

## CIRCUIT DESCRIPTION

The CS8126  $\overline{\text{RESET}}$  function, has hysteresis on both the Reset and Delay comparators, a latching Delay capacitor discharge circuit, and operates down to 1.0 V.

The  $\overline{\text{RESET}}$  circuit output is an open collector type with ON and OFF parameters as specified. The  $\overline{\text{RESET}}$  output NPN transistor is controlled by the two circuits described (see Block Diagram).

**Low Voltage Inhibit Circuit**

This circuit monitors output voltage, and when the output voltage falls below  $V_{\text{RT(OFF)}}$ , causes the  $\overline{\text{RESET}}$  output transistor to be in the ON (saturation) state. When the output voltage rises above  $V_{\text{RT(ON)}}$ , this circuit permits the  $\overline{\text{RESET}}$  output transistor to go into the OFF state if allowed by the  $\overline{\text{RESET}}$  Delay circuit.

 **$\overline{\text{RESET}}$  Delay Circuit**

This circuit provides a programmable (by external capacitor) delay on the  $\overline{\text{RESET}}$  output lead. The Delay lead provides source current to the external delay capacitor only when the “Low Voltage Inhibit” circuit indicates that output

voltage is above  $V_{\text{RT(ON)}}$ . Otherwise, the Delay lead sinks current to ground (used to discharge the delay capacitor). The discharge current is latched ON when the output voltage falls below  $V_{\text{RT(OFF)}}$ . The Delay capacitor is fully discharged anytime the output voltage falls out of regulation, even for a short period of time. This feature ensures a controlled  $\overline{\text{RESET}}$  pulse is generated following detection of an error condition. The circuit allows the  $\overline{\text{RESET}}$  output transistor to go to the OFF (open) state only when the voltage on the Delay lead is higher than  $V_{\text{DC(HI)}}$ .

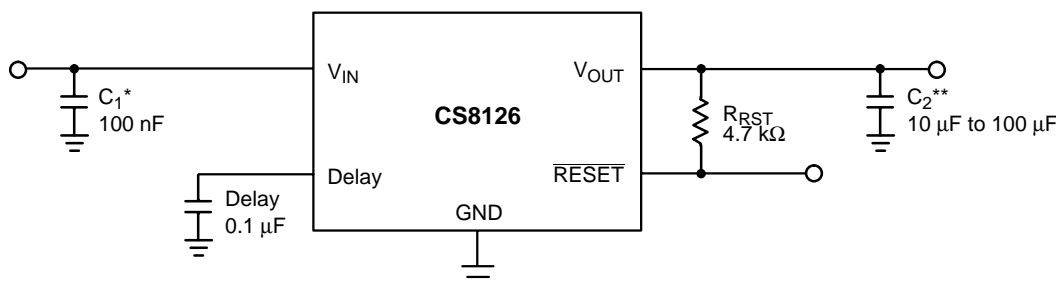
The Delay time for the  $\overline{\text{RESET}}$  function is calculated from the formula:

$$\text{Delay time} = \frac{C_{\text{Delay}} \times V_{\text{Delay Threshold}}}{I_{\text{Charge}}}$$

$$\text{Delay time} = C_{\text{Delay}} \times 3.2 \times 10^5$$

If  $C_{\text{Delay}} = 0.1 \mu\text{F}$ , Delay time (ms) = 32 ms  $\pm$  50%: i.e. 16 ms to 48 ms. The tolerance of the capacitor must be taken into account to calculate the total variation in the delay time.

## APPLICATION DIAGRAM



\*  $C_1$  is required if the regulator is far from the power source filter.

\*\*  $C_2$  is required for stability.

Figure 13. Application Diagram

## APPLICATION NOTES

**Stability Considerations**

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR, can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low

temperatures ( $-25^{\circ}\text{C}$  to  $-40^{\circ}\text{C}$ ), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor  $C_2$  shown in the test and applications circuit should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for  $C_2$  for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

**Step 1:** Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

**Step 2:** With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

**Step 3:** Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

**Step 4:** Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

**Step 5:** If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

**Step 6:** Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

**Step 7:** Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of  $\pm 20\%$  so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in step 3 above.

### Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 14) is:

$$P_{D(\max)} = (V_{IN(\max)} - V_{OUT(\min)})I_{OUT(\max)} + V_{IN(\max)}I_Q \quad (1)$$

where:

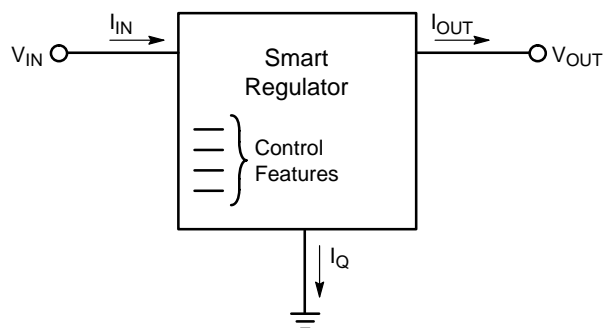
$V_{IN(\max)}$  is the maximum input voltage,  
 $V_{OUT(\min)}$  is the minimum output voltage,  
 $I_{OUT(\max)}$  is the maximum output current, for the application, and  
 $I_Q$  is the quiescent current the regulator consumes at  $I_{OUT(\max)}$ .

Once the value of  $P_{D(\max)}$  is known, the maximum permissible value of  $R_{\Theta JA}$  can be calculated:

$$R_{\Theta JA} = \frac{150^\circ\text{C} - T_A}{P_D} \quad (2)$$

The value of  $R_{\Theta JA}$  can then be compared with those in the package section of the data sheet. Those packages with  $R_{\Theta JA}$ 's less than the calculated value in equation 2 will keep the die temperature below  $150^\circ\text{C}$ .

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.



**Figure 14. Single Output Regulator With Key Performance Parameters Labeled**

### Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of  $R_{\Theta JA}$ .

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA} \quad (3)$$

where:

$R_{\Theta JC}$  = the junction-to-case thermal resistance,  
 $R_{\Theta CS}$  = the case-to-heatsink thermal resistance, and  
 $R_{\Theta SA}$  = the heatsink-to-ambient thermal resistance.

$R_{\Theta JC}$  appears in the package section of the data sheet. Like  $R_{\Theta JA}$ , it is a function of package type.  $R_{\Theta CS}$  and  $R_{\Theta SA}$  are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.



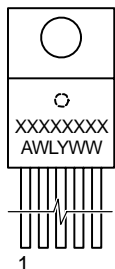
# CS8126

## ORDERING INFORMATION

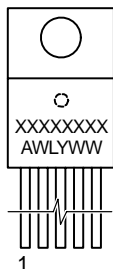
Device	Description	Shipping
CS8126-1YT5	TO-220 FIVE LEAD STRAIGHT	50 Units/Rail
CS8126-1YTVA5	TO-220 FIVE LEAD VERTICAL	50 Units/Rail
CS8126-1YTHA5	TO-220 FIVE LEAD HORIZONTAL	50 Units/Rail
CS8126-1YTHE5	TO-220 FIVE LEAD SURFACE MOUNT	50 Units/Rail
CS8126-1YTHER5	TO-220 FIVE LEAD SURFACE MOUNT	750 Tape & Reel
CS8126-1YDPS7	D <sup>2</sup> PAK, 7-PIN	50 Units/Rail
CS8126-1YDPSR7	D <sup>2</sup> PAK, 7-PIN	750 Tape & Reel
CS8126-1YDW16	SO-16L	46 Units/Rail
CS8126-1YDWR16	SO-16L	1000 Tape & Reel

## MARKING DIAGRAMS

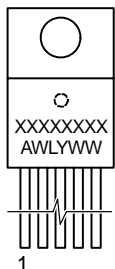
TO-220  
FIVE LEAD  
T SUFFIX  
CASE 314D



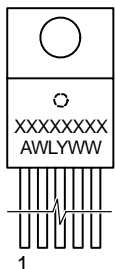
TO-220  
FIVE LEAD  
TVA SUFFIX  
CASE 314K



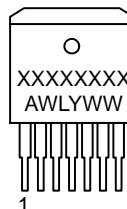
TO-220  
FIVE LEAD  
THA SUFFIX  
CASE 314A



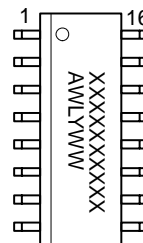
TO-220  
FIVE LEAD  
THE SUFFIX  
CASE 314J



D<sup>2</sup>PAK  
7-PIN  
DPS SUFFIX  
CASE 936H



SO-16L  
D SUFFIX  
CASE 751B

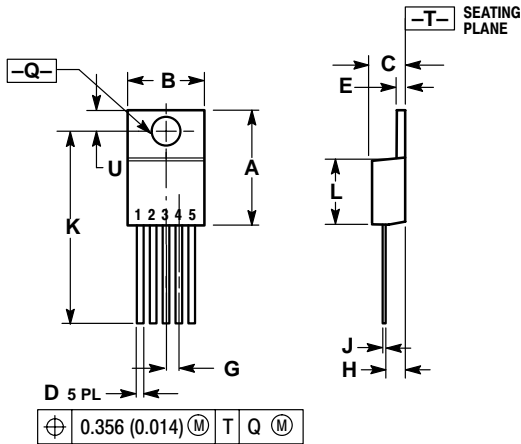


XXX... = Specific Device Code  
 A = Assembly Location  
 WL, L = Wafer Lot  
 YY, Y = Year  
 WW, W = Work Week

# CS8126

## PACKAGE DIMENSIONS

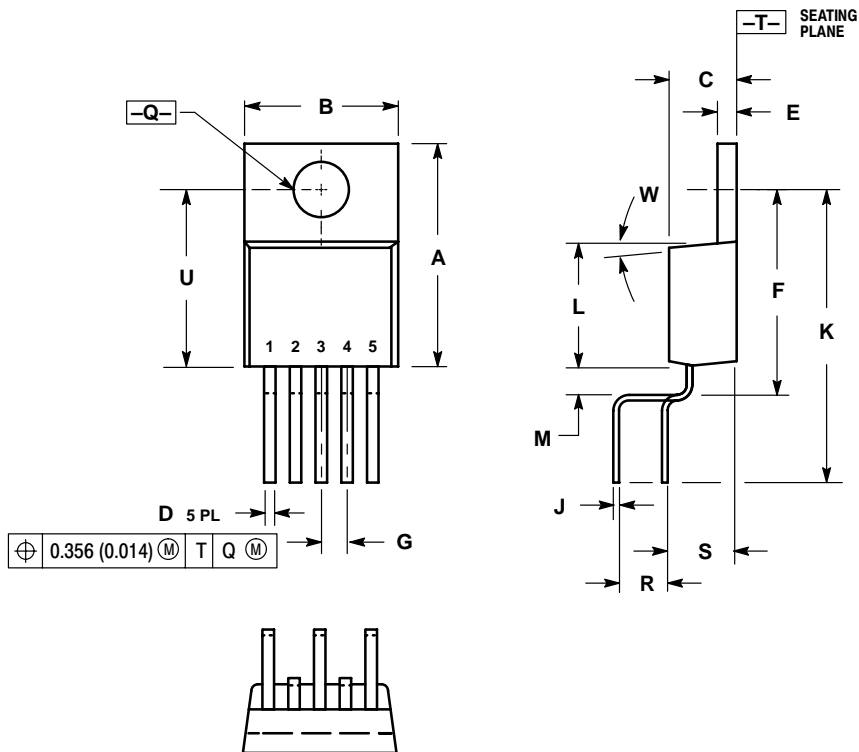
TO-220  
FIVE LEAD  
T SUFFIX  
CASE 314D-04  
ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
G	0.067 BSC		1.702 BSC	
H	0.087	0.112	2.210	2.845
J	0.015	0.025	0.381	0.635
K	0.990	1.045	25.146	26.543
L	0.320	0.365	8.128	9.271
Q	0.140	0.153	3.556	3.886
U	0.105	0.117	2.667	2.972

TO-220  
FIVE LEAD  
TVA SUFFIX  
CASE 314K-01  
ISSUE O

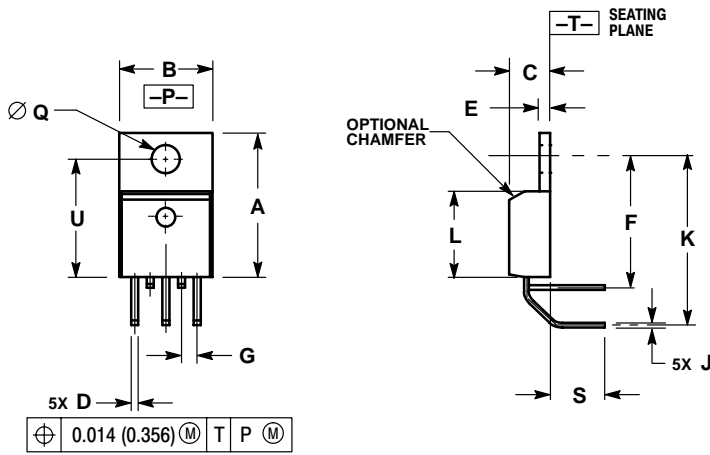


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DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.560	0.590	14.22	14.99
B	0.385	0.415	9.78	10.54
C	0.160	0.190	4.06	4.83
D	0.027	0.037	0.69	0.94
E	0.045	0.055	1.14	1.40
F	0.530	0.545	13.46	13.84
G	0.067 BSC		1.70 BSC	
J	0.014	0.022	0.36	0.56
K	0.785	0.800	19.94	20.32
L	0.321	0.337	8.15	8.56
M	0.063	0.078	1.60	1.98
Q	0.146	0.156	3.71	3.96
R	0.271	0.321	6.88	8.15
S	0.146	0.196	3.71	4.98
U	0.460	0.475	11.68	12.07
W	5°		5°	

# CS8126

## TO-220 FIVE LEAD THA SUFFIX CASE 314A-03 ISSUE E

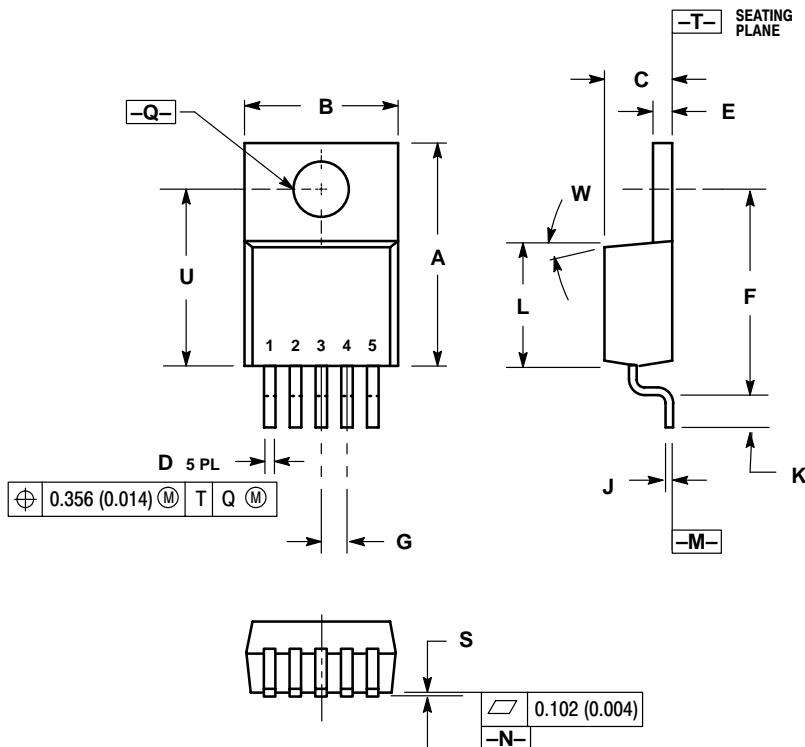


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DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
F	0.570	0.585	14.478	14.859
G	0.067 BSC		1.702 BSC	
J	0.015	0.025	0.381	0.635
K	0.730	0.745	18.542	18.923
L	0.320	0.365	8.128	9.271
Q	0.140	0.153	3.556	3.886
S	0.210	0.260	5.334	6.604
U	0.468	0.505	11.888	12.827

## TO-220 FIVE LEAD THE SUFFIX CASE 314J-01 ISSUE O



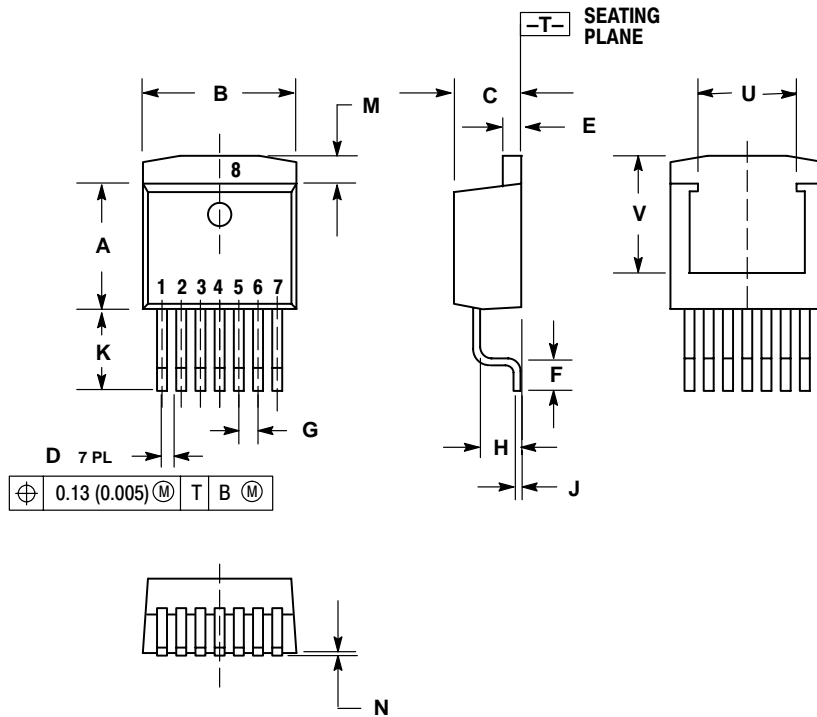
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.43) MAXIMUM.
4. DIMENSIONS EXCLUSIVE OF MOLD FLASH AND METAL BURRS.
5. FOOTPAD LENGTH MEASURED FROM LEAD TIP WITH REFERENCE TO DATUM -M-.
6. COPLANARITY 0.004" MAX. REFERENCE TO DATUM -N- STANDOFF HEIGHT 0.00 - 0.010".

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.568	0.583	14.43	14.81
B	0.395	0.405	10.03	10.29
C	0.170	0.180	4.32	4.57
D	0.028	0.036	0.71	0.91
E	0.045	0.055	1.14	1.40
F	0.543	0.558	13.79	14.17
G	0.067 BSC		1.70 BSC	
J	0.014	0.022	0.36	0.56
K	0.073	0.088	1.85	2.24
L	0.324	0.339	8.23	8.61
Q	0.146	0.156	3.71	3.96
S	0.000	0.010	0.00	0.25
U	0.460	0.475	11.68	12.07
W	5°		5°	

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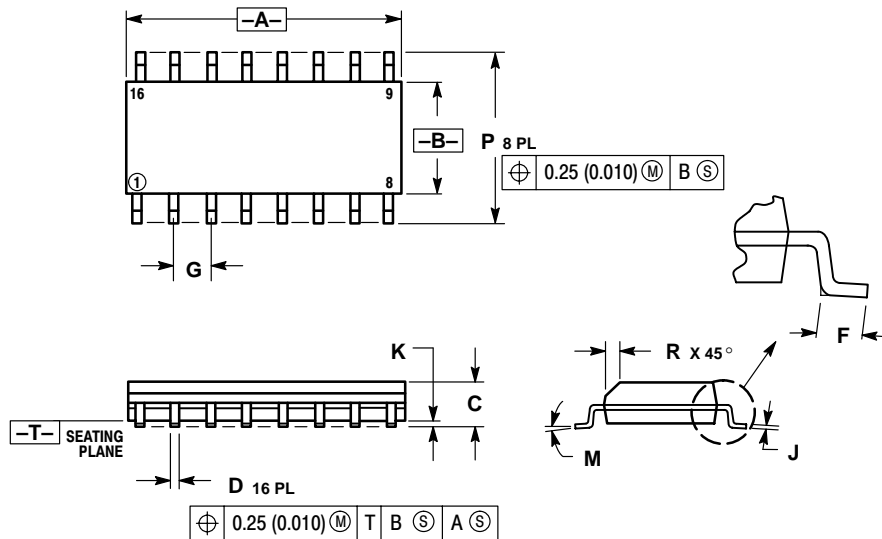
D<sup>2</sup>PAK  
7-PIN  
DPS SUFFIX  
CASE 936H-01  
ISSUE O



- NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS B AND M.
  4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAX.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.326	0.336	8.28	8.53
B	0.396	0.406	10.05	10.31
C	0.170	0.180	4.31	4.57
D	0.026	0.036	0.66	0.91
E	0.045	0.055	1.14	1.40
F	0.058	0.078	1.41	1.98
G	0.050 BSC		1.27 BSC	
H	0.100	0.110	2.54	2.79
J	0.018	0.025	0.46	0.64
K	0.204	0.214	5.18	5.44
M	0.055	0.066	1.40	1.68
N	0.000	0.004	0.00	0.10
U	0.256 REF		6.50 REF	
V	0.305 REF		7.75 REF	

SO-16L  
D SUFFIX  
CASE 751B-05  
ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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## PACKAGE THERMAL DATA

Parameter		TO-220 FIVE LEAD	D <sup>2</sup> PAK 7-PIN	SO-16L	Unit
R <sub>θJC</sub>	Typical	2.1	2.1	23	°C/W
R <sub>θJA</sub>	Typical	50	10-50*	105	°C/W

\*Depending on thermal properties of substrate.  $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$ .

# Notes

# Notes

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