65,536-WORD by 18-BIT HIGH SPEED BiCMOS SYNCHRONOUS STATIC RAM **Advanced Information**

Description

The CXK77B1810 is a high speed BiCMOS synchronous static RAM with common I/O pins, organized as 65,536-words by 18-bits. This synchronous SRAM integrates input registers, high speed SRAM, output registers/latches and write buffers onto a single monolithic IC. 4 different operation modes are offered for highest performance synchronous SRAM: Register-Register mode; Register-Latch mode; Register-Flow Thru mode; Dual clock mode.

All input signals except $\overline{G}$ (Output Enable) are latched at the positive edge of an external clock (K). With 4 different modes to be selected, the Read cycle can be operated as output registered on Register-Register mode; or as output latched on Register-Latch mode; or as output simply flow through on Register-Flow Thru mode; or as additional external clock (C) to control output register/latch on Dual clock mode.

Write operation is initiated by the positive edge of K and the data input is strobed into write buffer on the subsequent clock cycle. The write cycle is started by multiplexing the address and data of internal write buffers and writing into SRAM core while the current cycle's address and data are stored into write buffers. The write buffer is one entry deep and allows data to be input one clock cycle later which eliminates one dead cycle for Read followed by Write cycles. In both Register-Latch and Register-Flow Thru modes, the positive edge of K on a write cycle tri-states the SRAM's output buffer which allow consecutive Read-Write-Read cycles. Write cycle is internally self-timed which eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

The output drivers are series terminated and the output impedance is programmable through a external matching resistor RQ. By connecting RQ between ZQ pin and VSS, the output impedance of all 18 DQ pins is precisely controlled. The value of RQ is scaled to 5X of the driver impedance.

Power down control is provided through asynchronous ZZ input. 200 MHz operation is obtained from a single 3.3V power supply. Boundary scan interface is provided using IEEE standard 1149.1 protocol.

Features

- 4 synchronous operation modes:

  Register-Register; Register-Latch; Register-Flow Thru; Dual Clock Mode
- High speed, low power consumption.
- Single +3.3V power supply: 3.3V ± 5%
- Dedicated Output Supply Voltage : VDDQ
- Inputs and outputs level are HSTL compatible.
- Precise output driver impedance control.
- Differential clock input (K/$\overline{K}$, C/$\overline{C}$) to minimized system clock skew.
- Byte Write capability.
- Common data input and output.
- 5 ns cycle time (200 MHz).
- All inputs (except Output Enable) and outputs are registered on a single clock edge.
- Asynchronous Output Enable control.
- Delay Write scheme to eliminate dead cycle for Read followed by Write operation.
- Consecutive Read-Write-Read operation achieves separate data IO performance.
- Self-timed write cycle.
- Power down mode.
- JTAG test mode conforms to IEEE standard 1149.1 is provided.
- Available in a 50 mil pitch 7X17 Plastic Ball Grid Array package.

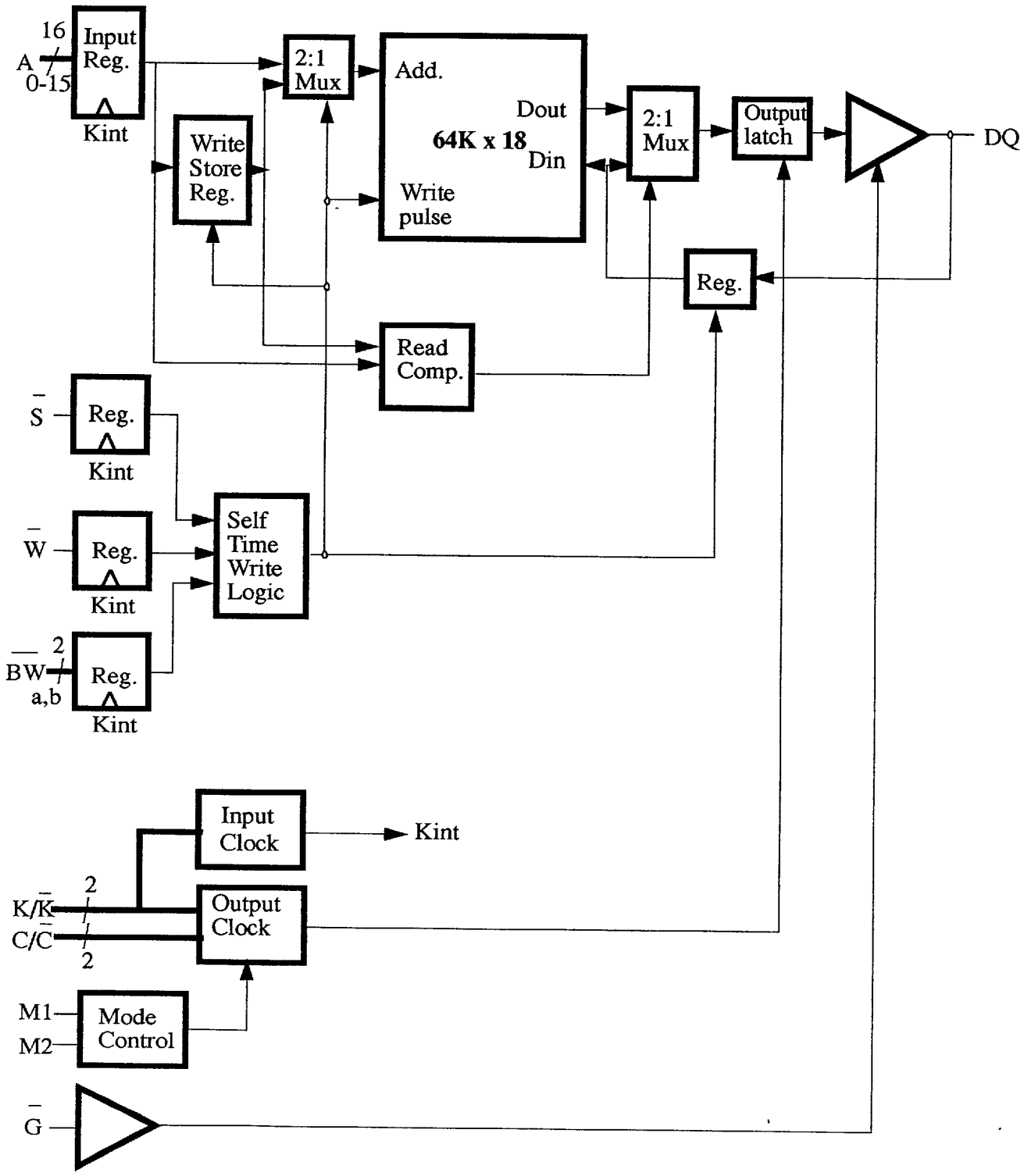
Pin Configuration (Top View)

	1	2	3	4	5	6	7
A	VDDQ	A7	A4	NC	A3	A0	VDDQ
B	NC	NC	NC	NC	NC	NC	NC
C	NC	A6	A5	VDD	A2	A1	NC
D	DQ1b	NC	VSS	ZQ	VSS	DQ9b	NC
E	NC	DQ2b	VSS	$\overline{S}$	VSS	NC	DQ8a
F	VDDQ	NC	VSS	$\overline{G}$	VSS	DQ7a	VDDQ
G	NC	DQ3b	$\overline{BW}$b	$\overline{C}$	VSS	NC	DQ6a
H	DQ4b	NC	VSS	C	VSS	DQ5a	NC
J	VDDQ	VDD	VREF	VDD	VREF	VDD	VDDQ
K	NC	DQ5b	VSS	K	VSS	NC	DQ4a
L	DQ6b	NC	VSS	$\overline{K}$	$\overline{BW}$a	DQ3a	NC
M	VDDQ	DQ7b	VSS	$\overline{W}$	VSS	NC	VDDQ
N	DQ8b	NC	VSS	A9	VSS	DQ2a	NC
P	NC	DQ9b	VSS	A11	VSS	NC	DQ1a
R	NC	A8	M1	VDD	M2	A12	NC
T	NC	A10	A15	NC	A13	A14	ZZ
U	VDDQ	TME	TDI	TCK	TDO	NC	VDDQ

Pin Description

Symbol	Description	Symbol	Description	Symbol	Description
A	Address Input (0-15)	$\overline{W}$	Write Enable	TDO	JTAG Data Out
DQ	Data I/O 1-9 in byte a,b	$\overline{BW}$x	Byte Write Enable (a,b)	VDD	+3.3V power supply
K	Positive Clock	$\overline{G}$	Asyn Output Enable	VDDQ	Output power supply
$\overline{K}$	Negative Clock	ZZ	Sleep Mode Select	VSS	Ground
C	Output positive clock	TCK	JTAG Clock	VREF	Input reference voltage
$\overline{C}$	Output negative clock	TMS	JTAG Mode Select	ZQ	Output impedance control resistor input
$\overline{S}$	Chip Select	TDI	JTAG Data In	M1,M2	Mode Select
				NC	No Connect

BLOCK DIAGRAM



Absolute Maximum Ratings (T_a = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	VDD	-0.5 to +4.6	V
Output supply voltage	VDDQ	-0.5 to +4.6	
Input voltage	V_{IN}	-0.5 to VDD+0.5 (4.6V max.)	V
Output voltage	V_O	-0.5 to VDDQ+0.5 (4.6V max.)	V
Allowable power dissipation	P_D	2.0	W
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	-55 to 150	°C

Truth Table

Register - Register mode

ZZ	$\overline{S}$ (t_n)	$\overline{W}$ (t_n)	$\overline{BW}$x (t_n)	$\overline{G}$	Mode	DQ_{0-17} (t_n)	DQ_{0-17} (t_{n+1})	VDD Current
H	X	X	X	X	Sleep mode. Power down	Hi - Z	Hi - Z	I_{SB}
L	H	X	X	X	Deselect	X	Hi - Z	I_{DD}
L	L	H	X	H	Read	Hi - Z	Hi - Z	I_{DD}
L	L	H	X	L	Read	X	$Q(t_n)$	I_{DD}
L	L	L	L	X	Write both bytes (bits 0-17)	X	$D(t_n)$	I_{DD}
L	L	L	X	X	Write bytes with $\overline{BW}$x=L	X	$D(t_n)$	I_{DD}
L	L	L	H	X	Aborted Write	X	X	I_{DD}

Register - Latch mode and Register - Flow Thru mode

ZZ	$\overline{S}$ (t_n)	$\overline{W}$ (t_n)	$\overline{BW}$x (t_n)	$\overline{G}$	Mode	DQ_{0-17} (t_n)	DQ_{0-17} (t_{n+1})	VDD Current
H	X	X	X	X	Sleep mode. Power down	Hi - Z	Hi - Z	I_{SB}
L	H	X	X	X	Deselect	Hi - Z	X	I_{DD}
L	L	H	X	H	Read	Hi - Z	Hi - Z	I_{DD}
L	L	H	X	L	Read	$Q(t_n)$	X	I_{DD}
L	L	L	L	X	Write both bytes (bits 0-17)	Hi - Z	$D(t_n)$	I_{DD}
L	L	L	X	X	Write bytes with $\overline{BW}$x=L	Hi - Z	$D(t_n)$	I_{DD}
L	L	L	H	X	Aborted Write	Hi - Z	X	I_{DD}

Mode Select Truth Table

	M1	M2
Register-Register	L	H
Register-Flow Thru	L	L
Register-Latch	H	L
Dual Clock Mode	H	H

Dual clock mode will be updated on the later revision.

DC Recommended Operating Conditions **(T_a = 25°C, GND =0V)**

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	VDD	3.15	3.3	3.45	V
Output supply voltage	VDDQ	1.14	---	1.6	V
Input reference voltage	VREF	0.5	---	0.9	V
Input high voltage	V_{IH}	VREF + 0.1	---	VDDQ + 0.3	V
Input low voltage	V_{IL}	-0.3	---	VREF - 0.1	V
Input high voltage in Test Mode	VTIH	2.0	---	VDD+0.3	V
Input low voltage in Test Mode	VTIL	-0.3	---	0.8	V
Differential clock input signal	V_{DIF}	0.2	---	VDDQ+0.6	V
Differential clock input common mode voltage	V_{CM}	0.5	---	0.9	V
Differential clock input cross point voltage	V_X	0.5	---	0.9	V
Output impedance matching resistor connect between ZQ and VSS.	RQ	200	250	350	Ω

•DC and operating characteristics

(VCC = 3.3V± 5%, GND = 0V, T_a = 0 to 70°C)

Item	Symbol	Test conditions	Min	Typ*	Max	Unit
Input leakage current	I_{LI}	Vin = GND to VDD	-1	---	1	uA
Output leakage current	I_{LO}	V_O = GND to VDD $\overline{G}$ = V_{IH}	-10	---	10	uA
Operating power supply current	I_{DD}	Cycle = min. Duty =100% Iout=0mA	---	---	580	mA
Standby Current	I_{SB}	ZZ ≥ VIH			20	mA
Output high voltage	V_{OH}	I_{OH} = -2.0 mA RQ=250Ω	VDDQ-0.4	---	---	V
Output low voltage	V_{OL}	I_{OL} = 6.0 mA RQ=250Ω	---	---	0.4	V
Output driver impedance	R_{OUT}[1,2,3]	V_{OH}=VDDQ/2 V_{OL}=VDDQ/2	0.9*RQ/5	RQ/5	1.1*RQ/5	Ω

1. RQ needs to be ranged from minimum of 200Ω to maximum of 350Ω for proper control of the value of R_{OUT}.
   1.1 R_{OUT} ≤ 44Ω (1.1*200Ω/5) when RQ ≤ 200Ω
   1.2 R_{OUT} ≥ 63Ω (0.9*350Ω/5) when RQ ≥ 350Ω
2. For maximum output drive ZQ pin can tie directly to VSS. The output impedance is described as note 1.1.
3. For minimum output drive, ZQ pin can be no connect or tie to VDDQ. The output impedance is described in note 1.2.

•I/O capacitance

(T_a = 25°C, f = 1 MHz)

Item	Symbol	Test conditions	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	---	5	pF
Clock input capacitance	C_{CLK}	V_{IN} = 0V	---	8	pF
Output capacitance	C_{OUT}	V_{OUT} = 0V	---	8	pF

•AC ELECTRICAL CHARACTERISTICS

Item	Symbol	-5		-6		-7		Unit
		Min	Max	Min	Max	Min	Max	
Address access (Latch and Flow Thru modes)	t_{AA}		7.5	---	9	---	10	ns
Clock period	t_{KP}	5		6	---	7	---	ns
Clock pulse high	t_{KH}	2		2	---	3	---	ns
Clock pulse low	t_{KL}	2		2	---	3	---	ns
Setup time	t_S	0.5		0.5	---	1	---	ns
Hold time	t_H	1.5		1.5	---	1.5	---	ns
Clock high to output (Register-Register mode only)	t_{KQ}	1.5	3	1.5	3.5	1.5	4	ns
Clock high to output (Latch and Flow Thru modes)	t_{KQ1}		7	---	7	---	8	ns
Clock low to output (Latch mode only)	t_{KQ2}	1	3	1	3	1	3.5	ns
Write cycle clock high to following Read cycle output (Latch and Flow Thru modes)	t_{KQ3}		14		15		17	ns
Clock high to output high impedance ($\overline{S}$ deselect cycle)	t_{HZ} *2	1	3	1.5	3.5	1.5	4	ns
Write cycle clock high to output high impedance (Latch and Flow Thru modes)	t_{WHZ} *2	1	3	1.5	3	1.5	3.5	ns
Clock high to output low impedance (Register-Register mode only)	t_{LZ} *2	1.5		1.5	---	1.5	---	
Clock high to output low impedance (Flow Thru mode only)	t_{LZ1} *2	1.5		1.5	---	1.5	---	ns
Clock low to output low impedance (Latch mode only)	t_{LZ2} *2	1		1	---	1	---	ns
Output enable to output valid ($\overline{G}$)	t_{OE}		3	---	3	---	3.5	ns
Output enable to output in low Z ($\overline{G}$)	t_{OLZ} *2	1		1	---	1	---	ns
Output disable to output in high Z ($\overline{G}$)	t_{OHZ} *2		3	---	3	---	3.5	ns

1. All parameters are specified over the range 0-70°C.
2. These parameters are sampled and are not 100% tested.

AC characteristics

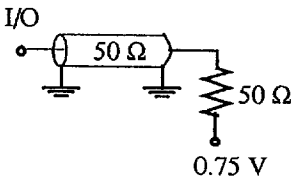
• AC test conditions

(VDD = 3.3V ± 5%, Ta = 0 to 70°C)

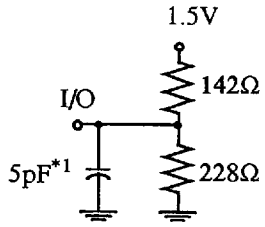
Item	Conditions
Input reference voltage	V_{REF}=0.75 V
Input pulse high level	V_{IH}=1.25 V
Input pulse low level	V_{IL}=0.25 V
Input rise & fall time	1V/ns
Input reference level	0.75 V
Clock input reference level	K/$\overline{K}$ cross; C/$\overline{C}$ cross
Clock input differential signal	1.0 V
Clock input crossing level	0.75 V
Clock input rise & fall time	1V/ns
Output supply voltage	VDDQ=1.5V
Output reference level	0.75 V
Output load conditions	Fig.1

FIG.1

Output Load (1)



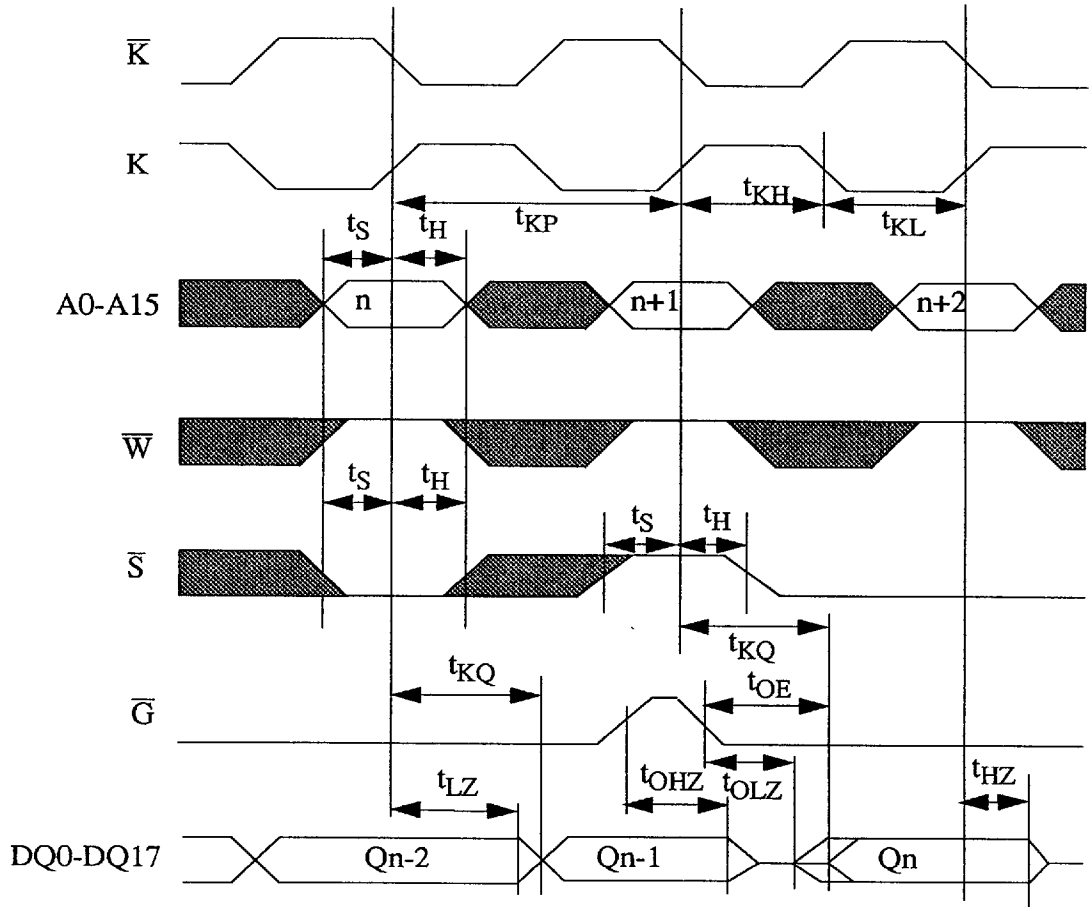
Output Load*2 (2)



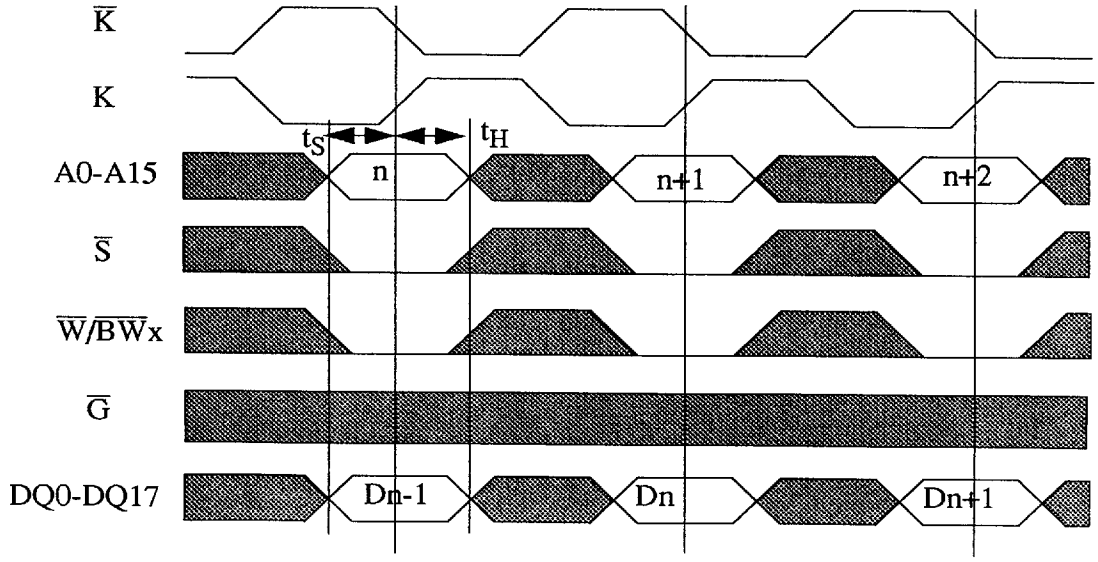
1. Including scope and jig capacitance.
2. For t_{LZ}, t_{HZ}.

Register - Register mode

TIMING WAVEFORM OF READ CYCLE

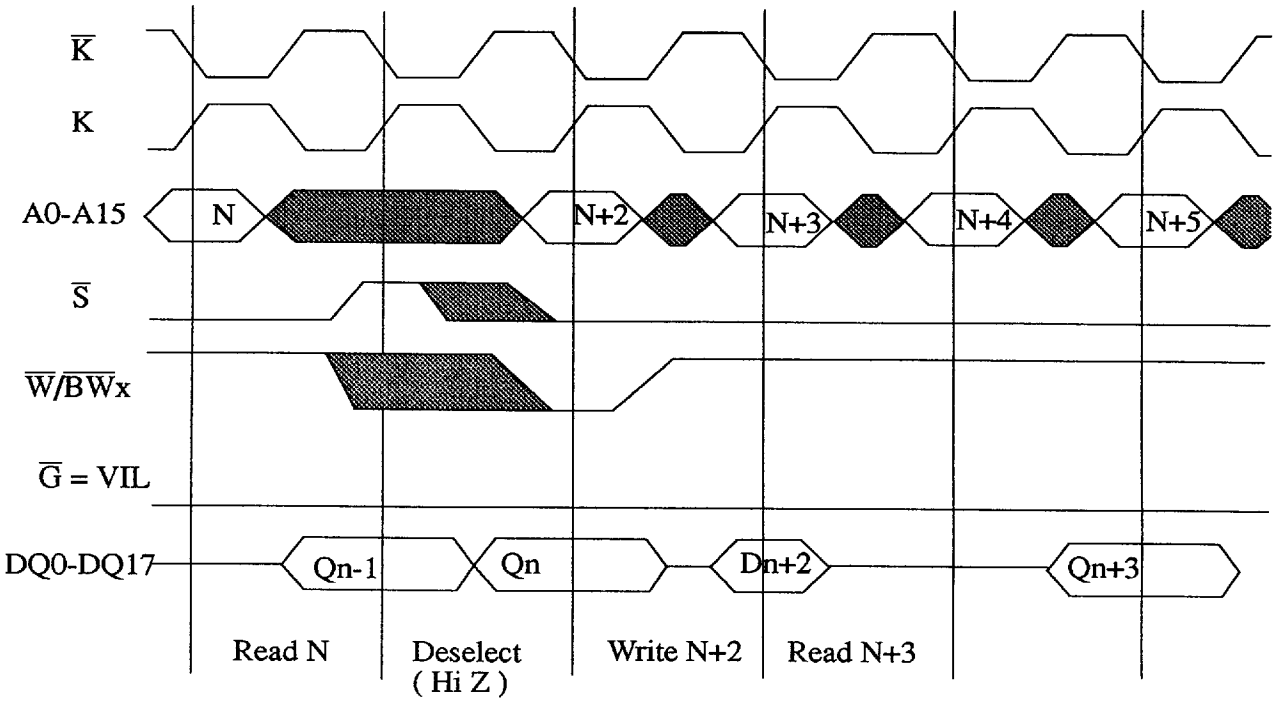


TIMING WAVEFORM OF WRITE CYCLE

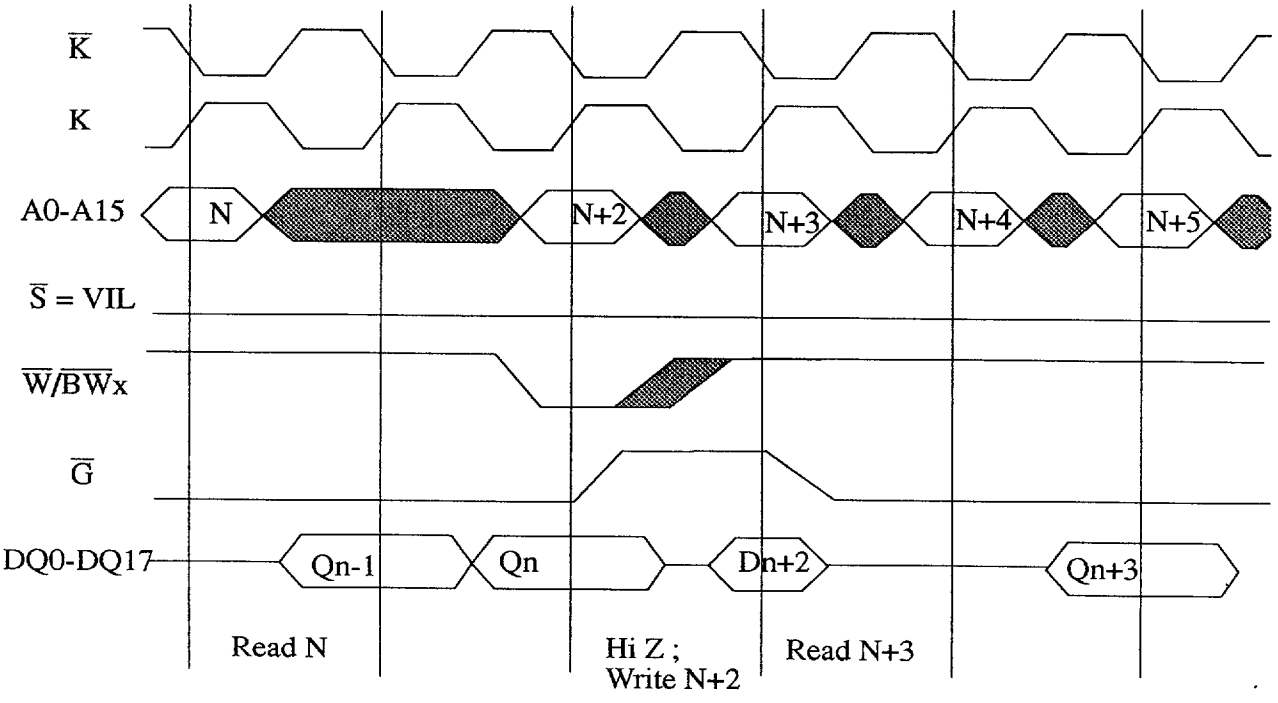


Register - Register mode

TIMING WAVEFORM OF READ-WRITE-READ CYCLE I ($\overline{S}$ controlled)

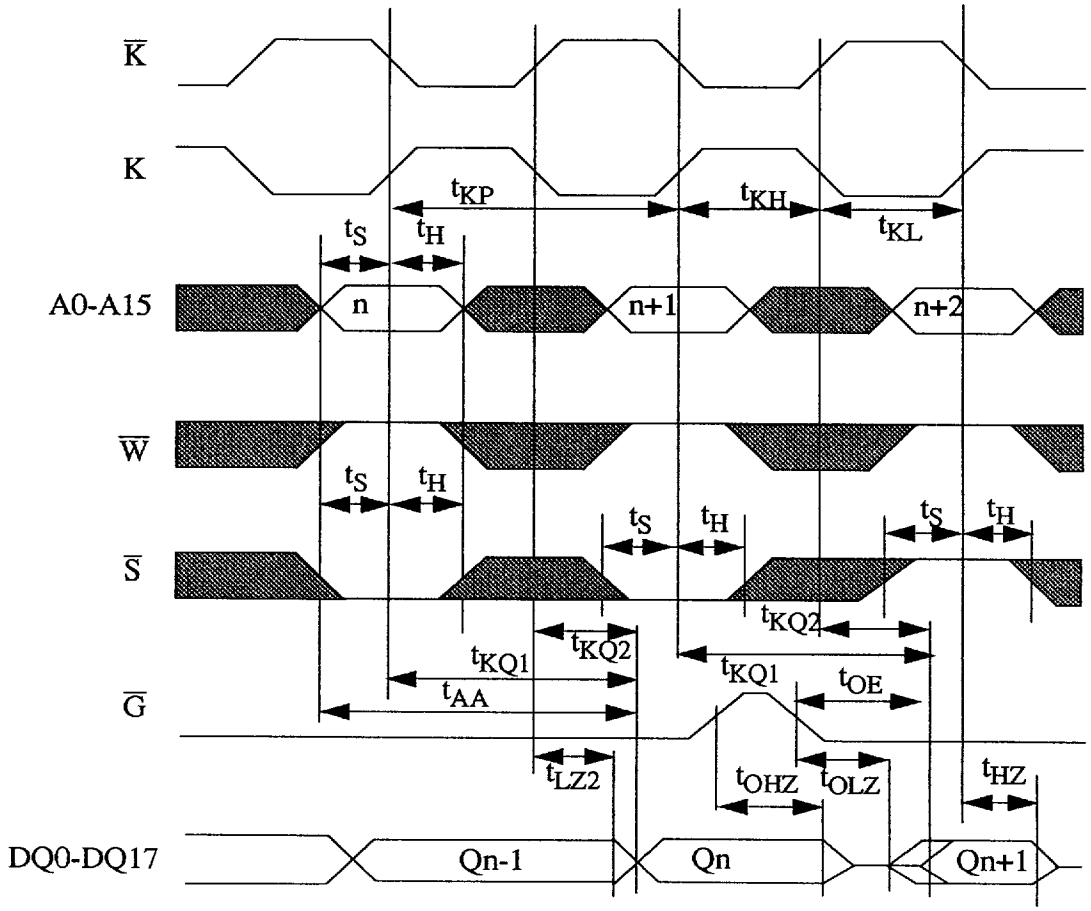


TIMING WAVEFORM OF READ-WRITE-READ CYCLE II ($\overline{G}$ controlled)

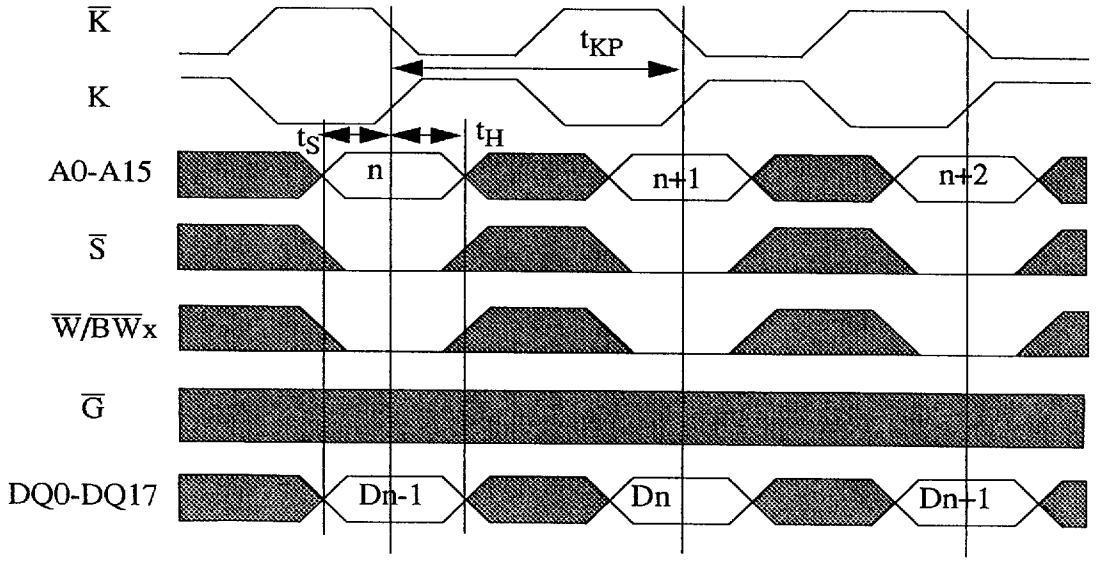


Register - Latch mode

TIMING WAVEFORM OF READ CYCLE

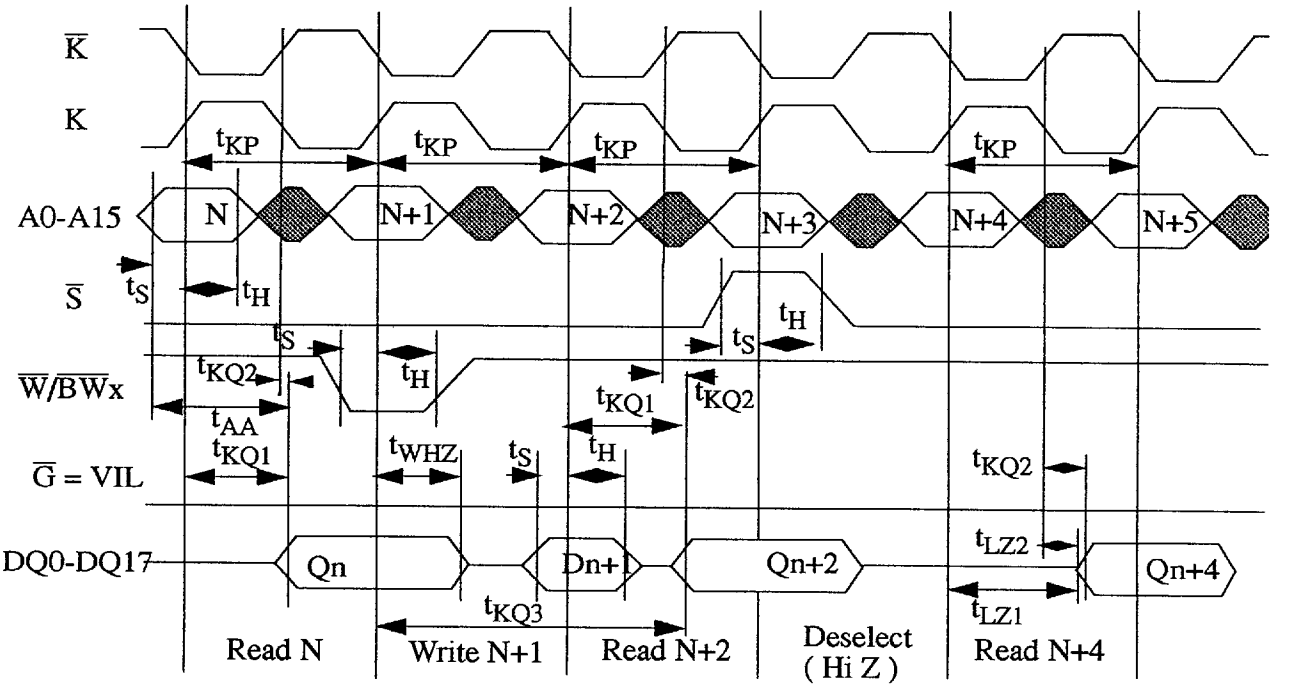


TIMING WAVEFORM OF WRITE CYCLE



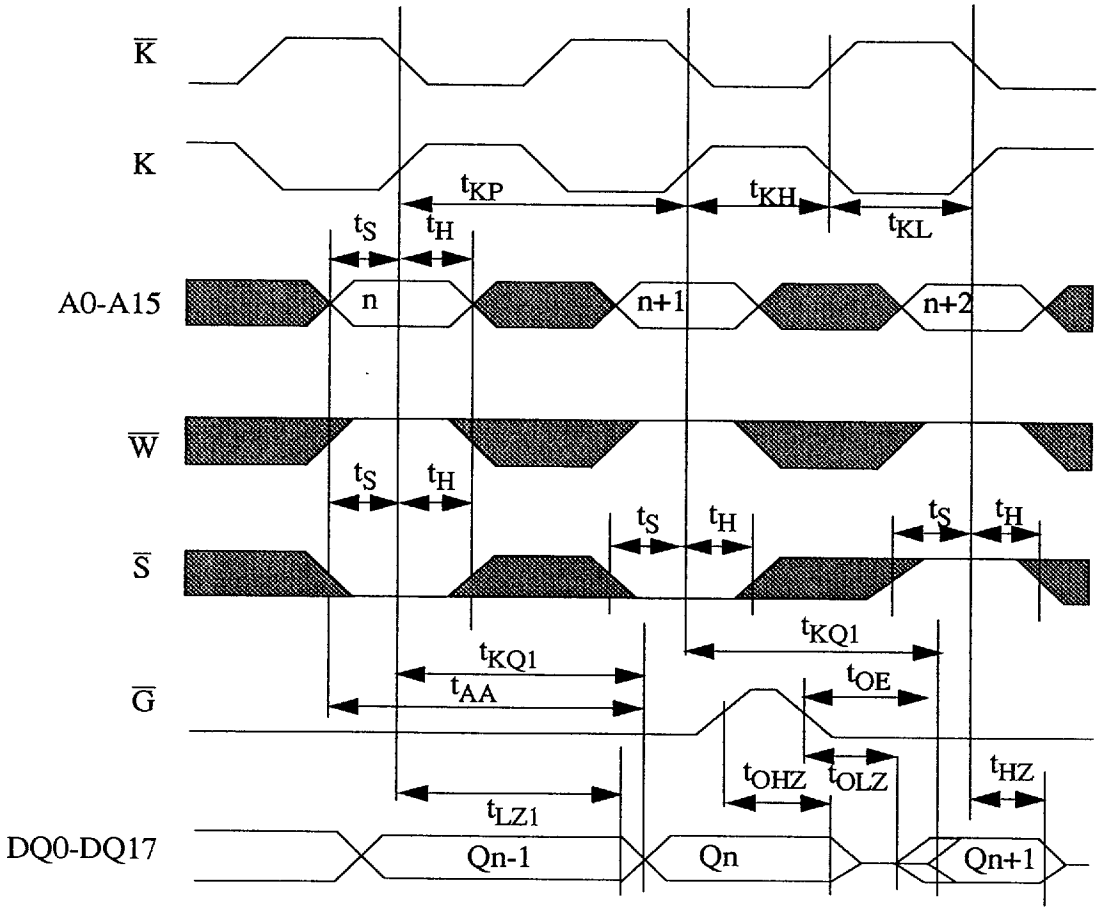
Register - Latch mode

TIMING WAVEFORM OF READ-WRITE-READ CYCLE

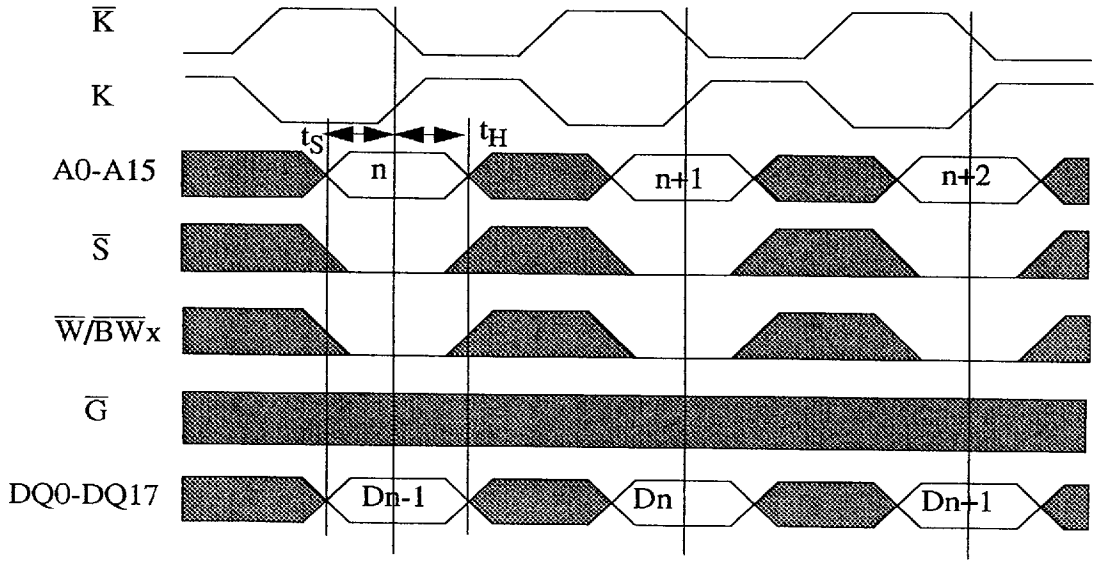


Register - Flow Thru mode

TIMING WAVEFORM OF READ CYCLE

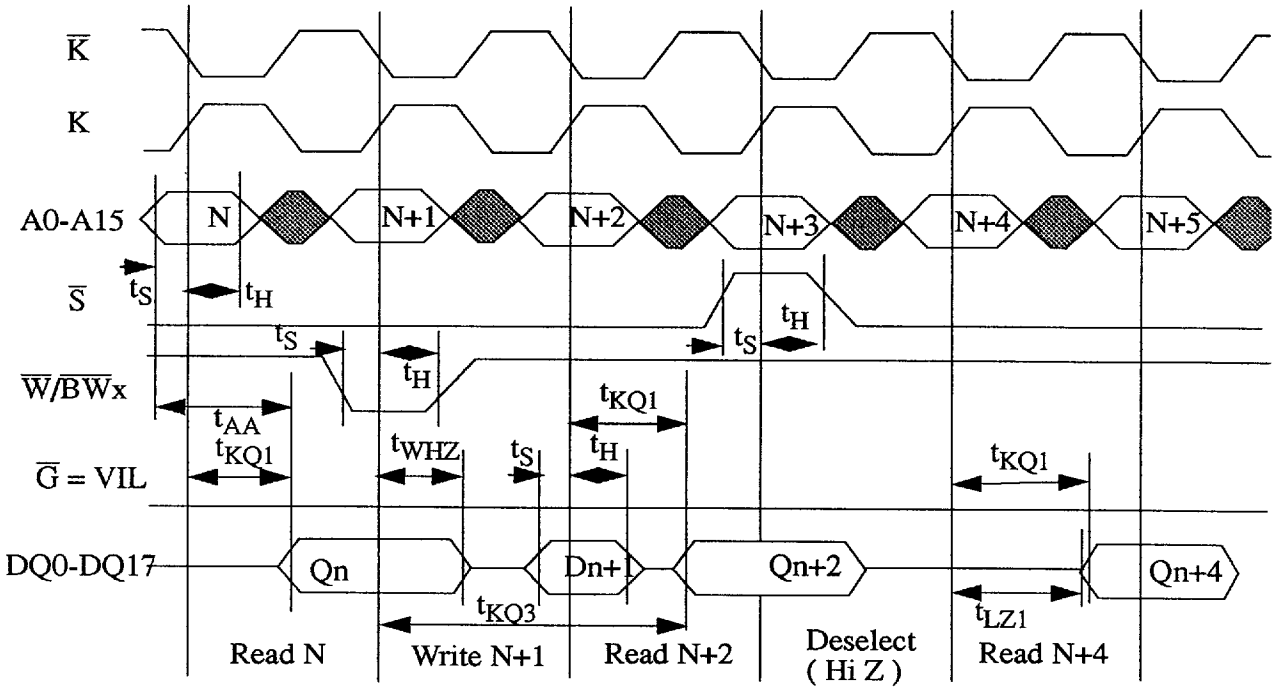


TIMING WAVEFORM OF WRITE CYCLE



Register - Flow Thru mode

TIMING WAVEFORM OF READ-WRITE-READ CYCLE



Test Mode Description

Functional Description

The CXK77B1810 provides JTAG boundary scan interface using IEEE std. 1149.1 protocol. The test mode is intended to provided a mechanism for testing the interconnect between master (processor, controller, etc.), SRAMs, other components and print circuit board.

In conformance with IEEE std. 1149.1, the CXK77B1810 contains a TAP controller, Instruction register, Boundary scan register and Bypass register.

Test Access Port (TAP)

4 pins as defined in Pin Description table are used to perform JTAG functions. TDI input pin is used to scan test data serially into one of three registers (Instruction register, Boundary scan register and Bypass register). TDO is output pin used to scan test data serially out. The TDI send the data into LSB of selected register and the MSB of the selected register feeds the data to TDO. TMS input pin controls the state transition of 16 state TAP controller as specified in IEEE std. 1149.1. Inputs on TDI, TMS are registered on the rising edge of TCK clock and the output data on TDO is presented on the falling edge of TCK. TDO driver is in active state only when TAP controller is in Shift-IR state or in Shift-DR state.

TAP Controller

16 state controller is implemented as specified in IEEE std. 1149.1.

The controller enter reset state in one of three ways:

1. Power up

2. Apply logic 1 on TMS input pin on 5 consecutive TCK rising edges.

Instruction Register (3 bits)

The JTAG Instruction register is consisted of shift register stage and parallel output latch. The register is 3 bits wide and is encoded as follow:

Octal	MSB.....LSB			Instruction
0	0	0	0	Bypass
1	0	0	1	IDCODE. Read device ID
2	0	1	0	Sample-Z. Sample Inputs and tri-state DQs
3	0	1	1	Bypass
4	1	0	0	Sample. Sample Inputs.
5	1	0	1	Private. Manufacturer use only.
6	1	1	0	Bypass
7	1	1	1	Bypass

Bypass Register (1 bit)

The Bypass Register is one bit wide and is connected electrically between TDI and TDO and provides the minimum length serial path between TDI and TDO.

ID Registers (32 bits)

The ID Register are 32 bits wide and are listed as follow:

	ID[0}	1
Sony ID	ID[11:1]	0000 1110 001
Part Number	ID[27:12]	0000 0000 0000 0010
Revision Number	ID[31:28]	xxxx

Boundary Scan Register (51 bits)

The Boundary Scan Registers are 51 bits wide and are listed as follow:

DQ	18
A	16
$\overline{W}$, $\overline{BW}$x	3
$\overline{S}$, $\overline{G}$	2
K, $\overline{K}$, C, $\overline{C}$	4
ZZ	1
Mode	2
ZQ	1
Place Holder	4

K/ $\overline{K}$, C/$\overline{C}$ inputs are sampled through one differential stage and internal inverted to generate internal K/$\overline{K}$, C/$\overline{C}$ signals for scan registers. Place Holder are required for some NC pins to maintain 51 bits Scan Register for different types of same family SRAM and for density upgrade. All Place Holder Registers are connected to VSS internally regardless of pin connection externally.

Scan Order (Order by exit sequence)

27	-	VSS		VSS	-	26
28	3A	A		VSS	-	25
29	3C	A		VSS	-	24
30	2C	A		A	5A	23
31	2A	A		A	5C	22
32	1D	DQb		A	6C	21
33	2E	DQb		A	6A	20
34	2G	DQb		DQa	6D	19
35	1H	DQb		DQa	7E	18
36	3G	/Wb		DQa	6F	17
37	4D	ZQ		DQa	7G	16
38	4E	/S		DQa	6H	15
39	4G	/C		/G	4F	14
40	4H	C		K	4K	13
41	4M	/W		/K	4L	12
42	2K	DQb		/Wa	5L	11
43	1L	DQb		DQa	7K	10
44	2M	DQb		DQa	6L	9
45	1N	DQb		DQa	6N	8
46	2P	DQb		DQa	7P	7
47	3T	A		ZZ	7T	6
48	2R	A		A	5T	5
49	4N	A		A	6R	4
50	2T	A		A	4P	3
51	3R	M1		A	6T	2
				M2	5R	1