



HC-55564

Continuously Variable
Slope Delta-modulator (CVSD)

Features

- All Digital
- Requires Few External Parts
- Low Power Drain: 1.5mW Typical From Single 3.0V-7V Supply
- Time Constants Determined by Clock Frequency; No Calibration or Drift Problems; Automatic Offset Adjustment
- Half Duplex Operation Under Digital Control
- Filter Reset Under Digital Control
- Automatic Overload Recovery
- Automatic "Quiet" Pattern Generation
- AGC Control Signal Available

Applications

- Voice Transmission Over Data Channels (Modems)
- Voice/Data Multiplexing (Pair Gain)
- Voice Encryption/Scrambling
- Voicemail
- Audio Manipulations: Delay Lines, Time Compression, Echo Generation/Suppression, Special Effects, Etc.
- Pagers/Satellites
- Data Acquisition Systems
- Voice I/O For Digital Systems and Speech Synthesis Requiring Small Size, Low Weight, and Ease of Reprogrammability

Description

The HC-55564 is a half duplex modulator/demodulator CMOS integrated circuit used to convert voice signals into serial NRZ digital data and to reconvert that data into voice. The conversion is by delta-modulation, using the Continuously Variable Slope (CVSD) method of modulation/de-modulation.

While the signals are compatible with other CVSD circuits, the internal design is unique. The analog loop filters have been replaced by very low power digital filters which require no external timing components. This approach allows inclusion of many desirable features which would be difficult to implement using other approaches.

The fundamental advantages of delta-modulation, along with its simplicity and serial data format, provide an efficient (low data rate/low memory requirements) method for voice digitization. The device may be easily configured with the HC-5512C/12D PCM/CVSD filter.

The HC-55564 is usable from 9K bits/sec to above 64Kbps. The unit is available in a 14 pin ceramic DIP or LCC package in commercial, industrial, and military temperature ranges including the Harris High Rel Dash 7 and Dash 8 programs. Application Notes 607 and 576 are available, as are Demonstration Boards.

Functional Diagram

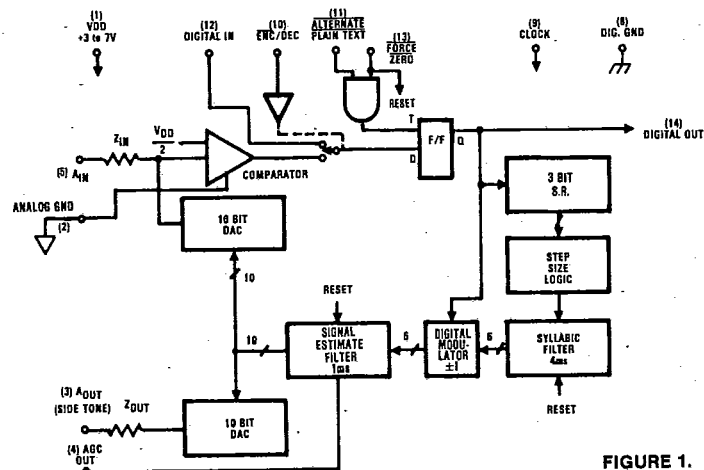
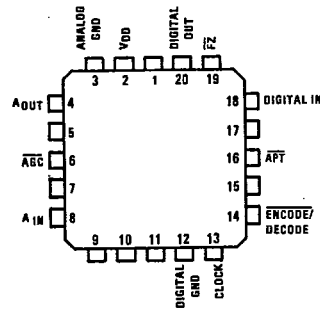
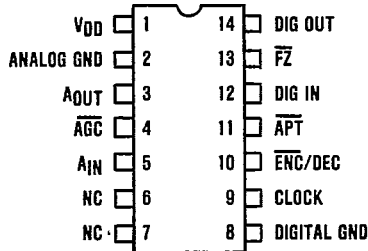


FIGURE 1.

Pinouts

TOP VIEWS



Pin Assignments

PIN # 14-PIN DIP	PIN # 20-PIN LCC	SYMBOL	DESCRIPTION
1	2	VDD	Positive supply voltage. Voltage range is +3.0V to +7.0V.
2	3	Analog Gnd	Analog Ground connection to D/A ladders and comparator.
3	4	AOUT	Audio Out recovered from 10 bit DAC. May be used as side tone at the transmitter. Presents approximately 150 kilohm source with DC offset of $V_{DD}/2$. Within $\pm 2\text{dB}$ of Audio Input. Should be externally AC coupled.
4	6	AGC	Automatic Gain Control output. A logic low level will appear at this output when the recovered signal excursion reaches one-half of full scale value. In each half cycle full scale is $V_{DD}/2$. The mark-space ratio is proportional to the average signal level.
5	8	AIN	Audio Input to comparator. Should be externally AC coupled. Presents approximately 280 kilohms in series with $V_{DD}/2$.
6,7	1,5,7,9, 10,11, 15,17	NC	No internal connection is made to these pins.
8	12	Digital Gnd	Logic ground. 0V reference for all logic inputs and outputs
9	13	Clock	Sampling rate clock. In the decode mode, must be synchronized with the digital input data such that the data is valid at the positive clock transition. In the encode mode, the digital data is clocked out on the negative going clock transition. The clock rate equals the data rate.
10	14	Encode/ Decode	A single CVSD can provide half-duplex operation. The encode or decode function is selected by the logic level applied to this input. A low level selects the encode mode, a high level the decode mode.
11	16	APT	Alternate Plain Text input. Activating this input causes a digital quieting pattern to be transmitted, however; internally the CVSD is still functional and a signal is still available at the AOUT port. Active low.
12	18	Digital In	Input for the received digital NRZ data.
13	19	FZ	Force Zero input. Activating this input resets the internal logic and forces the digital output and the recovered audio output into the "quieting" condition. An alternating 1-0 pattern appears at the digital output at $1/2$ the clock rate. When this is decoded by a receive CVSD, a 10mVp-p inaudible signal appears at audio output. Active low.
14	20	Digital Out	Output for transmitted digital NRZ data.

NOTE: No active input should be left in a "floating condition."

8
TELECOM-
MUNICATIONS

Specifications HC-55564

Absolute Maximum Ratings

Voltage at Any Pin GND -0.3V to V_{DD} +0.3V
 Maximum V_{DD} Voltage +7.0V
 Minimum V_{DD} Voltage +3.0V
 Operating V_{DD} Range +3.0V to +7.0V

Operating Temperature

Storage Temperature -65°C to +150°C
 Operating Temperature -55°C to +125°C

Electrical Characteristics

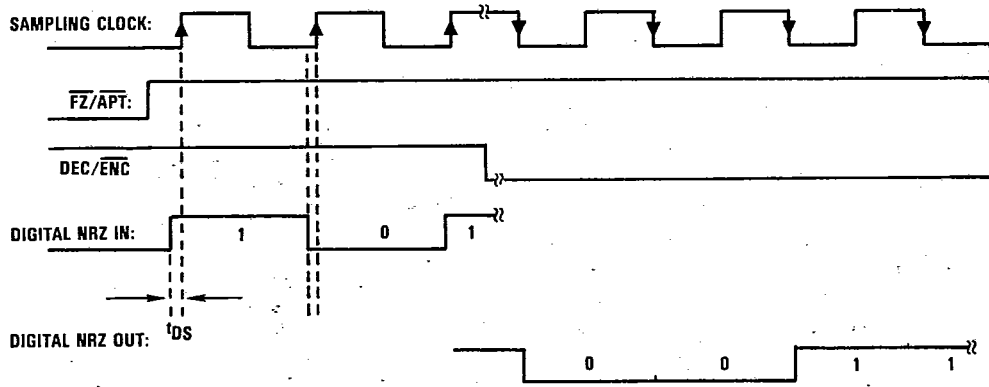
Unless otherwise noted, T_A = 25°C, V_{DD} = +5.0V, Sampling Rate = 16Kbps, AG = DG = 0V, A_{IN} = 1.2Vrms.

SYMBOL	PARAMETER	MIN	TYPICAL	MAX	UNITS	CONDITIONS
CLK	Sampling Rate	9	16	64	Kbps	Note 1
I _{DD}	Supply Current		0.3	1.5	mA	
V _{IH}	Logic '1' Input	3.5			V	Note 2
V _{IL}	Logic '0' Input			1.5	V	Note 2
V _{OH}	Logic '1' Output	4.0			V	Note 3
V _{OL}	Logic '0' Output			0.4	V	Note 3
	Clock Duty Cycle	30		70	%	
A _{IN}	Audio Input Voltage		0.5	1.2	Vrms	AC coupled. Note 4
A _{OUT}	Audio Output Voltage		0.5	1.2	Vrms	AC coupled. Note 5
Z _{IN}	Audio Input Impedance		280		kΩ	Note 6
Z _{OUT}	Audio Output Impedance		150		kΩ	Note 6
A _{E-D}	Transfer Gain	-2.0		+2.0	dB	No Load. Audio In to Audio Out.
A _E	Encode Gain		.34		dB	
A _D	Decode Gain		1.23		dB	
t _{SF}	Syllabic Filter Time Constant		4.0		mS	Note 7
t _{SE}	Signal Estimate Filter Time Constant	1.0			mS	Note 7
	Resolution		0.1		%	Note 8
	Minimum Step Size		0.2		%	Note 9
V _{QP}	Quieting Pattern Amplitude		10		mVp-p	FZ = 0V or APT = 0V, or A _{IN} = 0V. Note 10
V _{AL}	AGC Lo Threshold		1.24		Vp-p	Note 11
V _{AH}	AGC Hi Threshold		3.85		Vp-p	Note 11
V _{CTH}	Clamping Threshold		0.75		F.S.	Note 12

NOTES:

1. There is one NRZ (Non-Return Zero) data bit per clock period. Data is clocked out on the negative clock edge. Data is clocked into the CVSD on the positive going edge (see Figure 2). Clock may be run at less than 9Kbps and greater than 64Kbps.
2. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate.
3. Logic outputs are CMOS compatible at supply voltage and will withstand short-circuits to V_{DD} or ground. Digital data output is NRZ and changes with negative clock transitions. Each output will drive two LS TTL loads.
4. Recommended voice input range for best voice performance. Should be externally AC coupled.
5. May be used for side-tone in encode mode. Should be externally AC coupled. Varies with audio input level by ± 2 dB.
6. Presents series impedance with audio signal. Zero signal reference is approximately $V_{DD}/2$.
7. Note that filter time constants are inversely proportional to clock rate. Both filters approximate single pole responses.
8. Minimum quantization voltage level expressed as a percentage of supply voltage.
9. The minimum step size between levels is twice the resolution.
10. The "quieting" pattern or idle-channel audio output steps at one-half the bit rate, changing state on negative clock transitions.
11. A logic "0" will appear at the AGC output pin when the recovered signal reaches one-half of full-scale value (positive or negative), i.e. at $V_{DD}/2 \pm 25\%$ of V_{DD} .
12. The recovered signal will be clamped, and the computation will be inhibited, when the recovered signal reaches three-quarters of full-scale value, and will unclamp when it falls below this value (positive or negative).

Timing Waveforms



t_{DS} : DATA SET UP TIME, 100ns TYPICAL

FIGURE 2. CVSD TIMING DIAGRAM

Interface Circuit for HC-55564 CVSD

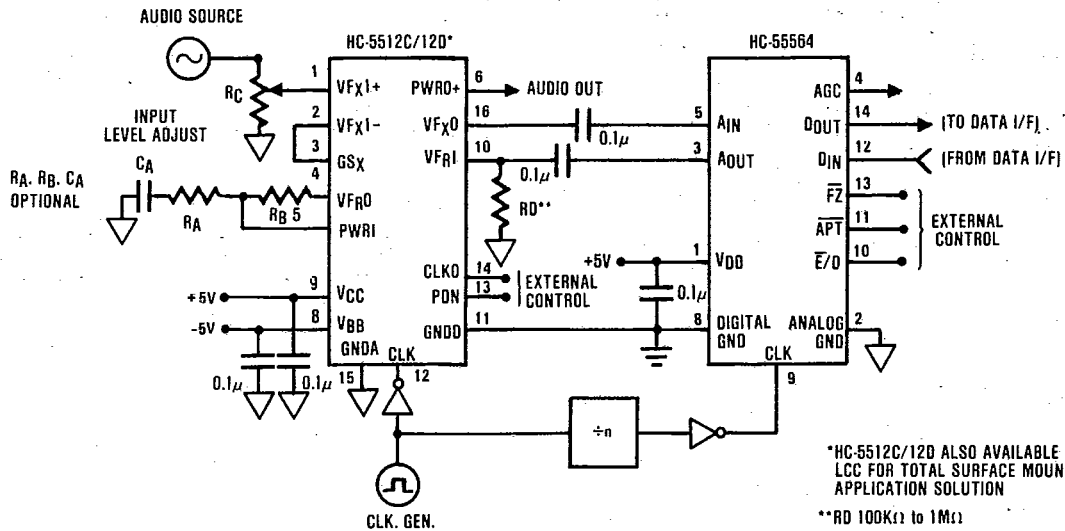
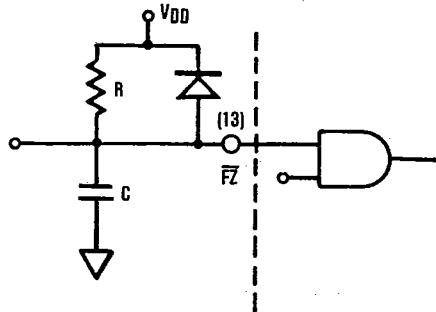


FIGURE 3.

CVSD Hookup for Evaluation

The circuit in Figure 3 is sufficient to evaluate the voice quality of the CVSD, since when encoding the feedback signal at the audio output pin is the reconstructed audio input signal. CVSD design considerations are as follows;

- 1) Care should be taken in layout to maintain isolation between analog and digital signal paths for proper noise consideration.
- 2) Power supply decoupling is necessary as close to the device as possible. A 0.1uf should be sufficient.
- 3) Ground, then power, must be present before any input signals are applied to the CVSD. Failure to observe this may cause a latchup condition which may be destructive. Latchup may be removed by cycling the power off/on. A power-up reset circuit may be used that strobes Force Zero (Pin 13) during power-up as follows:
- 4) Analog (signal) ground (Pin 2) should be externally tied to Pin 8 and power ground. It is recommended that the AIN and AOUT ground returns connect only to Pin 2.
- 5) Digital inputs and outputs are compatible with standard CMOS logic using the same supply voltage. All unused logic inputs must be tied to the appropriate logic level for desired operation. TTL outputs will require 1K Ohm pull-up resistors. Pins 4 and 14 will each drive CMOS logic or one low power TTL input.
- 6) Since the Audio Out pins are internally DC biased to $V_{DD}/2$, AC coupling is required. In general, a value of 0.1 μ f is sufficient for AC coupling of the CVSD audio pins to a filter circuit.
- 7) The AGC output may be externally integrated to drive an AGC pre-amp, or it could drive an LED indicator through a buffer to indicate proper speaking volume.



Figures 4, 5, and 6 illustrate the typical frequency response of the HC-55564 for varying input levels and for varying sampling rates. To prevent slope overload (slew limiting), the 0dB boundary should not be exceeded. The frequency response is directly proportional to the

sampling clock rate. The flat bandwidth at 0dB doubles for every 16kHz increase in sampling rate. The output levels were measured in the encode mode, without filtering, from A_{IN} to A_{OUT}, at V_{DD} = +5V. 0dB = 1.2Vrms.

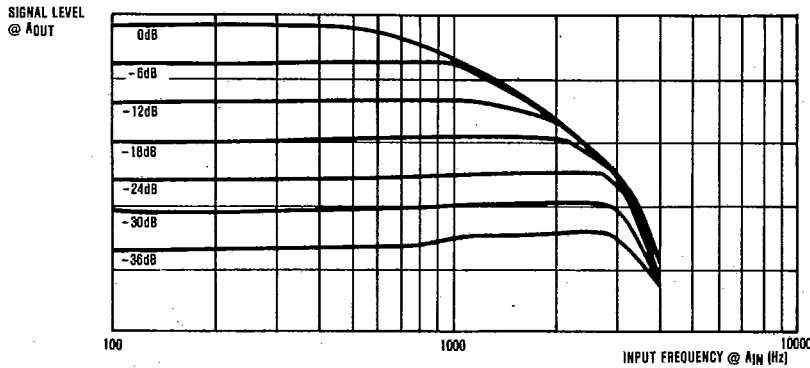


FIGURE 4. TRANSFER FUNCTION FOR CVSD AT 16Kbps

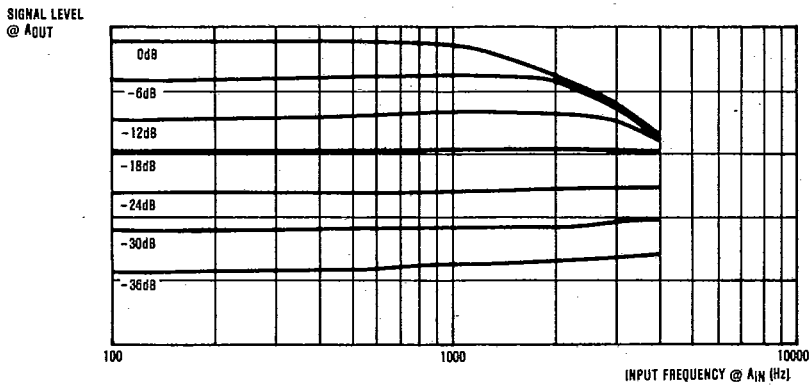


FIGURE 5. TRANSFER FUNCTION FOR CVSD AT 32Kbps

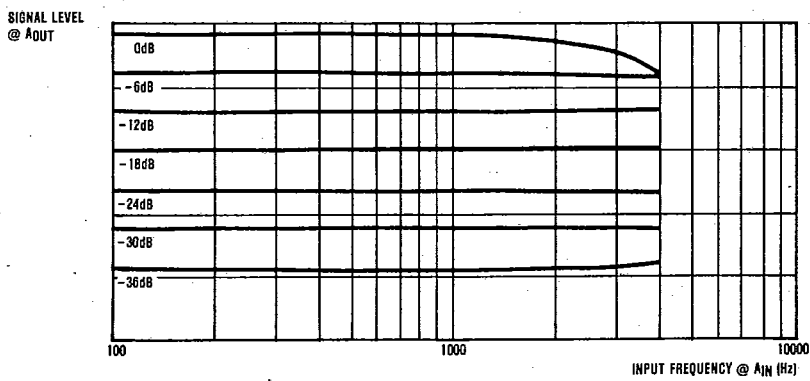


FIGURE 6. TRANSFER FUNCTION FOR CVSD AT 64Kbps

8
TELECOM-
MUNICATIONS

The following typical performance distortion graphs were realized with the test configuration of Figure 7. The measurement vehicle for Total Harmonic Distortion (THD) was an HP-339A distortion measurement set, and

for 2nd and 3rd harmonic distortion, an HP-3582A spectrum analyzer. All measurement conditions were at $V_{DD} = +5V$, and 2nd and 3rd harmonic distortion measurements were C-message filtered. $0dB = 1.2V_{rms}$.

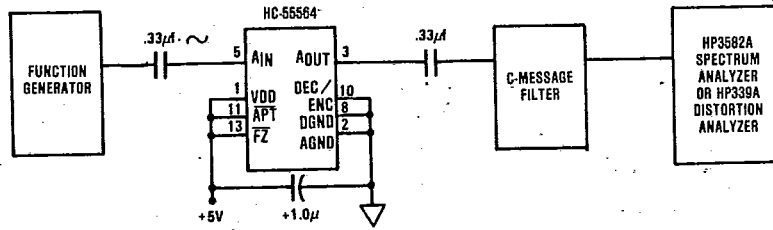


FIGURE 7. TEST AND MEASUREMENT CIRCUIT

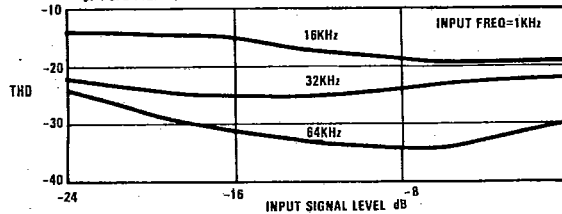


FIGURE 8. CVSD SIGNAL LEVEL VERSUS TOTAL HARMONIC DISTORTION

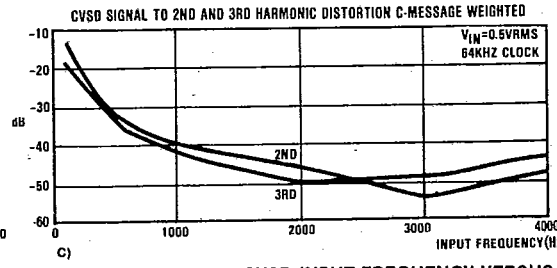
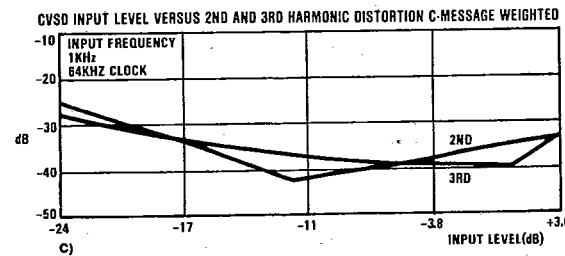
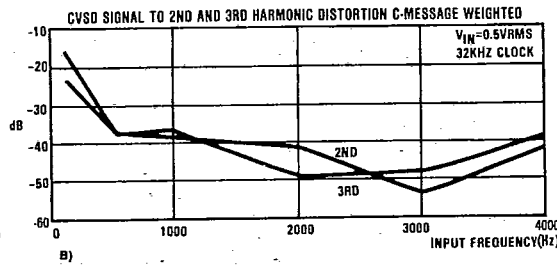
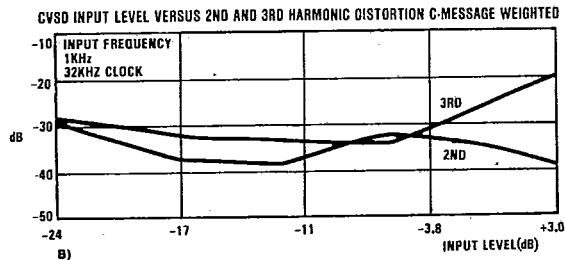
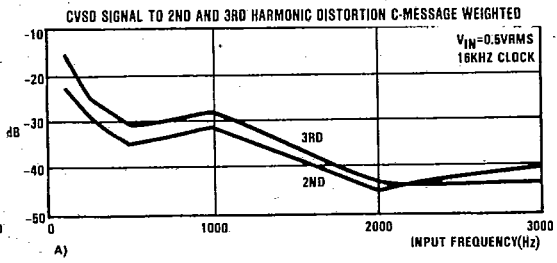
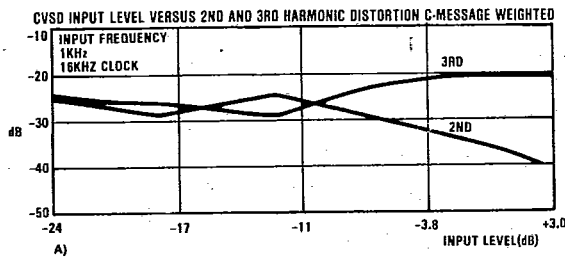


FIGURE 9A, B, C. CVSD INPUT LEVEL VERSUS 2ND AND 3RD HARMONIC DISTORTION

FIGURE 10A, B, C. CVSD INPUT FREQUENCY VERSUS 2ND AND 3RD HARMONIC DISTORTION