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FUJITSU

DATA SHEET

MB8441-45/-55
CMOS 64K-BIT DUAL PORT SRAM

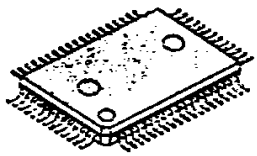
8K x 8-BIT CMOS DUAL PORT STATIC RANDOM ACCESS MEMORY

PRELIMINARY

The Fujitsu MB8441 is an 8K words x 8 bits dual-port high-performance Static Random Access Memory (SRAM) fabricated in CMOS. The SRAM uses asynchronous circuitry and no external clocks are required. The MB8441 provide the user with two separately controlled I/O ports with independent addresses, Chip Select ($\overline{CS}$), Write Enable ($\overline{WE}$), Output Enable ($\overline{OE}$), and I/O functions. This arrangement permits independent access to any memory location for either a Read or Write operation — a useful feature for shared data processing applications. These devices have an automatic power-down feature controlled by $\overline{CS}$. The MB8441 can be used as either a master operation or slave operation by selecting the $\overline{BE}$ pin.

To avoid data contention on the same address, a ($\overline{BUSY}$) flag is provided for address arbitration; In addition, the MB8441 utilizes an ($\overline{INT}$) flag which allows communication between systems on either side of the RAM. The MB8441 uses a single 5-volt power supply and all pins are TTL-compatible.

Some typical applications for these memory devices are multiprocessing systems, distributed networks, external register files, and peripheral controllers.



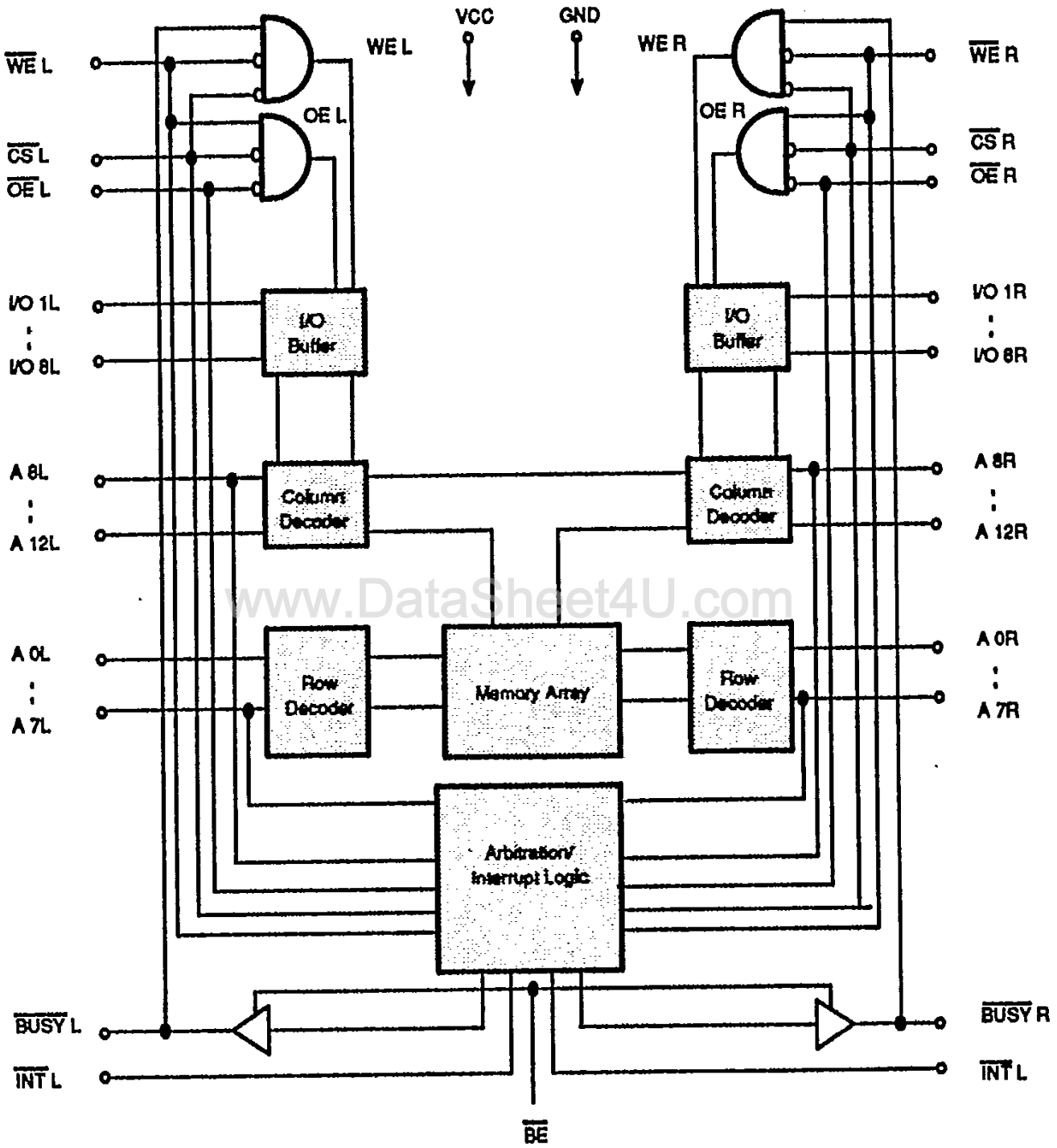
FPT-64P-M06

Features

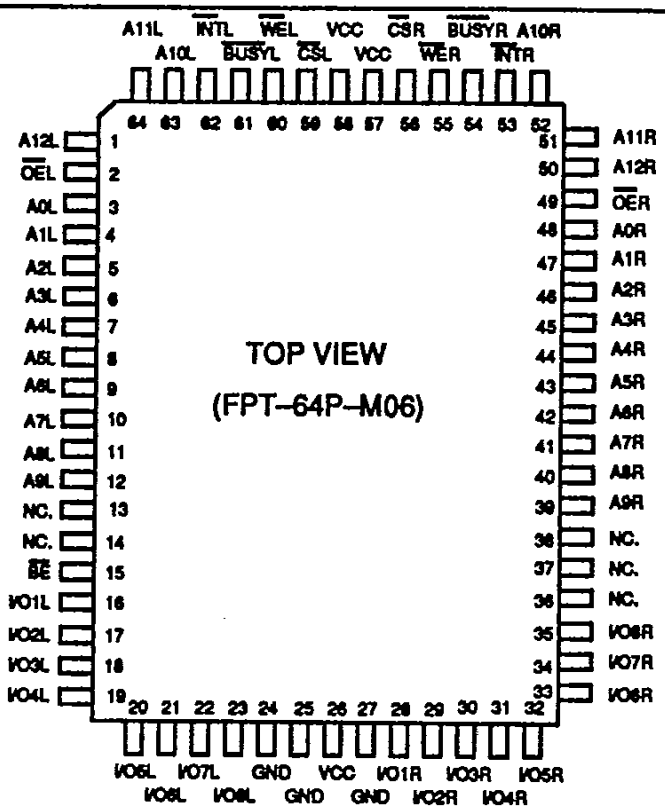
- Organization: 8,192 words x 8 bits.
- Static operation: No clocks or timing strobes required.
- Access Time: tAA = tACS = 45ns max. (MB8441-45)
  tAA = tACS = 55ns max. (MB8441-55)
- Power Consumption:
  Both ports active = 660 mW (max)
  Both ports standby
  CMOS = 1.1 mW (max)
  TTL = 27.5 mW (max)
- TTL-compatible inputs and outputs.
- Three-state outputs with Or-tie capability.
- Electrostatic protection for all inputs and outputs.
- Addres arbitration: ($\overline{BUSY}$) flag output (Master Operation: $\overline{BE}$ = "L")
  ($\overline{BUSY}$) flag output (Slave Operation: $\overline{BE}$ = "H")
- Interrupt function for communication between systems: $\overline{INT}$ flag.
- Data retention voltage: 2.0V min.
- Single +5V (±10%) supply.
- 64-pin plastic quad flat package

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig.1 – BLOCK DIAGRAM of MB8441



PIN ASSIGMENT



PIN DESCRIPTION

Symbol		I/O	Function
Left Port	Right Port		
$\overline{CS}$ L	$\overline{CS}$ R	I	Chip select
$\overline{WE}$ L	$\overline{WE}$ R	I	Write enable
$\overline{OE}$ L	$\overline{OE}$ R	I	Output enable
A 0L to A 12L	A 0R to A 12R	I	Address
I/O 1L to I/O 8L	I/O 1R to I/O 8R	I/O	Data input / output
$\overline{BUSY}$ L	$\overline{BUSY}$ R	I/O	BUSY flag ($\overline{BE}$ = "L" : output, $\overline{BE}$ = "H" : input)
$\overline{INT}$ L	$\overline{INT}$ R	O	Interrupt output
$\overline{BE}$		I	BUSY output enable (Selects a Master or a Slave.)
V CC		—	Supply voltage
GND		—	Ground
NC.		—	No connection

FUNCTION DESCRIPTION

The MB8441 provides two ports with separate control signals, address inputs, and input/output data pins that allow asynchronous read and write operation to any memory location. This device has an on-chip automatic power-down feature controlled by $\overline{CS}$ that places the respective port in the standby mode when the chip is deselected ($\overline{CS}$ is HIGH). When a port is enabled, access to the entire memory array is permitted. Each port has an independent Output Enable ($\overline{OE}$) control that is active in the read mode and enables the output drivers.

ARBITRATION LOGIC

1. Master busy function ($\overline{BE}$ = "L")

The arbitration logic resolves an address match or chip-enable match and determines the access priority. In both cases, an active $\overline{BUSY}$ flag is set for the port-in-waiting. Since both ports are asynchronous, there is the possibility of accessing the same memory location from both sides. In the read mode, this condition is not a problem. However, this is a problem when both ports are in the write mode with different data words or when one port is reading and the other is writing. When both ports access the same memory location, the on-chip arbitration logic determines which port has access and the $\overline{BUSY}$ flag for the delayed port is set active LOW and all operations on that port are inhibited.The delayed port can be accessed when the $\overline{BUSY}$ flag becomes inactive. Basic modes of abitration are described in subsequent paragraphs. (refer to timing diagram of "contention cycle".)

Access to delayed port is enabled as following, first set $\overline{BUSY}$ from "L" to "H" and then retain write mode ($\overline{CS}$ = $\overline{WE}$ = "L") during t_{BW}. $\overline{BUSY}$ signal dose not affect the read mode of delayed port normally. But in case that write operation is done from opposite port during $\overline{BUSY}$ signal output, read data may change. So it is recommended to read output data after t_{BD} passes from reset of $\overline{BUSY}$ signal.

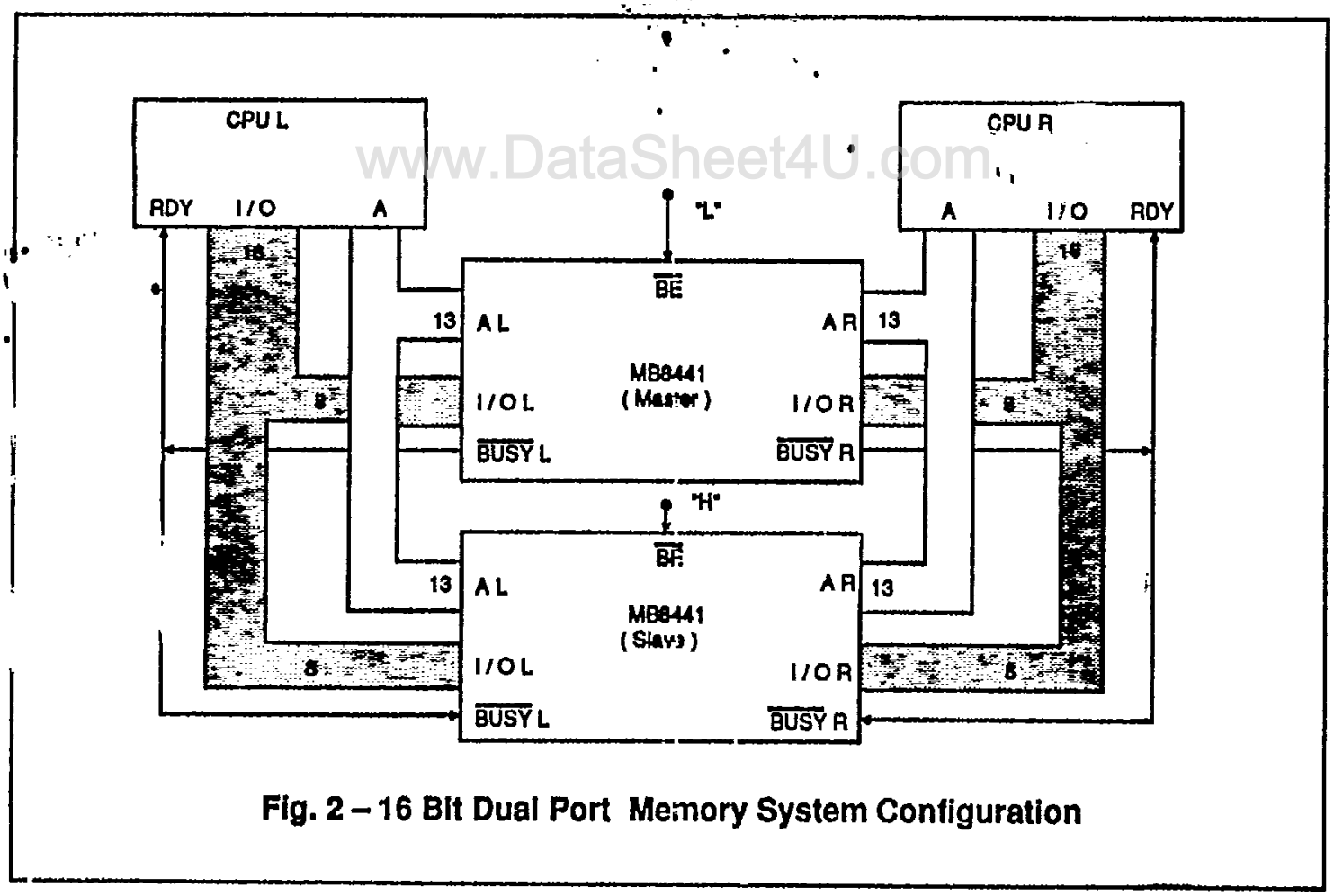


Fig. 2 – 16 Bit Dual Port Memory System Configuration

2. Slave busy function ($\overline{BE}$ = "H")

When the MB8441 is used with larger bit width than 8 bits, it is necessary to use more than two chips in paralell. In this case, each chip may output $\overline{BUSY}$ signal to other ports. It will be a problem if both CPU get $\overline{BUSY}$ signal. But the slave busy function can solve this problem. By this function, only the master chip operates the master busy function and the other chip obeys the master chip's $\overline{BUSY}$ signal. This function is operated by setting $\overline{BE}$ = "L" on one master chip and setting BE = "H" on the slave chips. By way of example, the composition of the 16 bit dual port memory system is showen in fig. 2.
In this system the master MB8441 with $\overline{BE}$ = "L" decides which port is first, and outputs the result to $\overline{BUSY}$ pin. This data is sent to the CPU and slave MB8441, then the CPU incurs the "wait" condition.

3. Interrupt function

The interrupt ($\overline{INT}$) function provides communication between systems on both sides of the dual-port RAM. $\overline{INT}$ is set to "L" when the processor on the right port writes to address 1FFE (A0 = "L" and A1–A12 = "H"). When the left port acknowledges by reading address 1FFE, $\overline{INT}$ is then reset to "H". In essence, address 1FFE serves as an 8-bit mailbox that transfers information from the right port to the left port. When $\overline{INTR}$ is set "L", the processor on the left port writes to address 1FFF (A0–A12="H"). When the right port acknowledges by reading address 1FFF, $\overline{INTR}$ is then reset to "H". Hence, address 1FFF serves as a second 8-bit mailbox, transferring information from the left port to the right port.

ABSOLUTE MAXIMUM RATINGS

(All voltages are referenced to GND.)

Parameter	Symbol	Value	Unit
Supply Voltage	V CC	– 0.5 to + 7.0	V
Input Voltage on any pin	V IN	– 0.5 to V CC + 0.5	V
Output Voltage on any pin	V I/O	– 0.5 to V CC + 0.5	V
Output Current	I OUT	± 20	mA
Temperature under Bias	T A	– 10 to + 85	°C
Storage Temperature	T STG	– 40 to + 125	°C
Power Dissipation	P D	1.0	W

Note ;
Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

RECOMMENDED OPERATING CONDITIONS

(All voltages are referenced to GND.)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V CC	4.5	5.0	5.5	V
Supply Voltage	GND	——	0	——	V
Operating Temperature	T A	0	——	+ 70	°C

FUNCTION TABLE

1. BASIC FUNCTION (A 0L to A12 L = A 0 R to A12 R)

Left Port Input			Right Port Input			Function	Supply Current
$\overline{CS}$ L	$\overline{WE}$ L	$\overline{OE}$ L	$\overline{CS}$ R	$\overline{WE}$ R	$\overline{OE}$ R		
H	X	X	X	X	X	Left port standby	Standby
L	H	H	X	X	X	Left port output disable	Active
L	H	L	X	X	X	Left port read	Active
L	L	X	X	X	X	Left port write	Active
X	X	X	H	X	X	Right port standby	Standby
X	X	X	L	H	H	Right port output disable	Active
X	X	X	L	H	L	Right port read	Active
X	X	X	L	L	X	Right port write	Active

NOTES: X = Don't Care, L = Low, H = High

2. ARBITRATION FUNCTION (A 0 L to A12 L = A 0 R to A12 R)

$\overline{BE}$		Left Port Input			Right Port Input			Function
		$\overline{CS}$ L	A 0L to A12 L	$\overline{BUSY}$ L	$\overline{CS}$ R	A 0 R to A12 R	$\overline{BUSY}$ R	
Master	L	L	VBR	H	L	Valid	L	Left operation permitted Right operation not permitted
	L	LBR	Match	H	L	Match	L	
	L	L	Valid	L	L	VBL	H	Right operation permitted Left operation not permitted
	L	L	Match	L	LBL	Match	H	
	L	L	VST	*	L	VST	*	*
	L	LST	Match		LST	Match		
Slave	H	L	X	H	L	X	L	Left operation permittde Right operation not permitted
	H	L	X	L	L	X	H	Right operation permitted Left operation not permitted

X = Don't Care, L = Low, H = High, VBR = Valid Before Right, VBL = Valid Before Left, LBR = Low Before Right, LBL = Low Before Left, VST = Valid Same Time, LST = Low Same Time

* In case that t APS (min.) is not satisfied, the on-chip arbitration logic decides which port has access. And the busy flag for the delayed port is set "L" and all operations on that port are inhibited. But it is undefined which port has access or not. (Refer to timing diagram)

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

Parameter		Symbol	Min	Typ.	Max	Unit	Condition
Operating Supply Current (Both Port Active)		I CC	—	—	120	mA	Cycle = min. Duty = 100%, I OUT = 0 mA
Standby Supply Current		I SB1	—	—	5	mA	Both ports at Standby ; $\overline{CSL}$ & $\overline{CSR}$ = V IH
		I SB2	—	—	70	mA	One port at Standby ; $\overline{CSL}$ or $\overline{CSR}$ = V IH, I OUT = 0 mA
		I SB3	—	—	0.2	mA	Both ports at Full Standby ; $\overline{CSL}$ & $\overline{CSR}$ ≥ VCC – 0.2 V $\overline{BE}$ ≥ VCC – 0.2 V or $\overline{BE}$ ≤ GND + 0.2 V
		I SB4	—	—	70	mA	One port at Full Standby ; $\overline{CSL}$ or $\overline{CSR}$ ≥ V CC – 0.2 V, I OUT = 0 mA
Input Leakage Current		I LI	–10	—	10	µA	V IN = GND to V CC
Output Leakage Current		I LO	–10	—	10	µA	$\overline{CS}$ = V IH, V OUT = GND to V CC
Input High Voltage		V IH	2.2	—	V CC + 0.3	V	——
Input Low Voltage		V IL	–0.5*1	—	0.8	V	——
Output High Voltage		V OH	2.4	—	—	V	I OH = –1.0 mA*2
Output Low Voltage	DOUT	V OL	—	—	0.4	V	I OL = 3.2 mA
	$\overline{BUSY}$ $\overline{INT}$		—	—	0.4	V	I OL = 8.0 mA

*1 –0.3 V Min. for pulse width less than 20 ns.

*2 The $\overline{BUSY}$ and $\overline{INT}$ pins require pull–up resistors because they are open–drain outputs.

I/O CAPACITANCE (TA = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Capacitance (VIN = 0V)	C IN	——	——	10	pF
I / O Capacitance (V I/O = 0V)	C I/O	——	——	10	pF

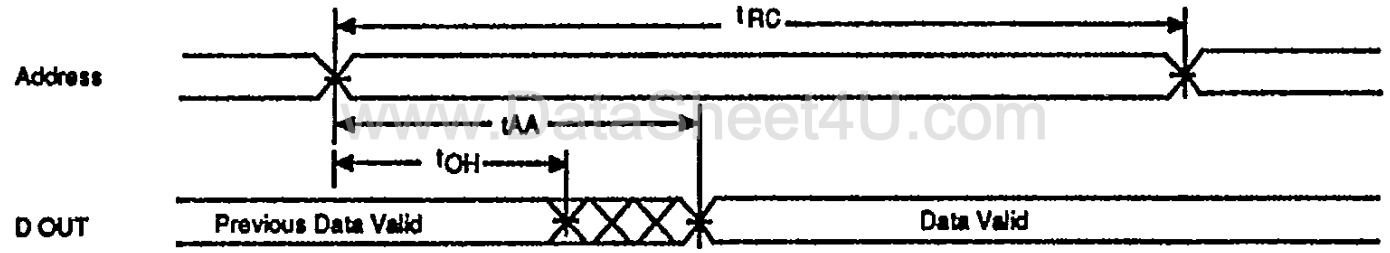
AC CHARACTERISTICS

READ CYCLE (Recommended operating conditions unless otherwisw noted.)

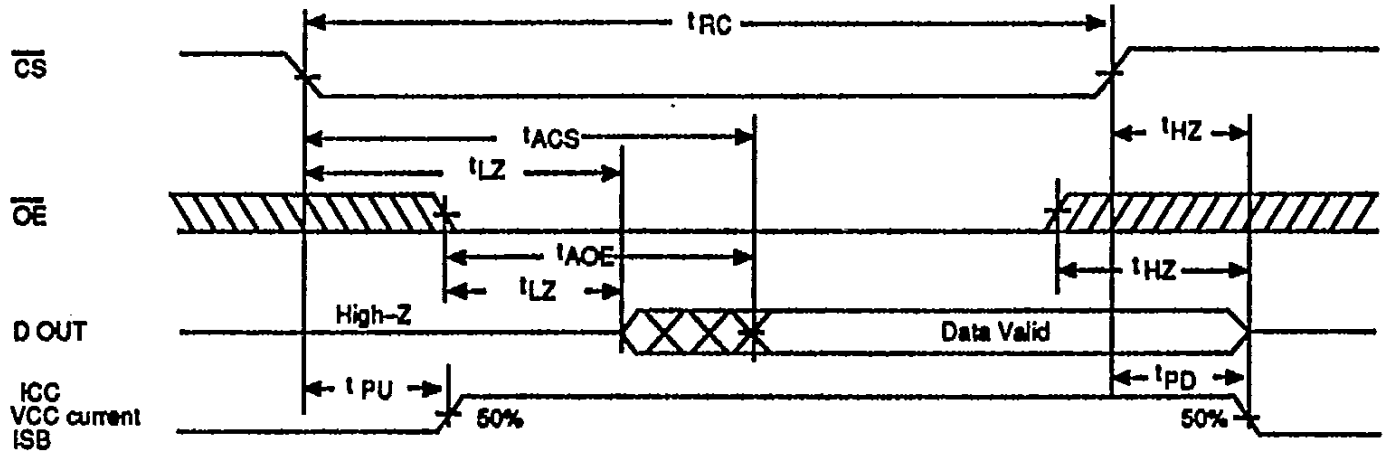
Parameter	Symbol	MB8441-45			MB8441-55			Unit
		Min	Typ.	Max	Min	Typ.	Max	
Read Cycle Time	tRC	45	—	—	55	—	—	ns
Address Access Time	tAA	—	—	45	—	—	55	ns
$\overline{CS}$ Access Time	tACS	—	—	45	—	—	55	ns
$\overline{OE}$ Access Time	tAOE	—	—	25	—	—	30	ns
Output Hold Time	tOH	3	—	—	3	—	—	ns
$\overline{CS}$ to Output Low-Z *1	tCLZ	3	—	—	3	—	—	ns
$\overline{OE}$ to Output Low-Z *1	tOLZ	3	—	—	3	—	—	ns
$\overline{CS}$ to Output High-Z *1	tCHZ	—	—	25	—	—	25	ns
$\overline{OE}$ to Output High-Z *1	tOHZ	—	—	25	—	—	30	ns
Power Up Time	tPU	0	—	—	0	—	—	ns
Power Down Time	tPD	—	—	30	—	—	40	ns

READ CYCLE TIMING DIAGRAMS ($\overline{WE}$ = V IH)

Read Cycle No. 1 (Address controlled) ($\overline{CS}$ = $\overline{OE}$ =V IL)



Read Cycle No. 2 ($\overline{CS}$ controlled) *2



Legend : Undefined Don't care

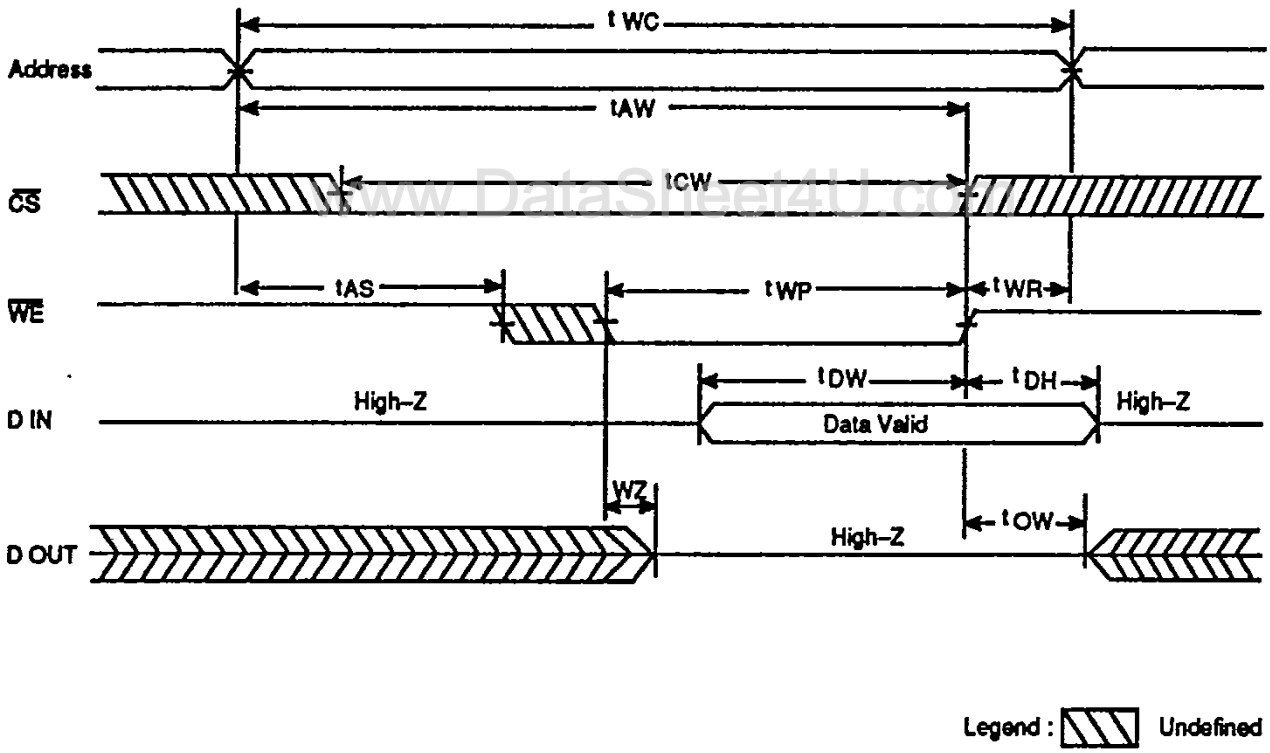
*1 :Transition is measured at the point of ± 500 mV from a steady state voltage with CL = 5 pF.
*2 : Address should be fixed before high-to-low transfer of $\overline{CS}$.

WRITE CYCLE
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8441-45			MB8441-55			Unit
		Min	Typ.	Max	Min	Typ.	Max	
Write Cycle Time	tWC	45	—	—	55	—	—	ns
Address Valid to End of Write	tAW	40	—	—	50	—	—	ns
Chip Select to End of Write	tCW	40	—	—	50	—	—	ns
Address Setup Time	tAS	0	—	—	0	—	—	ns
Write Pulse Width	tWP	25	—	—	35	—	—	ns
Write Recovery Time	tWR	0	—	—	0	—	—	ns
Data Setup Time	tDW	20	—	—	25	—	—	ns
Data Hold Time	tDH	0	—	—	0	—	—	ns
$\overline{WE}$ to Output Low-Z *1	tOW	0	—	—	0	—	—	ns
$\overline{WE}$ to Output High-Z*1	tWZ	20	—	—	30	—	—	ns

WRITE CYCLE TIMING DIAGRAMS

Write Cycle No. 1 ($\overline{WE}$ Controlled) *2 *3 *4



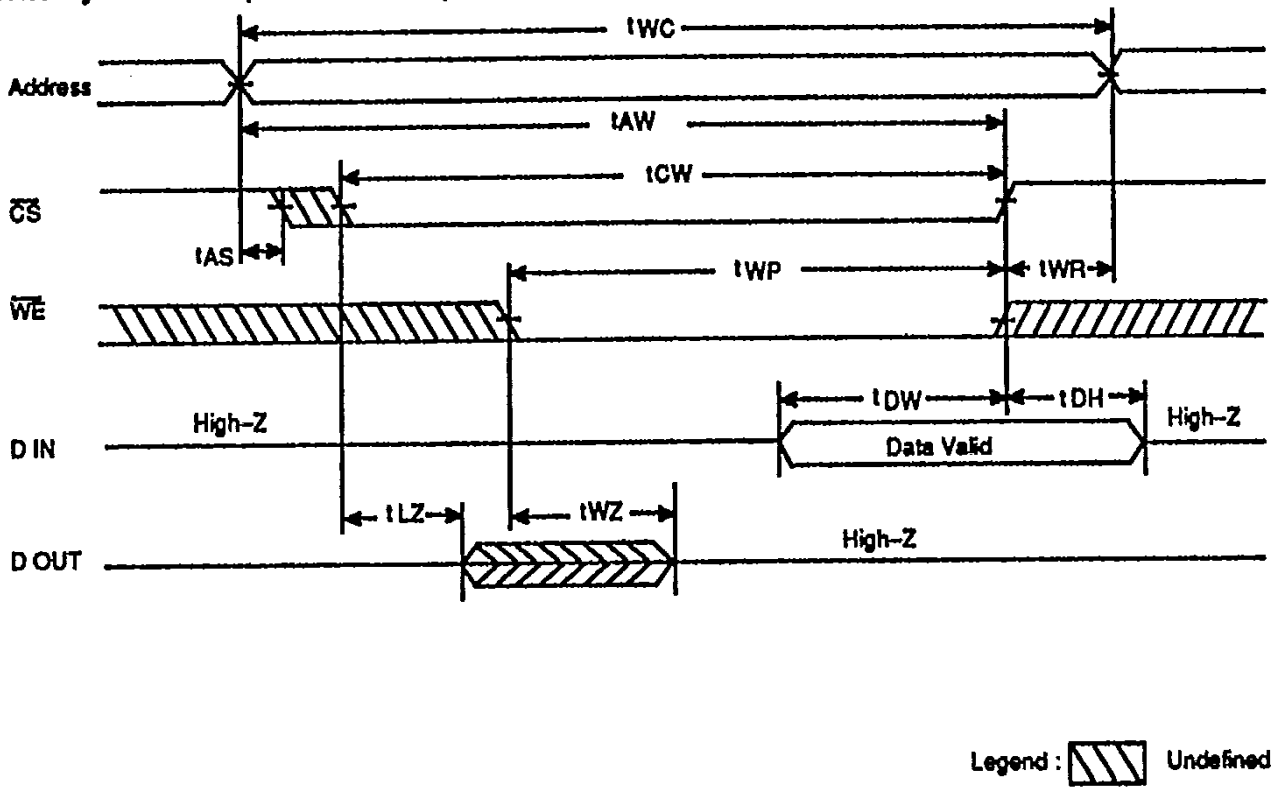
*1 : Transition is measured at the point of ± 500 mV from a steady state voltage with CL = 5 pF.

*2 : WE must be high during address transition.

*3 : If $\overline{OE}$ and $\overline{CS}$ are in the READ Mode, I/O pins are in the output state so that the input signals of the opposite phase to the output must not be applied.

*4 : If $\overline{CS}$ goes high prior to, or coincidently with, $\overline{WE}$ transition to high, the output remains in high impedance state.

Write Cycle No. 2 ($\overline{CS}$ Controlled) *1 *2 *3



*1 : $\overline{WE}$ must be high during address transition.
*2 : If $\overline{OE}$ and $\overline{CS}$ are in the READ Mode, then I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
*3 : If $\overline{CS}$ goes high prior to, or coincidently with, $\overline{WE}$ transition to high, the output remains in high impedance state.

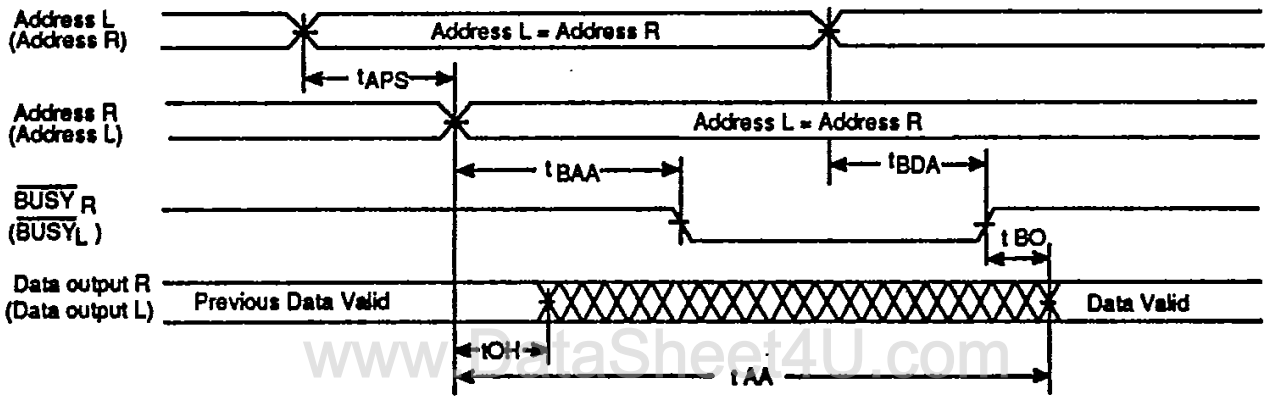
BUSY TIMING ($\overline{BE}$ = "L" ; Master Function)

(Recommended operating conditions unless otherwise noted.)

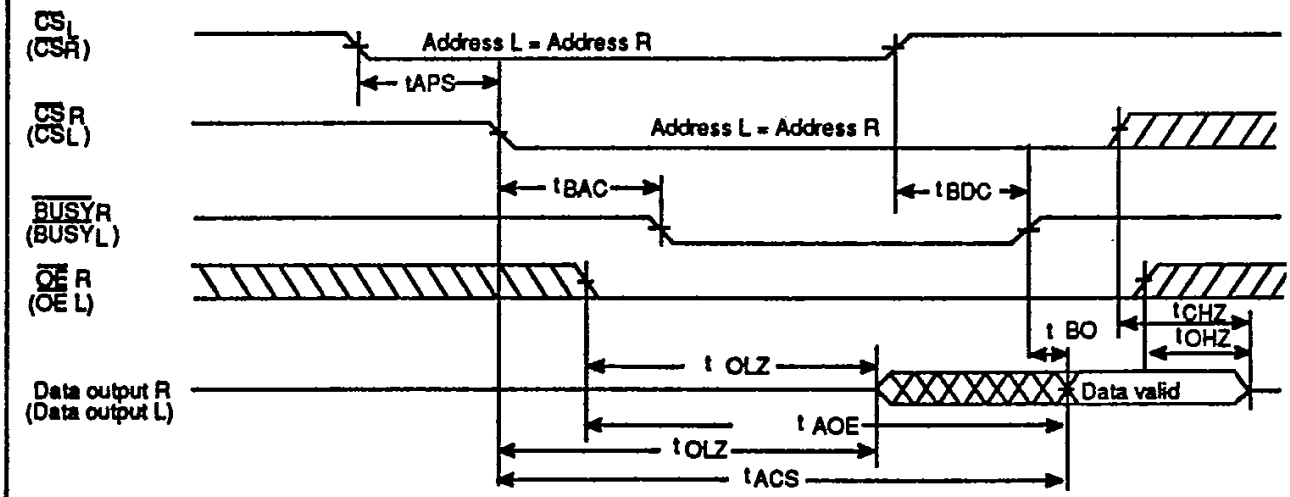
Parameter	Symbol	MB8441-45			MB8441-55			Unit
		Min	Typ.	Max	Min	Typ.	Max	
$\overline{BUSY}$ Access Time from Address	t BAA	—	—	30	—	—	30	ns
$\overline{BUSY}$ Access Time from $\overline{CS}$	t BAC	—	—	30	—	—	30	ns
$\overline{BUSY}$ Output High–Z from Address	t BDA	—	—	30	—	—	30	ns
$\overline{BUSY}$ Output High–Z from $\overline{CS}$	t BDC	—	—	30	—	—	30	ns
Arbitration Priority Setup Time	t APS	5	—	—	5	—	—	ns
Data Output Access Time from $\overline{BUSY}$	t BO	—	—	0	—	—	0	ns
Write Hold Time from $\overline{BUSY}$	t BW	25	—	—	35	—	—	ns

CONTENTION READ CYCLE TIMING DIAGRAMS ($\overline{WE}$ = V IH) ($\overline{BE}$ = V IL : Master Function)

Data Contention Cycle No. 1 (Address Controlled) ($\overline{CS}$ = $\overline{OE}$ = VIL)*1 *2



Data Contention Cycle No. 2 ($\overline{CS}$ Controlled) *1 *3

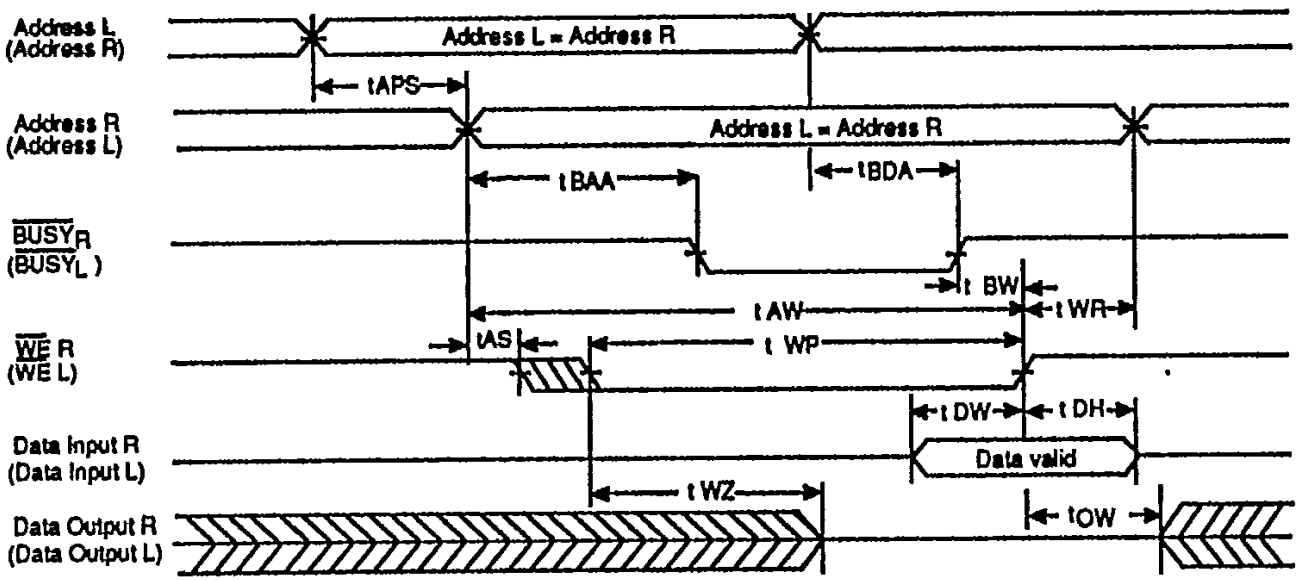


Legend : Undefined Don't care

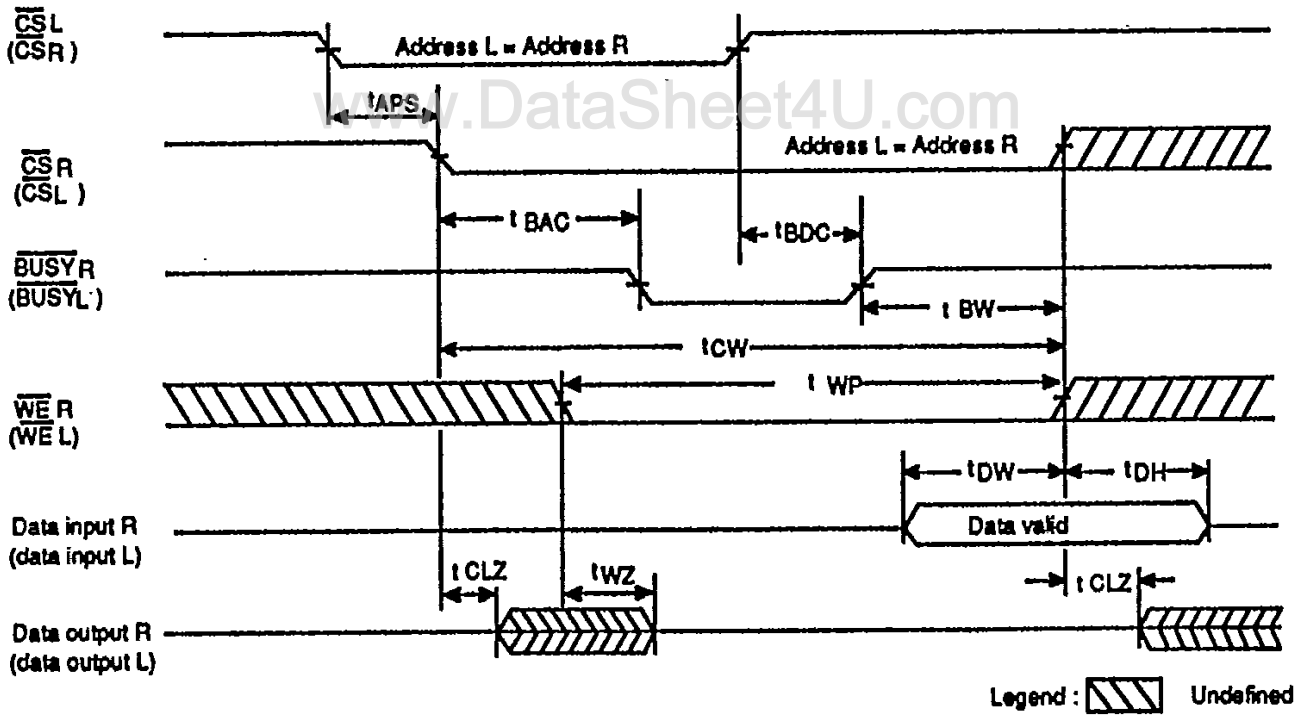
- *1 : In case of dual access at the same memory location, the port that accesses the RAM first sets the $\overline{BUSY}$ flag high.
- *2 : $\overline{CS}$ must be low before, or coincide with, transition of address.
- *3 : Address is valid prior to, or coincidently with, high-to-low transition of $\overline{CS}$.

CONTENTION WRITE CYCLE TIMING DIAGRAMS ($\overline{BE}$ = V IL : Master Function)

Contention Write Cycle No.1 ($\overline{WE}$ Controlled) *1 *2 *3 *4



Contention Write Cycle No.2 ($\overline{CS}$ Controlled) *1 *2 *3 *4 *5



*1 : $\overline{WE}$ must be high during address transition.

*2 : If $\overline{OE}$ and $\overline{CS}$ are in the READ Mode, then I/O pins are in the output state, and the input signals of opposite phase to the outputs must not be applied.

*3 : In case of dual access at the same memory location, the port that accesses the RAM first sets the $\overline{BUSY}$ flag high.

*4 : $\overline{CS}$ must be low before, or coincide with, transition of $\overline{CS}$.

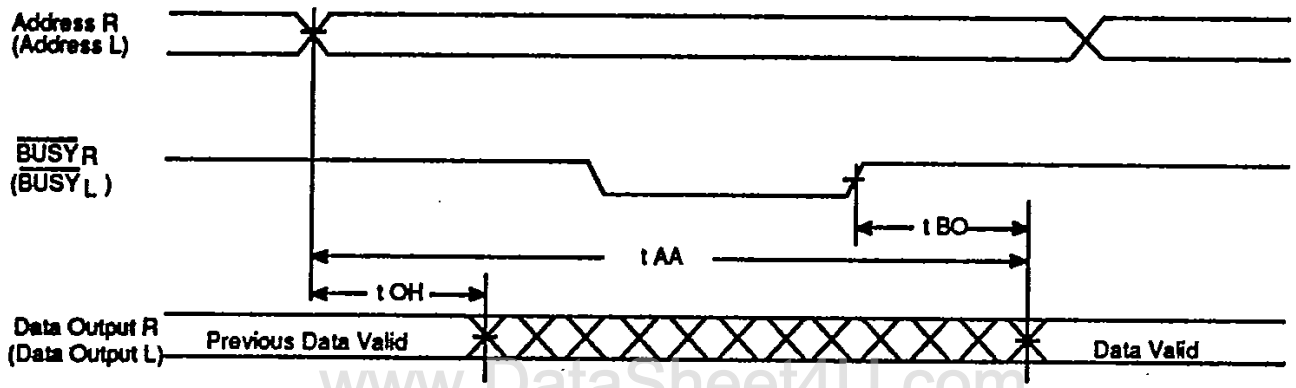
*5 : If $\overline{CS}$ goes high prior to, or coincidently with, $\overline{WE}$ transition to high, the output remains in high impedance.

BUSY TIMING ($\overline{BE}$ = "H" ; Slave Function)
(Recommended operating conditions unless otherwise noted.)

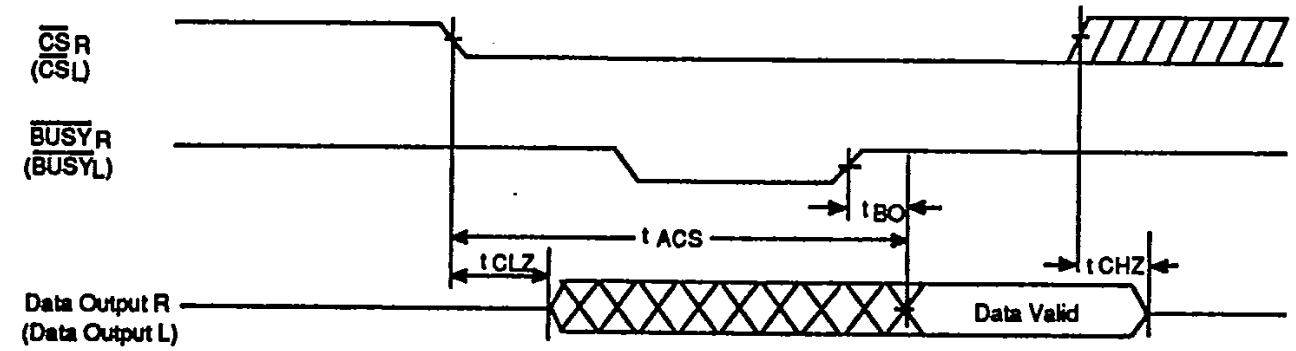
Parameter	Symbol	MB8441-45			MB8441-55			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Data Output Access Time from $\overline{BUSY}$	t BO	—	—	0	—	—	0	ns
Write Setup Time to $\overline{BUSY}$ *1	t WS	−10	—	—	−10	—	—	ns
Write Hold Time from $\overline{BUSY}$	t WH	25	—	—	35	—	—	ns

CONTENTION READ CYCLE TIMING DIAGRAMS ($\overline{WE}$ = V IH , $\overline{BE}$ = VIH : Slave Function)

Contention Read Cycle No.1 (Address controlled) ($\overline{CE}$ = $\overline{OE}$ = V IL) *2



Contention Read Cycle No.2 ($\overline{CS}$ controlled) *2



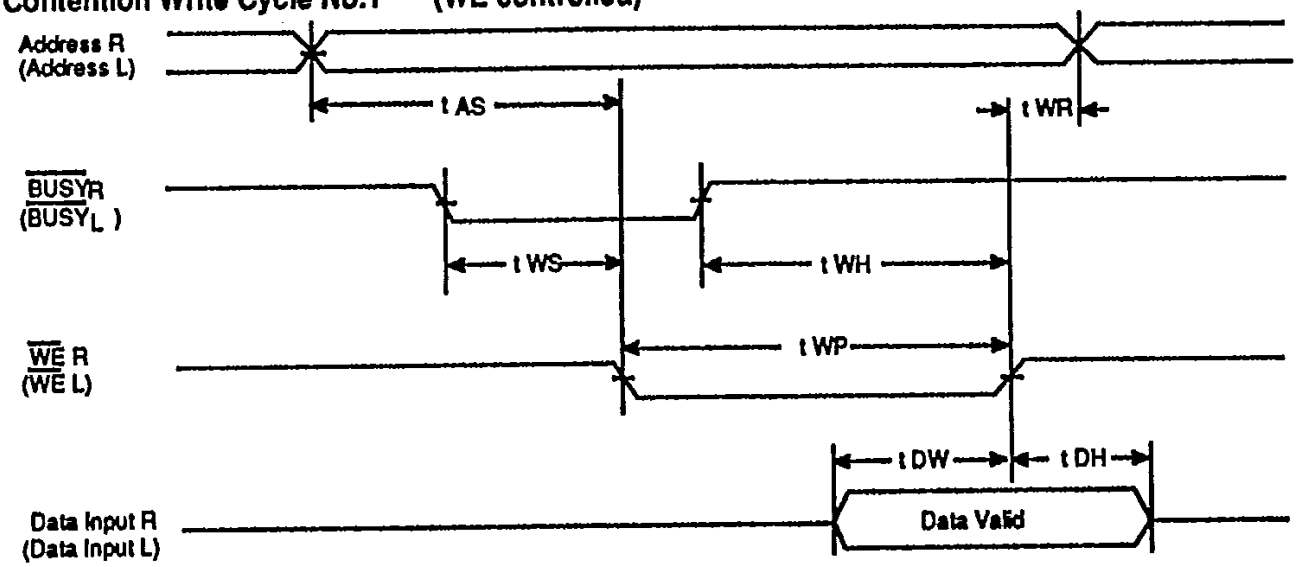
Legend : Undefined Don't care

*1 : It takes 30 ns to output $\overline{BUSY}$ signal from the master side, and so, the tAS (address set up time) of the slave side must be 20 ns or more.

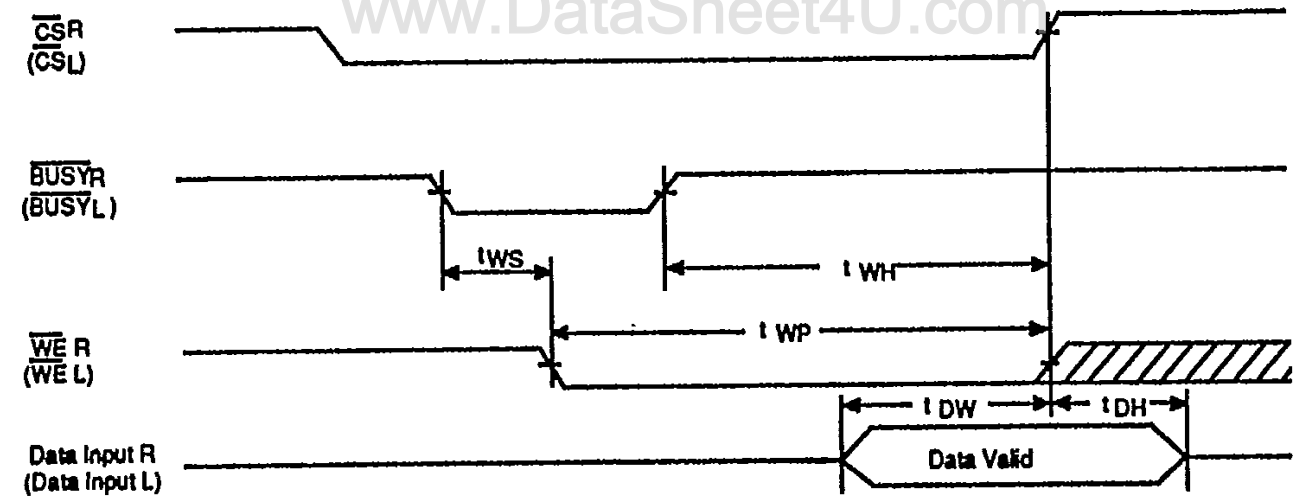
*2 : $\overline{CS}$ must be low before, or coincide with, transition of address.

CONTENTION WRITE CYCLE TIMING DIAGRAMS ($\overline{BE}$ = V IH : Slave Function)

Contention Write Cycle No.1 ($\overline{WE}$ controlled) *1 *2 *3 *4



Contention Write Cycle No.2 ($\overline{CS}$ controlled) *1 *2 *3 *4



Legend : Undefined

*1 : $\overline{WE}$ must be high during address transition.
*2 : I/O pins are in the output state, so the input signals of opposite phase must not be applied.
*3 : $\overline{CS}$ must be low before, or coincide with, transition of address.
*4 : During $\overline{BUSY}$ input is low, write operation can not be excuted even if $\overline{WE}$ is low.

INTERRUPT TIMING
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MB8441-45			MB8441-55			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
$\overline{INT}$ Set Time	t_{INS}	—	—	45	—	—	55	ns
$\overline{INT}$ Reset Time	t_{INR}	—	—	45	—	—	55	ns

INTERRUPT CYCLE TIMING DIAGRAMS

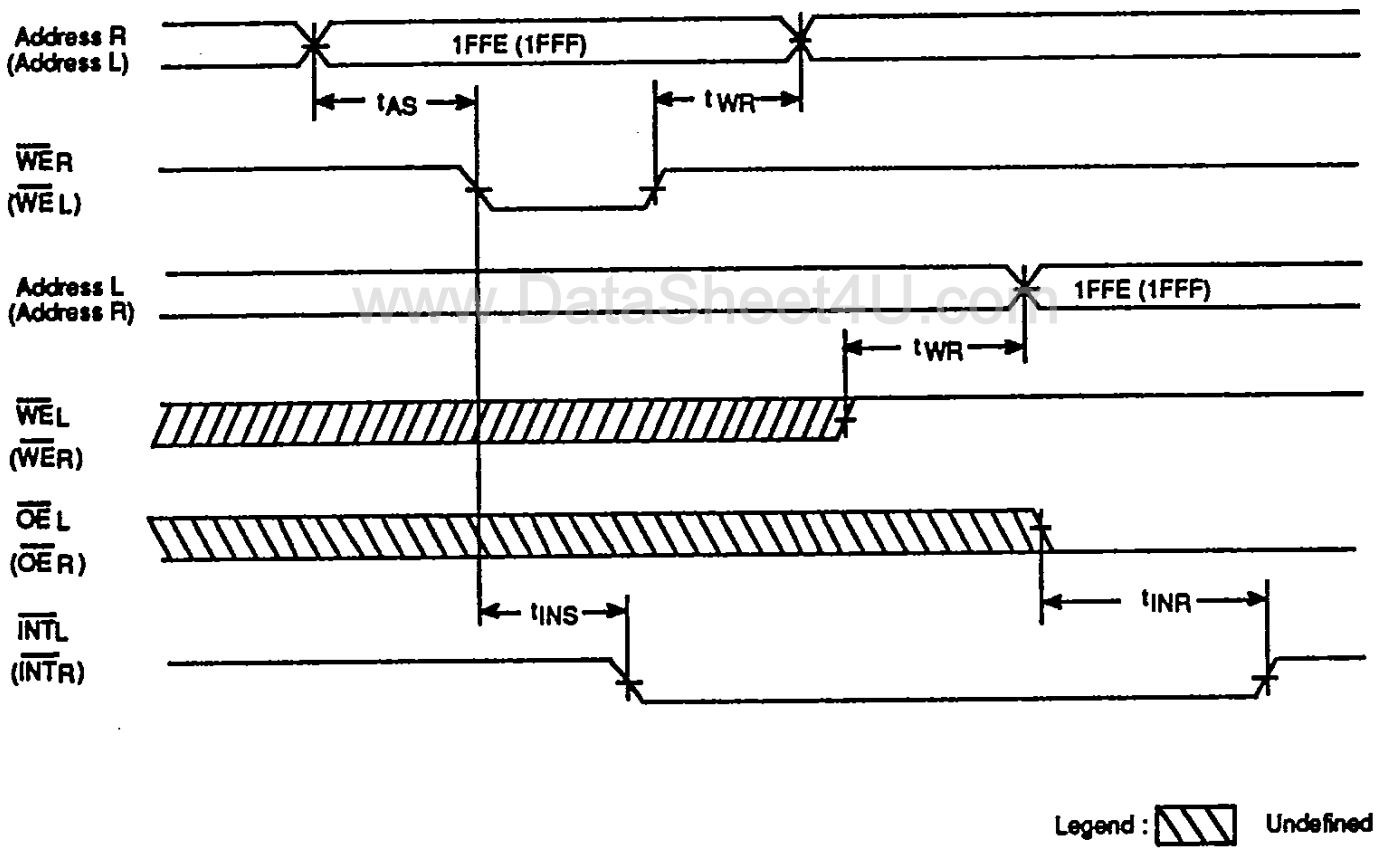
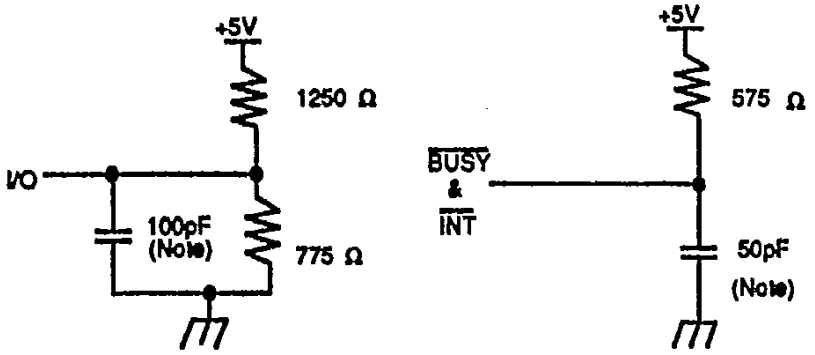


Fig.3 – AC Test Conditions

- Input Pulse Levels : 0 to 3.0 V
- Input Pulse Rise and Fall Times : t R = t F = 5 ns
- Timing Reference Levels : 1.5 V
- Output Loads



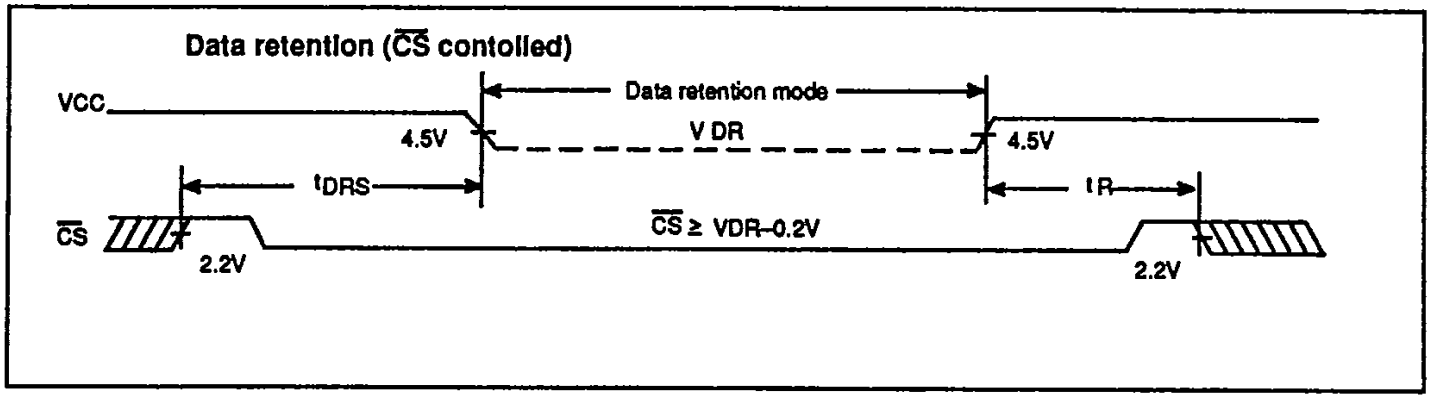
Note : Includes jig and stray capacitance

DATA RETENTION CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit	Condition
Data Retention Supply Voltage	VDR	2.0	5.5	V	
Data Retention Supply Current	IDR	—	0.02	mA	V CC = V DR = 3V $\overline{CSL}$ & $\overline{CSR}$ ≥ V CC – 0.2V, $\overline{BE}$ ≥ VCC – 0.2 V or $\overline{BE}$ ≤ GND + 0.2 V
Data Retention Setup Time	t_{DRS}	0	—	ns	
Operation Recovery Time	t_R	t_{RC}	—	ns	

DATA RETENTION TIMING

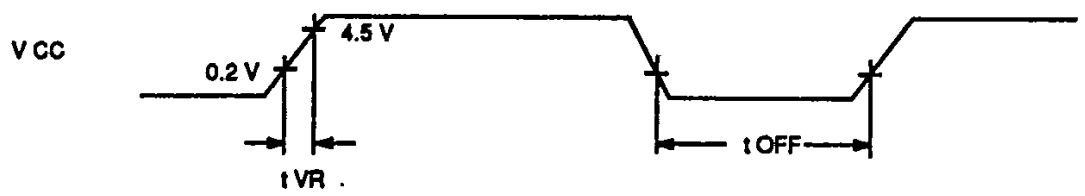


POWER ON/RESET CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit
Rising Time of Supply Voltage*1	t VR	0.05	50	ms
Power Off Time	t OFF	1	—	s

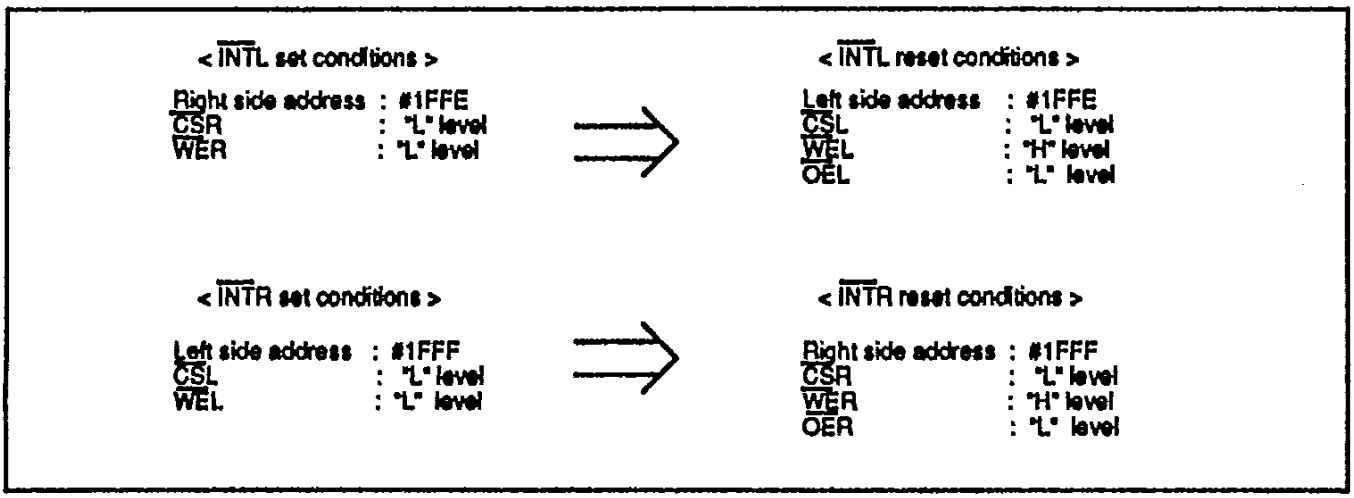
POWER ON/RESET TIMING



Note : Rise power slowly

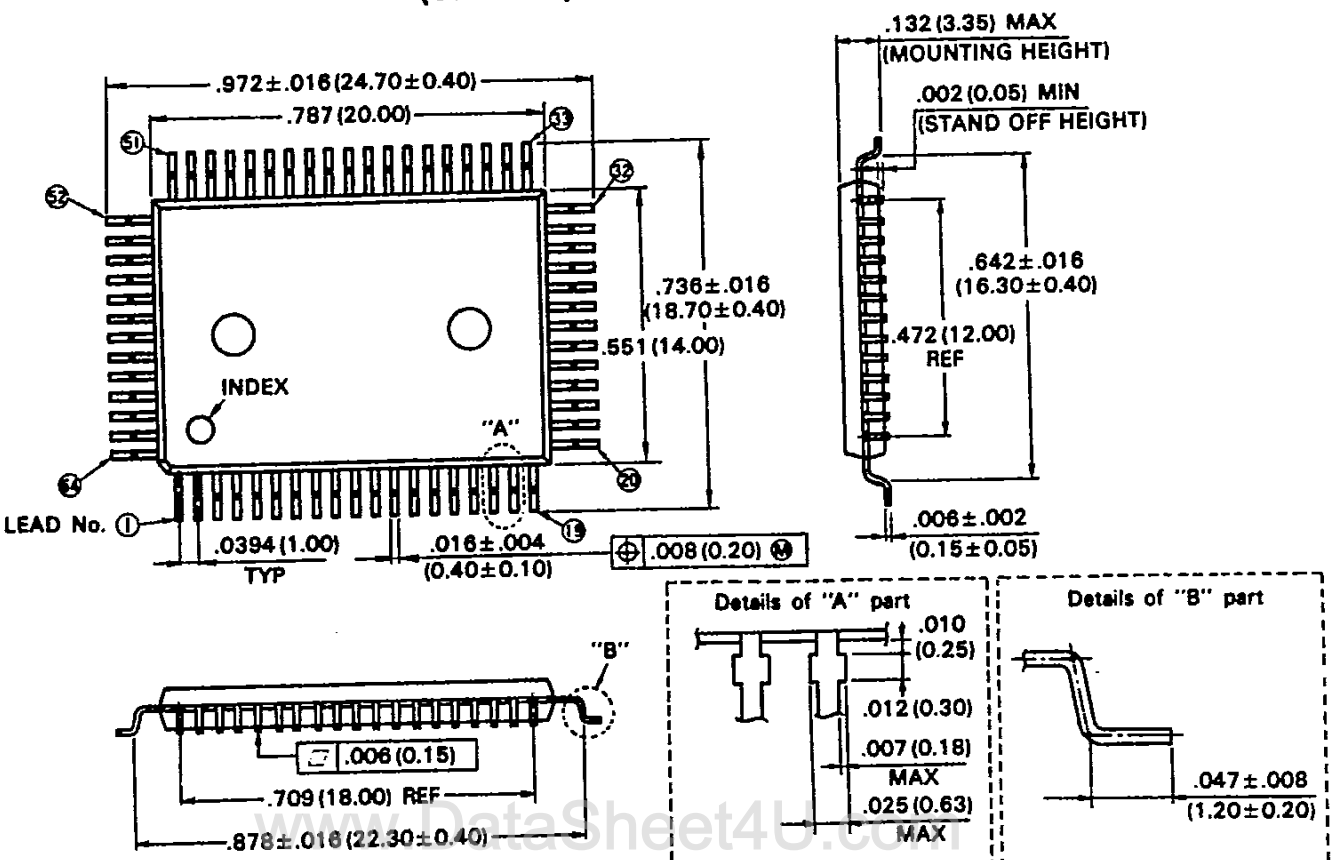
Note;

*1 : This is required to keep normal operation for the power on/reset circuit which initialize $\overline{INT}$ output to "H" automatically when Vcc is applied. In order to operate power-on-reset circuit normally, input conditions to set $\overline{INT}$ (refer to below) must not be applied during tVR period. And when input conditions are undefined during tvR period, $\overline{INT}$ may be set. So it is necessary to reset with a dummy read (refer to below).



PACKAGE DIMENSIONS

64-LEAD PLASTIC FLAT PACKAGE
(Case No. ; FPT-64P-M06)



Dimensions in
inches (millimeters)