SY58626L

DC-to-6.4Gbps Backplane Transmit Buffer with Selectable Output Pre-emphasis, I/O DC-Offset Control, and 200mV-3.0V$_{PP}$ Output Swing

General Description

The SY58626L high-speed, low jitter transmit buffer is optimized for backplane and transmission line data-path management applications in Automatic Test Equipment (ATE) and Test & Measurement (T&M) systems. The buffer includes a CML compatible, variable swing output with selectable pre-emphasis. The SY58626L is capable of driving serial data from DC through 6.4Gbps with a 3V$_{PP}$ (1.5V$_{PK}$ single ended) differential swing.

The SY58626L differential input includes Micrel's unique, 3-pin input termination architecture that directly interfaces to any DC- or AC-coupled, differential signal as small as 100mV$_{PK}$ without any termination resistor networks in the signal path. The outputs are 50Ω source-terminated CML with a programmable output swing from 200mV$_{PP}$ to 3V$_{PP}$ (100mV$_{PK}$ to 1.5V$_{PK}$).

The SY58626L includes an output stage that provides 4 levels of pre-emphasis. The output pre-emphasis level is programmed with a three-bit interface. Unlike other transmitter solutions, the output pre-emphasis duration can be programmed from 60ps to 400ps.

The SY58626L operates at 3.3V ±10% supply and is guaranteed over the commercial temperature range of 0°C to +70°C. The SY58626L transmitter is optimized to work with the SY58627L receiver. The SY58626L is part of Micrel's high-speed, Precision Edge® product line. Data sheets and support documentation can be found on Micrel's website at: www.micrel.com.

Precision Edge®

Features

- Transmit driver provides output pre-emphasis to extend transmission range
- 4 selectable pre-emphasis levels
- Drives 6.4Gbps up to 12″ FR4 PCB trace, or longer combinations of FR4+cable+interconnect
- DC through 6.4Gbps data rate throughput
- Integrated loopback capability
- Unique pre-emphasis:
  - Programmable pre-emphasis magnitude
  - Programmable pre-emphasis duration
- Unique, flexible I/O:
  - Internal termination to VTTIN pin interfaces to any differential AC- or DC-coupled signals
  - 50Ω source terminated CML outputs minimize round-trip reflections
  - Programmable output swing control: 200mV-3.0V$_{PP}$
  - Output Disable and output shutdown
  - DC-offset control with VTT I/O
- 3.3V ±10% supply voltage
- 0°C to +70°C temperature range
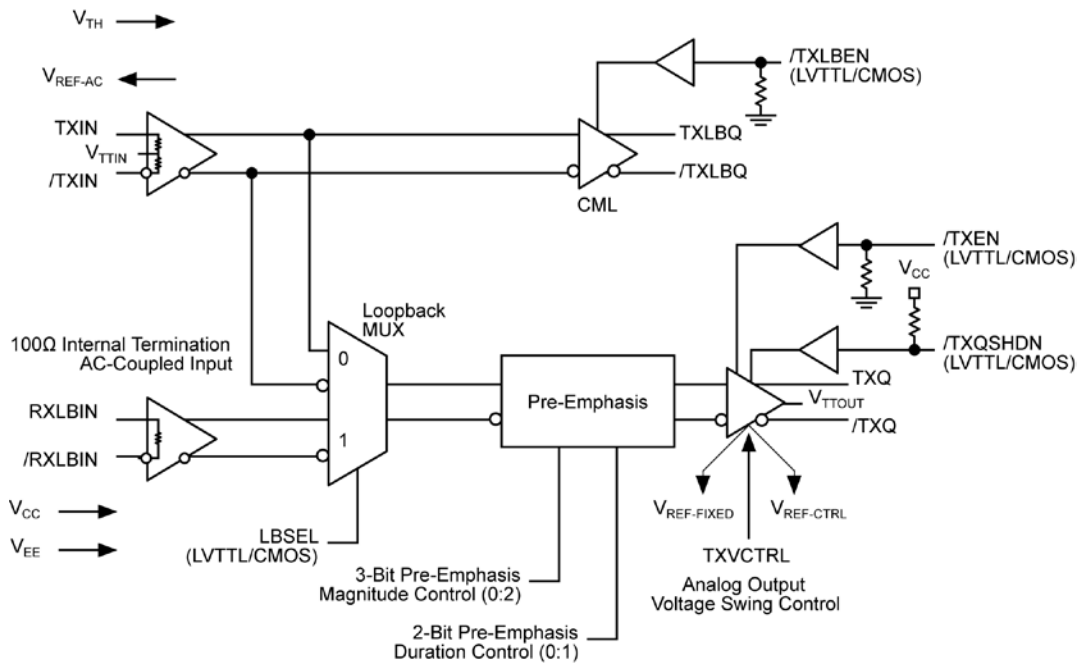- Available in 32-pin (5mm x 5mm) QFN package

Applications

- ATE, T&M backplane management
- Combination FR4+cable+interconnect driver
- Cable drivers
- Electrical interface and interconnect applications that require DC-offset control

Functional Block Diagram

Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY58626LMH	QFN-32	Commercial	SY58626L with bar-line Pb-Free indicator	NiPdAu Pb-Free
SY58626LMHTR[2]	QFN-32	Commercial	SY58626L with bar-line Pb-Free indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at $T_A = 25°C$, DC Electricals only.
2. Tape and Reel.

Pin Configuration
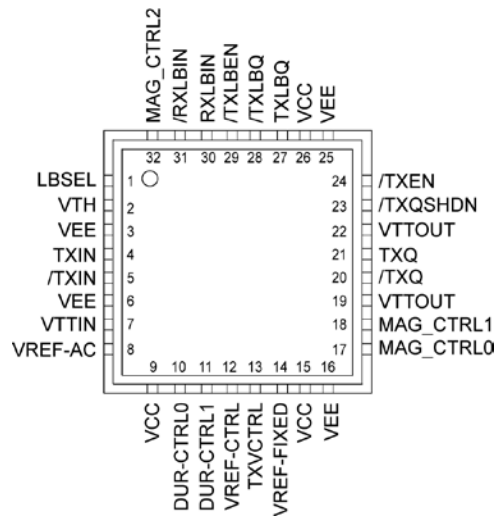
32-Pin QFN

Pin Description

Pin Number	Pin Name	Pin Function
4, 5	TXIN, /TXIN	Differential inputs: This input pair is the differential signal input to the device. They accept AC- or DC-coupled signals as small as 100mV (200mV$_{PP}$). Note that this input will default to an undetermined state if left open. TXIN and /TXIN internally terminate to the VTTIN pin through 50Ω. Please refer to the "Input Interface Applications" section for more details.
7	VTTIN	Input termination center-tap: TXIN and /TXIN terminate to VTTIN. The VTTIN pin provides a center-tap to the internal termination network for maximum interface flexibility and DC-offset capability. Please refer to the "Input Interface Applications" section for more details.
8	VREF-AC	Reference voltage: This output biases to V$_{CC}$ -1.3V. It is used for AC-coupling the input pair (TXIN, /TXIN). Connect VREF-AC directly to the VTTIN pin. Bypass with a 0.01uF low ESR capacitor to VCC. Maximum sink/source current is ±1.5mA. Due to the limited drive capability, the VREF-AC pin is only intended to drive the VTTIN pin. Please refer to the "Input Interface Applications" section for more details.
13	TXVCTRL	Analog input that controls TXQ output swing amplitude. The operating range of the control input is from VREF-CTRL (max swing) to VCC (min swing). Control of the output swing can be obtained by using a variable resistor between VREF-CTRL and VCC with the wiper driving TXVCTRL. Output swing ranges from 100mV$_{PK}$ to 1.5V$_{PK}$. When the TXQ output is selected for maximum swing amplitude of 1.5V$_{PK}$, no pre-emphasis is possible since the maximum swing cannot extend beyond 1.5V$_{PK}$. For applications that only require a fixed, full CML swing, connect TXVCTRL to VREF-FIXED.
12	VREF-CTRL	Reference control voltage for TXVCTRL swing control. The operating range of the control input is from VREF-CTRL (max swing) to VCC (min swing). Control of the output swing can be obtained by using a variable resistor between VREF-CTRL and VCC with the wiper driving TXVCTRL. Maximum sink/source current is ±1.5mA.
14	VREF-FIXED	Reference output voltage: Connect this reference output pin directly to the TXVCTRL input pin, and the TXQ output swing is fixed to 400mV$_{PK}$ (800mV$_{PP}$).
24	/TXEN	TTL/CMOS (or VTH controlled) compatible control input for the TXQ Outputs pair. When pulled HIGH, the TXQ Output pair is disabled. This input is internally connected to a 25kΩ pull-down resistor and will default to a logic LOW state (Enable) if left open. When disabled, the TXQ output goes LOW, and /TXQ goes HIGH. Default threshold is Vcc/2 when VTH pin is floating.
29	/TXLBEN	TTL/CMOS (or VTH controlled) compatible control input for the TXLBQ output pair. When pulled HIGH, the TXLBQ output pair is disabled. This input is internally connected to a 25kΩ pull-down resistor and will default to a logic LOW state (Enable) if left open. When disabled, the TXLBQ output goes LOW, and /TXLBQ goes HIGH. Default threshold is Vcc/2 when VTH pin is floating.
1	LBSEL	Loopback MUX select control: The TTL/CMOS (or VTH controlled) compatible input selects the input to the Loopback mode multiplexer. When LBSEL input is a logic HIGH, the Loopback mode is selected, and the RXLBIN input pair is selected to pass through the TXQ output. Note that the LBSEL pin is internally connected to a 25kΩ pull-down resistor and will default to a logic LOW state if left open (normal operation). The loopback MUX includes internal input isolation to minimize crosstalk.
30, 31	RXLBIN, /RXLBIN	Loopback differential input pair: AC-coupled, CML compatible input. This input pair includes internal termination connected to an internal VBB for an AC-coupled bias configuration. The RXLBIN input pair receives a signal from the RX buffer (SY58627L RXLBQ) loopback output. This input pair does not include any equalization. When Loopback mode is selected, the signal at the RXLBIN input is directed to the TXQ output.

Pin Description (Continued)

| Pin Number	Pin Name	Pin Function
27, 28	TXLBQ, /TXLBQ	Transmit loopback differential output: CML compatible output pair with 400mV swing into a 50Ω load (100Ω across the pair). The TXLBQ output pair is providing a copy of the TXIN input signal, bypassing the pre-emphasis stage. The SY58626L loopback function is optimized to operate with the SY58627L receiver, and the TXLBQ output pair is AC-coupled directly to the TXLBIN input pair on the SY58627L.
23	/TXQSHDN	TXQ shutdown control pin: The TTL/CMOS (or VTH controlled) compatible pin is an active LOW function. This input is internally connected to a 25kΩ pull-up resistor and will default to a logic HIGH state if left open. When pulled LOW, the TXQ and /TXQ output currents are shut off, and the TXQ and /TXQ output voltage is set to the same potential. The actual voltage level is set by the resistor divider ratio established by the internal 50Ω source resistors (connected to VTTOUT) and the external load. Default threshold is Vcc/2 when VTH pin is floating.
2	VTH	Input logic threshold control voltage for logic control threshold settings other than LVTTL/CMOS. This input control pin can be externally biased to set the proper threshold for all the logic control pins, /TXEN, LBSEL, /TXLBEN, 3-bit pre-emphasis control, 2-bit pre-emphasis duration control, and /TXQSHDN. For standard LVTTL/CMOS control, simply leave the VTH pin floating and the threshold voltage defaults to $V_{CC}/2$ (When VEE=0V). For LVPECL thresholds, set VTH to Vcc-1.3V.
21, 20	TXQ, /TXQ	Differential variable swing output pair: This CML output pair is the output of the device. This output is designed to drive $100mV_{PK}$ to $1.5V_{PK}$ into 50Ω (100Ω across the pair) with variable pre-emphasis. TXQ outputs include 50Ω source termination resistors. When the loopback mode is selected, the TXQ output pair is driven by the RXLBIN inputs.
19, 22	VTTOUT	Output termination center-tap: Each side of the differential output pair terminates to the VTTOUT pin through 50Ω. The VTTOUT pin provides a center-tap to the output termination network for maximum interface flexibility, and DC-offset capability. Please refer to the "CML Output Interface Applications" section for more details.
17 18 32	MAG_CTRL0 MAG_CTRL1 MAG_CTRL2	Pre-emphasis magnitude level control input: TTL/CMOS (or VTH controlled) compatible, 3-bit control interface. There are four levels of pre-emphasis magnitude, as shown in the "Pre-Emphasis Magnitude Truth Table." When MAG_CTRL2 (MSB) is logic 1, pre-emphasis is disabled and the TXQ outputs will not include any pre-emphasis. Pre-emphasis magnitude ranges from 10% to 33% above the base swing.
10 11	DUR_CTRL0 DUR_CTRL1	Pre-emphasis duration control input. TTL/CMOS (or VTH controlled) compatible, 2-bit control interface. This control establishes the pre-emphasis duration. Duration ranges from 60ps to 400ps typical as shown in the "Pre-emphasis Duration Control Truth Table." Pre-emphasis duration is measured from the mid-point of the pre-emphasis magnitude (50% point). Please refer to the "Pre-emphasis Output Description" for details.
9, 15, 26	VCC	Positive power supply: Connect to +3.3V power supply. Bypass with 0.1µF//0.01µF low ESR capacitors as close to VCC pins as possible.
3, 6, 16, 25	VEE, Exposed Pad	Ground: Ground pins and exposed pad must be connected to the same ground plane.

Pre-emphasis Magnitude Truth Table

Disable Mag Select (MSB=MAG_CTRL2)	Magnitude Select (MAG_CTRL1)	Magnitude Select (MAG_CTRL0)	Pre-emphasis Magnitude
0	0	0	10%
0	0	1	15%
0	1	0	25%
0	1	1	33%
1	X	X	Disabled

Pre-emphasis Duration Control Truth Table

Duration	DUR_CTRL1	DUR_CTRL0	Typical Data Rate	Time Duration
Minimum (Shortest)	0	0	3.2Gbps-6.4Gbps	60ps
Medium-short	0	1		100ps
Medium-long	1	0	DC-3.2Gbps	200ps
Longest	1	1		400ps

Pre-emphasis Output Description

6
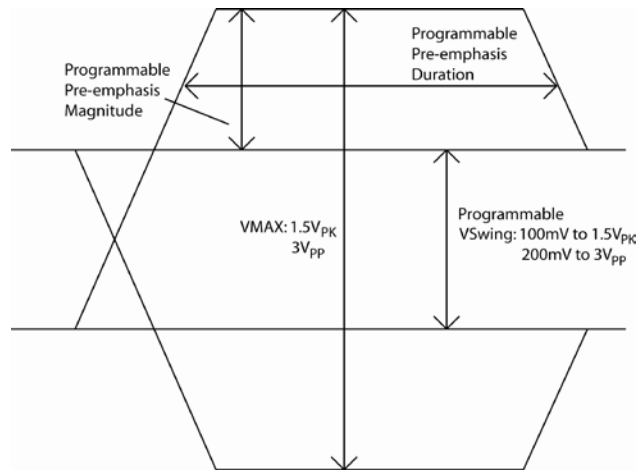
Absolute Maximum Ratings[1]

Supply Voltage (V_{CC})..-0.5V to +4.0V
Input Voltage (V_{IN})....................................... -0.5V to V_{CC}
Input Current (TXIN, /TXIN, ≤120mins) 67mA
CML Output Current (I_{OUT})
    Continuous (≤120mins)... 67mA
    Surge.. 100mA
Termination Current
    V_T.. ±100mA
V_{REF-AC} Current
    Source/sink current on V_{REF-AC}.. ±2mA
    Source/sink current on $V_{REF-CTRL}$..................................... ±2mA
Lead Temperature (soldering, 20 sec.) ....+260°C
Storage Temperature (T_S) .... -65°C to 150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) .... +3.0V to +3.6V
Ambient Temperature (T_A).............................. 0°C to +70°C
Package Thermal Resistance[3]
QFN (θ_{JA})
    Still-Air ....34°C/W
QFN (Ψ_{JB})
    Junction-to-Board ....20°C/W

DC Electrical Characteristics[4]

T_A= 0°C to +70°C; unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply		3.0	3.3	3.6	V
I_{EE}	Power Supply Current	Max $V_{CC,}$ includes 50Ω internal source resistors, 1.5V_{PK} output swing, no external load current		290	370	mA
R_{IN}	Input Resistance (TXIN-to-VTTIN)		45	50	55	Ω
R_{DIFF_IN}	Differential Input Resistance (TXIN-to-/TXIN)		90	100	110	Ω
V_{IH}	Input High Voltage (TXIN, /TXIN)		V_{EE}+1.5		V_{CC}	V
V_{IL}	Input LOW Voltage (TXIN, /TXIN)		V_{EE}+0.7		V_{IH}-0.1	V
V_{IN}	Input Voltage Swing (TXIN, /TXIN)	See Figure 4a.	0.1		1.5	V_{PK}
V_{DIFF_IN}	Differential Input Voltage Swing |TXIN-/TXIN|	See Figure 4b.	0.2			V_{PP}
V_{TTIN}	TXIN-to-VTTIN (TXIN, /TXIN)				1. 28	V
V_{TTIN} Range	VTTIN Voltage Range	Voltage applied to VTTIN pin	V_{EE}+1.7		V_{CC}+0.1	V
V_{TTOUT} Range	VTTOUT Voltage Range	Voltage applied to VTTOUT pin	V_{CC}-1.5		V_{CC}+1.5	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. θ_{JA} and Ψ_{JB} values are determined for a 4-layer board in still air unless otherwise stated.

4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. 500lfpm Airflow. $T_J \leq 125°C$.

TXQ Outputs DC Electrical Characteristics[5]

V_{CC} = 3.3V ±10%; V_{EE} = 0V; T_A = 0°C to + 70°C; R_L = 100Ω across output pair; unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OUT} Range	Output Voltage Range (TXQ, /TXQ)		V_{CC}-1.5		V_{CC}	V
V_{OUT}	TXQ Output Voltage Swing (TXQ, /TXQ)[6]	Maximum Swing (TXVCTRL = VREF-CTRL) No pre-emphasis	1500			mV$_{PK}$
		Minimum Swing (TXVCTRL = V_{CC})			100	
		Fixed Output Swing (TXVCTRL = VREF-Fixed)	325	400		
V_{DIFF_OUT}	TXQ Differential Output Voltage Swing |TXQ-/TXQ|[7]	Maximum Swing (TXVCTRL = VREF-CTRL) No pre-emphasis	3000			mV$_{PP}$
		Minimum Swing (TXVCTRL = V_{CC})			200	
		Fixed Output Swing (TXVCTRL = VREF-Fixed)	650	800		
R_{OUT}	Output Resistance		45	50	55	Ω
V_{REF-AC}	Output Voltage Reference		V_{CC}-1.4	V_{CC}-1.3	V_{CC}-1.2	V
$V_{REF-CTRL}$	VREF-CTRL Output Voltage		V_{CC}-1.4	V_{CC}-1.3	V_{CC}-1.2	V
TXVCTRL	Output Swing Control Voltage Range		V_{REF-AC}		V_{CC}	V
I_{TX} Q$_{SHDN}$	TXQ Shutdown Leakage Current		-500		500	µA

TXLBQ CML Output DC Electrical Characteristics[5]

V_{CC} = 3.3V ±10%; V_{EE} = 0V; T_A = 0°C to + 70°C; R_L = 100Ω across output pair; unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	TXLBQ Output High Voltage	R_L = 50Ω to Vcc	V_{CC}-0.040	V_{CC}-0.010	V_{CC}	V
V_{OUT}	TXLBQ Output Voltage Swing (TXLBQ, /TXLBQ)[6]		325	400		mV$_{PK}$
V_{DIFF_OUT}	TXLBQ Differential Output Voltage Swing |TXLBQ-/TXLBQ|[7]		650	800		mV$_{PP}$
R_{OUT}	Output Impedance		45	50	55	Ω

Notes:

5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. 500lfpm Airflow. $T_J \leq$ 125°C.

6. Please refer to figure 4a.

7. Please refer to figure 4b.

Logic Control DC Electrical Characteristics[8]

V_{CC} = 3.3V ±10%; V_{EE} = 0V; T_A = 0°C to + 70°C; unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage	All control input pins	V_{TH}+0.2		V_{CC}	V
V_{IL}	Input LOW Voltage	All control input pins	V_{EE}		V_{TH}–0.2	V
V_{CTRL}	Output Swing Control Voltage Range at TXVCTRL		V_{REF}-CTRL		V_{CC}	V
I_{IH}	Input HIGH Current				300	µA
I_{IL}	Input LOW Current		-300			µA
V_{TH}	Threshold Input Voltage	Voltage applied to pin (V_{EE} = 0V)	1.4	V_{CC}/2	2.6	V

Notes:

8. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. 500lfpm Airflow. $T_J \leq 125$°C.

AC Electrical Characteristics[9]

V_{CC} = 3.3V ±10%; V_{EE} = 0V; T_A = 0°C to + 70°C; R_L = 100Ω across output pair; unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Freq	Data Rate Throughput (TXQ)	1.5V_{PK} output swing, No pre-emphasis	DC		6.4	Gbps
		400mV output swing, 33% pre-emphasis	DC		6.4	
	Data Rate Throughput (TXLBQ)	400mV output swing	DC		6.4	Gbps
t_{pd}	Differential Propagation Delay	TXIN-to-TXQ (V_{IN} >200mV_{PK})	150	250	450	ps
		RXLBIN-to-TXQ		250		ps
t_{pd} Tempco	Differential Propagation Delay Temperature Coefficient			120		fs/°C
t_{EN}	TXQ Enable/Disable Time	/TXEN			600	ps
t_{LB_EN}	TXLBQ Enable/Disable Time	/TXLBEN		200		ps
t_{SHDN}	TXQ Shutdown Time	/TXQ_SHDN HIGH-to-LOW (TXQ Outputs SHUTDOWN)		3	4.5	ns
		/TXQ_SHDN LOW-to-HIGH (TXQ Outputs ON)		3	4.5	
t_{LBSEL}	Loopback Select Time	LBSEL		350	600	ps
t_{PROG}	Programming Logic Control Time	3-bit pre-emphasis magnitude, 2-bit duration control update-to-valid TXQ		1		ns
MAG_CTRL	Pre-emphasis Magnitude (Percent beyond base swing) MAG_CTRL (2,1,0)	(0,0,0)		10		%
		(0,0,1)		15		
		(0,1,0)		25		
		(0,1,1)		33		
		(1,X,X)		0		
DUR_CTRL	Pre-emphasis Duration DUR_CTRL (1,0)	Minimum (shortest)		60		ps
		Medium-short		100		
		Medium-long		200		
		Longest		400		
t_{SKEW}	Part-to-Part Skew	Note 10			200	ps
t_{JITTER}	Random Jitter (RJ)	Note 11, 13, 14, 15		1		ps
	Deterministic Jitter (DJ)	Note 12, 13, 14, 15		15		ps
t_r, t_f	Output Rise/Fall Time (20% to 80%)	At full output swing	20	50	80	ps

Notes:

9. High-frequency AC-parameters are guaranteed by design and characterization.

10. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

11. This jitter is the RMS difference between the RJ measured at the end of a 9in FR4 transmission line driven by the SY58626 and the signal source.

12. This jitter is a difference between the DJ measured at the end of a 9in FR4 transmission path driven by an SY58626 and the signal source.

13. PE Mag: 010 and PE Dur: 10.

14. The typical jitter is measured at 4.25Gbps and 6.4Gbps using PRBS 2^7 pattern and 4.25Gbps using K28.5 pattern.

15. The transmission line is differential 6mil FR4 stripline with 100Ω differential impedance.

Detailed Description

The SY58626L is a high speed, low jitter transmit buffer with integrated loopback capability. Adjustable pre-emphasis amplitudes and selectable pre-emphasis durations are included with the transmitter. The SY58626L also includes disable and shutdown control for the transmitter output.

Transmitter

The SY58626L transmitter includes the VTTIN and VTTOUT pin for maximum interface flexibility and DC-offset capability for the input and output, respectively. This feature allows for interfacing with different logic families without the use of AC-coupling. The output buffer has internal 50Ω source terminated CML outputs for minimizing round-trip reflections.
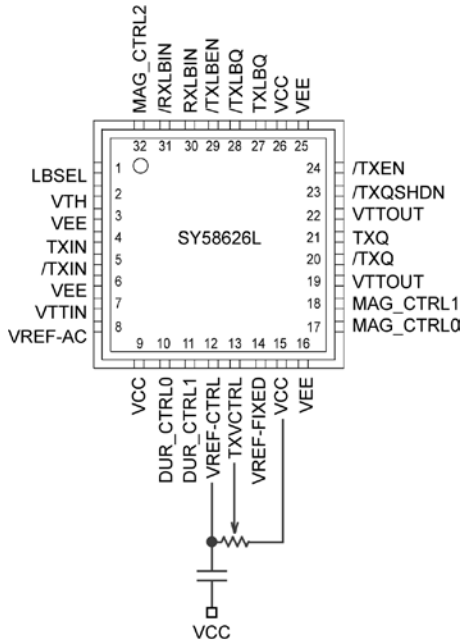
Figure 1. Variable Output Swing Circuit

Transmitter Variable-Swing Output Buffer

- Connecting VREF-CTRL to TXVCTRL sets the transmitter output buffer to max swing $1.5V_{PK}$ ($3.0V_{PP}$).
- Connecting VCC to TXVCTRL sets the transmitter output buffer to minimum swing $100mV_{PK}$ ($200mV_{PP}$).
- Connecting VREF-FIXED to TXVCTRL sets the transmitter output buffer to $400mV_{PK}$ ($800mV_{PP}$).

- Control of the transmitter output swing buffer can be obtained by using a variable resistor connected between VREF-CTRL and VCC with the wiper driving TXVCTRL. Please refer to Figure 1 for more details.

Transmitter Disable and Shutdown

The SY58626L provides two methods to turn off the output when desired. When /TXEN is pulled HIGH, the transmitter output pair is disabled. TXQ goes to a LOW state and /TXQ goes to a HIGH state. When /TXQSHDN is pulled LOW, the transmitter output pair is in shutdown mode. TXQ and /TXQ output currents are shut off and the TXQ and /TXQ outputs are set to the same potential. The threshold for the /TXEN and /TXQSHDN pins is set with the VTH pin. Please refer to the "Typical Operating Characteristics" for more details.

Loopback

The SY58626L features a loopback test mode, activated by setting LBSEL to logic HIGH. Using the SY58626L with the SY58627L enables local loopback and link side loopback, shown in Figures 2b and 2c. This mode enables an external loopback path, bypassing circuitry on both local and link side. Please refer to Table 1 and Figure 3 for Loopback Control information.
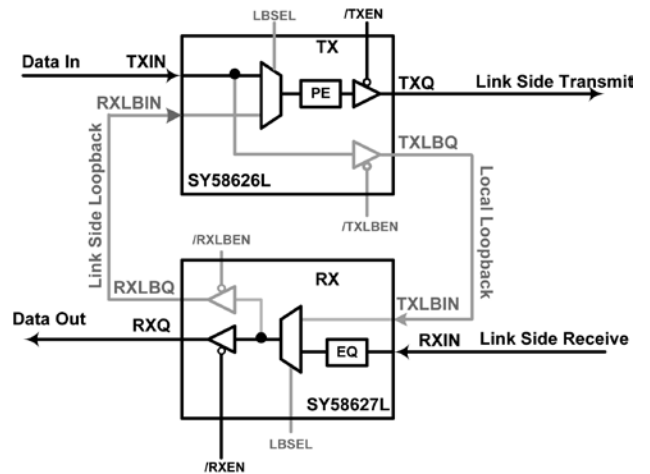
Figure 2a. Normal Operation
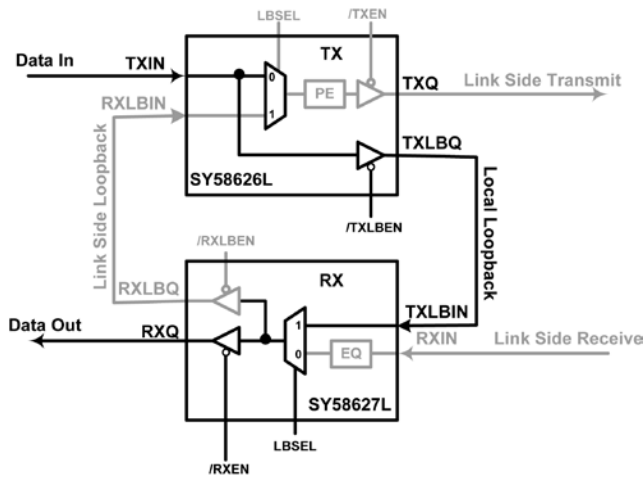
Figure 2b. Local Loopback Mode

	TXLB	TXLBENb	TXENb	TXQ	TXLBQ
Normal Mode	0	0	0	TXIN	TXIN
	0	0	1	0	TXIN
	0	1	0	TXIN	0
	0	1	1	0	0
Link Side Loopback Mode	1	0	0	RXLBIN	TXIN
	1	0	1	0	TXIN
	1	1	0	RXLBIN	0
	1	1	1	0	0

Table 1. Transmit Loopback Control Signal
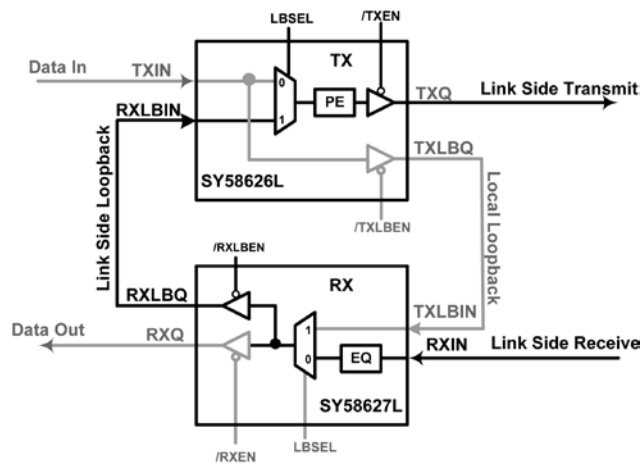
Figure 2c. Link Side Loopback Mode
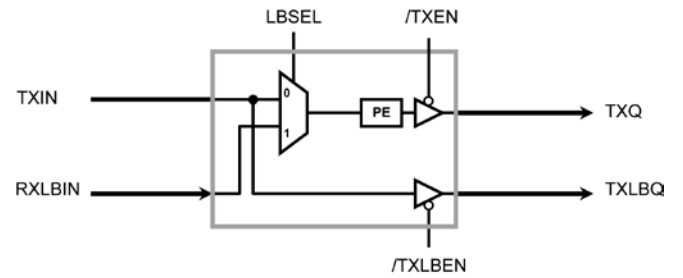
Figure 3. Loopback Control Pin

Typical Operating Characteristics

V_{CC} = 3.3V ±10%; V_{IN} > 400mV; T_A = 25°C, R_L = 100Ω across output pair; unless otherwise stated.

1m FR4 Output without
SY58626L 2.5Gbps PRBS 2^{-23}

Output Swing (100mV/div.)

TIME (50ps/div.)

1m FR4 Output with
SY58626L 2.5Gbps PRBS 2^{-23}

Output Swing (100mV/div.)

TIME (50ps/div.)

8in FR4 Output without
SY58626L 4.25Gbps PRBS 2^{-23}

Output Swing (100mV/div.)

TIME (66ps/div.)

8in FR4 Output with
SY58626L 4.25Gbps PRBS 2^{-23}

Output Swing (100mV/div.)

TIME (66ps/div.)

8in FR4 Output without
SY58626L 6.4Gbps PRBS 2^{-23}

Output Swing (100mV/div.)

TIME (66ps/div.)

8in FR4 Output with
SY58626L 6.4Gbps PRBS 2^{-23}

Output Swing (100mV/div.)

TIME (66ps/div.)

Typical Operating Characteristics (Continued)

V_{CC} = 3.3V ±10%; V_{IN} > 400mV; T_A = 25°C, R_L = 100Ω across output pair; unless otherwise stated.

Output Disable

Time (250ns/div.)

Output Shutdown

Time (250ns/div.)
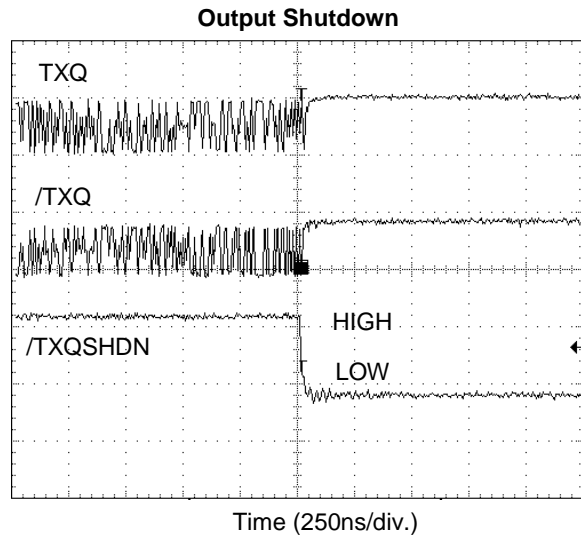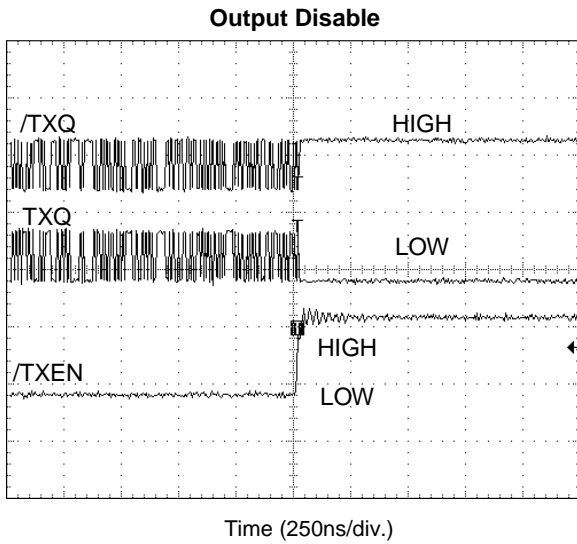
Single-Ended and Differential Swings
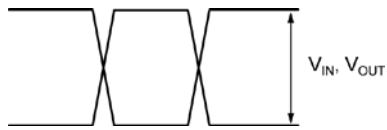
Figure 4a. Single-Ended Voltage Swing
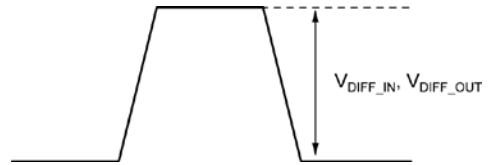
Figure 4b. Differential Voltage Swing

Input and Output Stages
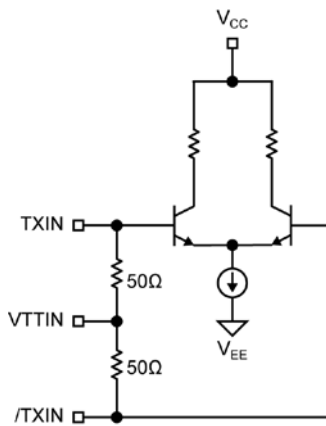
Figure 5a. Simplified Differential Input Stage
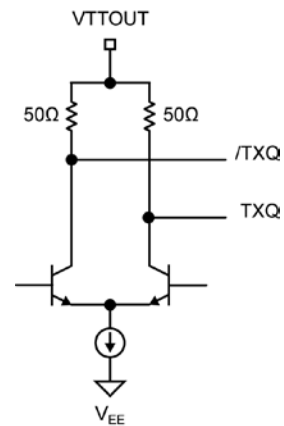
Figure 5b. Simplified Differential Output Stage

Input Interface Applications
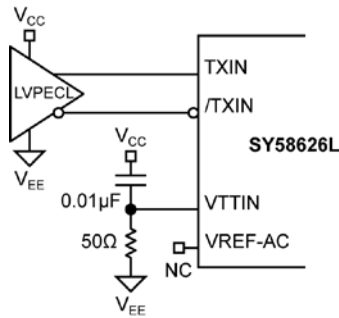
**Figure 6a. LVPECL Interface
(DC-Coupled)**
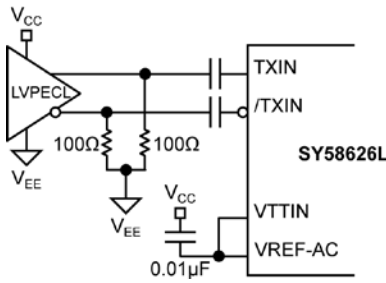
**Figure 6b. LVPECL Interface
(AC-Coupled)**
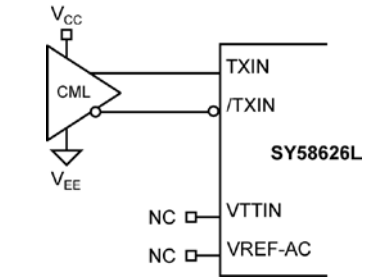
option: may connect VTTIN to VCC

**Figure 6c. CML Interface
(DC-Coupled)**
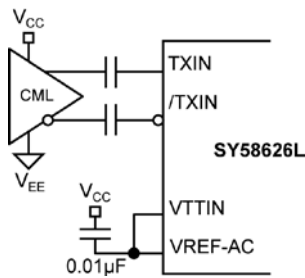
**Figure 6d. CML Interface
(AC-Coupled)**
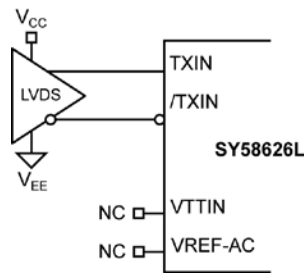
**Figure 6e. LVDS Interface
(DC-Coupled)**

CML Output Interface Applications
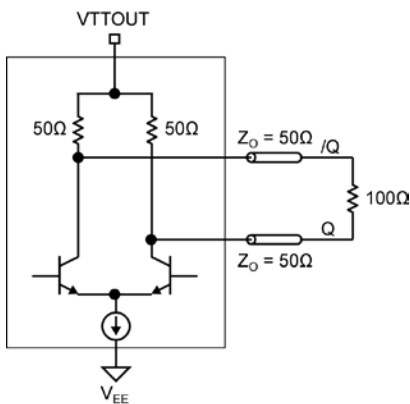
Figure 7a. CML DC-Coupled Termination
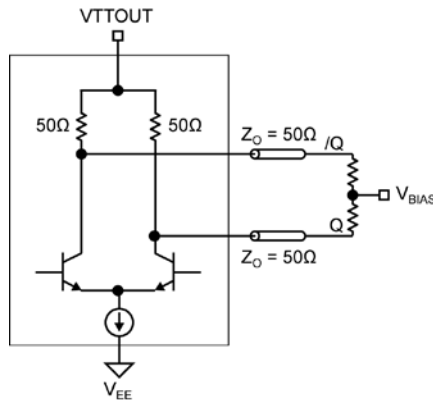
Figure 7b. CML DC-Coupled Termination
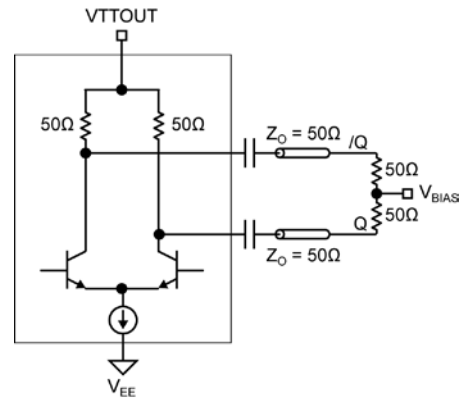
Figure 7c. CML AC-Coupled Termination

Related Product and Support Information

Part Number	Function	Datasheet Link
SY58627L	DC-to-6.4Gbps Backplane Receive Buffer with 4-Stage Programmable Equalization and DC-Offset Control	www.micrel.com/product-info/products/sy58627u.shtml
HBW Solutions	New Products and Applications	www.micrel.com/product-info/products/solutions.shtml

Package Information
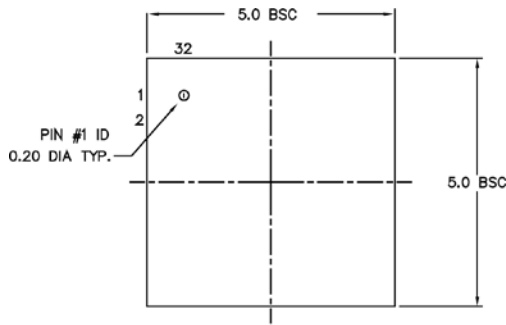
TOP VIEW
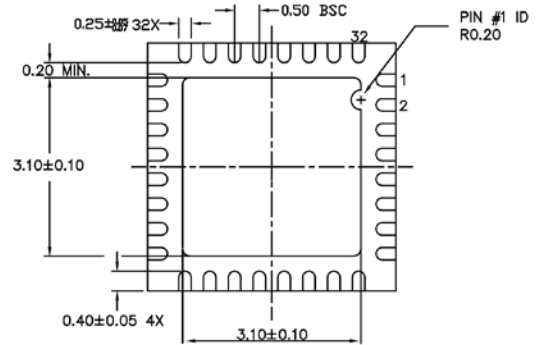
BOTTOM VIEW
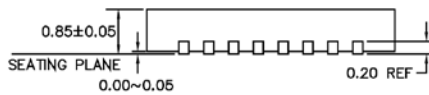
SIDE VIEW

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.

32-Pin QFN

Package Notes:

1. Package meets Level 2 Moisture Sensitivity Classification.
2. All parts are dry-packed before shipment.
3. Exposed pad must be soldered to a ground for proper thermal management.

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