

DGT409BCA Reverse Blocking Gate Turn-off Thyristor

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APPLICATIONS

The DGT409BCA is a symmetrical GTO designed for applications, which specifically require a reverse blocking capability, such as current source inverter (CSI). Reverse recovery ratings and characteristics are included.

FEATURES

- Reverse blocking Capability
- Double Side Cooling
- High Reliability In Service
- High Voltage Capability
- Fault Protection Without Fuses
- Turn-off Capability Allows Reduction in Equipment Size and Weight. Low Noise Emission Reduces Acoustic Cladding Necessary For Environmental Requirements

ORDERING INFORMATION

Order as: DGT409BCA6565

KEY PARAMETERS

I _{TCM}	1500A
V_{DRM}/V_{RRM}	6500V
dV _D /dt	1000V/μs
dl _T /dt	300A/μs



Fig. 1 Package outline



VOLTAGE RATINGS

Type Number	Repetitive Peak Off-state Voltage V _{DRM} (V)	Repetitive Peak Reverse Voltage V _{RRM} (V)	Conditions
DGT409BCA	6500	6500	$T_{vj} = 115 ^{\circ}C, I_{DM} =, I_{RRM} = 100 \text{mA}$

CURRENT RATINGS

Symbol	Parameter	Conditions	Max.	Units
I _{TCM}	Repetitive peak controllable on-state current	V _D = 4300V, T _j = 115 °C, dI _{GQ} /dt = 20A/μs, C _S = 2 μF	1500	А

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I _{TSM}	Surge (non repetitive) on-state current	10ms half sine. $T_j = 115 \degree$ C	3.0	kA
l ² t	I ² t for fusing	10ms half sine. $T_j = 115 \degree$ C	45	kA ² s
di _T /dt	Critical rate of rise of on-state current	$\label{eq:VD} \begin{array}{l} V_{D} = 3000V, \ I_{T} = 800A, \ T_{j} = 115 \ ^{o}\!C, \ I_{FG} > 20A, \\ Rise \ time \ (t_{r}) > 1.5 \ \mu s \end{array}$	300	A/µs
d\/_/dt	dt Rate of rise of off-state voltage	$V_{D}{=}\;3000V;R_{GK}\;\leq 1.5\Omega,T_{j}{=}\;115{}^{\circ}\!C$	175	V/µs
av _D /at		V_{D} = 3000V; $V_{RG} \le -2V$, T_{j} = 115 °C	1000	V/µs
Ls	Peak stray inductance in snubber circuit	$I_{T} = 1500A, V_{DM} = 6000V, Tj = 115^{\circ}C, dI_{GQ} = 20A/us, C_{S} = 2.0uF$	200	nH

GATE RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V _{RGM}	Peak reverse gate voltage	This value may exceeded during turn-off	-	25	V
I _{FGM}	Peak forward gate current		20	70	А
P _{FG(AV)}	Average forward gate power		-	10	W
P _{RGM}	Peak reverse gate power		-	15	kW
di _{GQ} /dt	Rate of rise of reverse gate current		15	60	A/µs
t _{ON(min)}	Minimum permissible on time		50	-	μS
t _{OFF(min)}	Minimum permissible off time		150	-	μS
I _{RGM}	Continuous reverse gate-cathode current	V _{RGM} = 16V, No gate cathode resistor	-	50	mA



THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
R _{th(j-hs)} T	Thermal resistance – junction to heatsink surface	Double side cooled	DC	-	0.046	°C/W
		Single side cooled	Anode DC	-	0.073	°C/W
			Cathode DC	-	0.124	°C/W
$R_{\text{th(c-hs)}}$	Contact thermal resistance	Clamping force 32.0kN With mounting compound	Per contact	-	0.009	℃/W
T_{vj}	Virtual junction temperature	On-state (conducting)		-	115	°C
T _{op} /T _{stg}	Operating junction/storage temperature range			-40	115	°C
F _m	Clamping force			11.0	15.0	kN

CHARACTERISTICS

Tj =115°C unless stated otherwise

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V _{TM)}	On-state voltage	At 200A peak, $I_{G(ON)} = 4A \text{ d.c.}$	-	4	V
I _{DM}	Peak off-state current	$V_{\text{DRM}} = 6500V, \ V_{\text{RG}} = 0V$	-	100	mA
I _{RRM}	Peak reverse current	V _{RRM} = 6500V	-	100	mA
V _{GT}	Gate trigger voltage	$V_D = 24V, I_T = 100A, Tj = 25^{\circ}C$	-	1	V
I _{GT}	Gate trigger current	$V_D = 24V, I_T = 100A, Tj = 25^{\circ}C$	-	2	А
I _{RGM}	Reverse gate cathode current	V_{RGM} = 16V, No gate/cathode resistor	-	50	mA
E _{ON}	Turn-on Energy	V _D = 3000V	-	2500	mJ
t _d	Delay time	I _T = 400A, dI _T /dt = 150A/μs	-	3	μs
tr	Rise time	I_{FG} = 20A, rise time (t _r) < 1.5µs	-	7	μs
E _{OFF}	Turn-off energy		-	2500	mJ
t _{gs}	Storage time			47	μs
t _{gf}	Fall time	$I_T = 800A, V_{DM} = 3000V$	See Fig.17 and Fig.18		μs
t _{gq}	Gate controlled turn-off time	Snubber Cap Cs = 2µC			μs
Q _{GQ}	Turn-off gate charge	di _{GQ} /dt = 20A/us	-	3600	μC
Q _{GQT}	Total turn-off gate charge		-	7200	μC
I _{GQM}	Peak reverse gate current		-	350	А





Fig.2 General switching waveforms



CURVES



Fig.3 Reverse recovery waveforms









DGT409BCA



Conditions:

 $T_j = 115^{\circ} \text{ C}, I_{FG} = 20\text{ A},$ $C_S = 2\mu\text{F}, R_S = 10\Omega,$

 $V_{\rm D} = 3000$ V, dl_T/dt = 150A/µs dl_{FG}/dt = 30A/µs



Peak forward gate current, I_{FGM} - (A)



On-state current, $I_T - (A)$

t_d

V_D = 1500V

Conditions:

 $\begin{array}{l} T_{\rm j} = 115^{\circ} \, {\rm C}, \, {\rm I}_{\rm T} = 400 {\rm A}, \\ {\rm C}_{\rm S} = 2 \mu {\rm F}, \, {\rm R}_{\rm S} = 20 \Omega, \\ {\rm d} {\rm I}_{\rm T} / {\rm d} {\rm t} = 150 {\rm A} / \mu {\rm s}, \end{array}$

 $dI_{FG}/dt = 30A/\mu s$









Fig.16 Turn-off energy vs rate of rise of reverse gate current













PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



Fig.20 Package outline



POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.

Stresses above those listed in this data sheet may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed.



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