

HYUNDAI**HYM572A224A R-Series****Unbuffered 2M x 72-bit CMOS DRAM MODULE
with EXTENDED DATA OUT****DESCRIPTION**

The HYM572A224A is a 2M x 72-bit EDO mode CMOS DRAM module consisting of two HY514404B in 20/26 pin SOJ or TSOP-II, four HY5118164B 42/42 pin SOJ or 44/50 pin TSOP-II and one 2048bit EEPROM on a 168 pin glass-epoxy printed circuit board. 0.1 μ F and 0.01 μ F decoupling capacitor is mounted for each DRAM.

The HYM572A224ARG/ASLRG/ATRG/ASLTRG is Gold plated socket type Dual In-line Memory Modules suitable for easy interchange and addition of 16M byte memory.

FEATURES

- **Low power dissipation**
Max. self-refresh 22.0mW (SL-part)
Max. battery back-up 28.6mW (SL-part)
Max. CMOS standby 17.6mW (SL-part)
66.0mW
Max. TTL standby 132.0mW
Max. operating

Speed	Power
60	4.58W
70	4.25W
80	3.15W

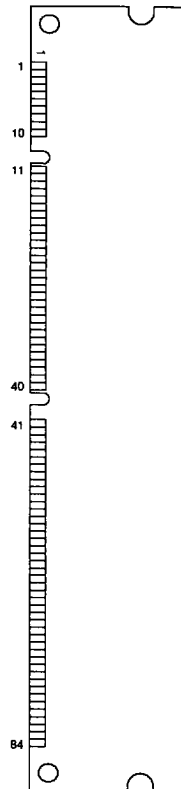
- **Single power supply of 5V \pm 10%**
- **TTL compatible inputs and outputs**
- **Fast access time**

Speed	tRAC	tCAC	tHPC
60	60ns	15ns	25ns
70	70ns	20ns	30ns
80	80ns	20ns	35ns

- **EDO mode operation**
- **CAS-before-RAS, RAS-only and Hidden refresh**
- **1024 refresh cycles / 256ms (SL-part)**
1024 refresh cycles / 16ms
- **Serial Presence Detect**

PIN DESCRIPTION

RAS0,RAS2	Row Address Strobe
CAS0-CAS7	Column Address Strobe
WE0,WE2	Write Enable
OE0,OE2	Output Enable
A0-A9	Address Input
SLC	Serial PD Clock Input
SDA	Serial PD Data Input/Output
SA0-SA2	Serial PD Device Add. Input
Vcc	Power (+ 5V)
Vss	Ground

PIN CONNECTION

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1EC06-10-APR95

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PIN NAME

#	NAME	#	NAME	#	NAME	#	NAME
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	OE2	86	DQ32	128	NC
3	DQ1	45	RAS2	87	DQ33	129	RAS3
4	DQ2	46	CAS2	88	DQ34	130	CAS5
5	DQ3	47	CAS3	89	DQ35	131	CAS7
6	Vcc	48	WE2	90	Vcc	132	NC
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	CB14
9	DQ6	51	NC	93	DQ38	135	CB15
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vcc	101	DQ45	143	Vcc
18	Vcc	60	DQ20	102	Vcc	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	NC	105	CB4	147	NC
22	CB1	64	Vss	106	CB5	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	Vcc	68	Vss	110	Vcc	152	Vss
27	WE0	69	DQ24	111	NC	153	DQ56
28	CAS0	70	DQ25	112	CAS4	154	DQ57
29	CAS1	71	DQ26	113	CAS5	155	DQ58
30	RAS0	72	DQ27	114	RAS1	156	DQ59
31	OE0	73	Vcc	115	NC	157	Vcc
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	NC	121	A9	163	NC
38	NC	80	NC	122	NC	164	NC
39	NC	81	NC	123	NC	165	SA0
40	Vcc	82	SDA	124	Vcc	166	SA1
41	NC	83	SCL	125	NC	167	SA2
42	NC	84	Vcc	126	NC	168	Vcc

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SERIAL PD BYTE DEFINITION

BYTENUMBER	FUNCTION DESCRIBED	FUNCTION	VALUE
Byte 0	Number of Byte written during module production	15 Bytes	0Fh
Byte 1	Total Byte of Serial Presence Detect Device	256 Bytes	08h
Byte 2	Memory Type	EDO	02h
Byte 3	Number of ROW Addresses	10	0Ah
Byte 4	Number of COLUMN Addresses	10	0Ah
Byte 5	Number of Banks	2 Bank	02h
Byte 6	Module Data Width	72bit	48h
Byte 7	Module Data Width(Continued)	Not Used	00h
Byte 8	Module Interface Levels	TTL	00h
Byte 9	tRAC	60ns 70ns 80ns	3Ch 46h 50h
Byte 10	tCAC	15ns 20ns 20ns	0Fh 14h 14h
Byte 11	Module Configuration Type	ECC	02h
Byte 12	Refresh Rate/Type	Normal(15.6μs) SL-Part(250μs)	00h 86h
Byte 13	Primary DRAM Width	x16	10h
Byte 14	Error Checking DRAM width	x4	04h
Byte 15 - 255	Undefined	Undefined	Undefined

NOTE:

1. Serial PD interface is standard IIC architecture.
2. Pull-up resistors(4.7K typical value) are required on all open collector bus devices (SCL and SDA).
3. Current sink capability on SCL and SDA (IoL max) must be at least 3ma to maintain a valid low level.

IIC BUS INTERFACE

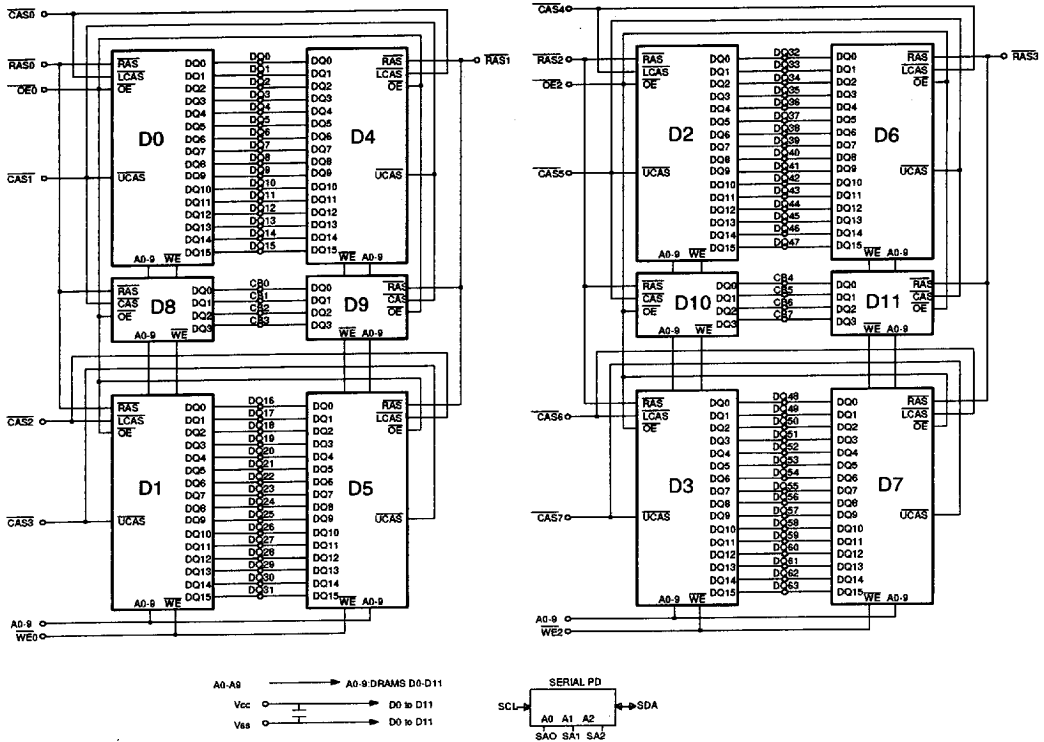
SYMBOL	RATING	NOTE
C _{MAX}	400pF	1
f _{MAX}	80 KHz(3.3V) 100 KHz(5.0V)	2
I _{OL MAX}	3mA	

NOTE:

1. The maximum number of devices connected on the IIC bus is controlled by the maximum allowable capacitance which is 400pF per line.
2. The maximum IIC system clock frequency depends on Vcc.

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BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-1.0 to 7.0	V
Vcc	Voltage on Vcc Relative to Vss	-1.0 to 7.0	V
IOS	Short Circuit Output Current	50	mA
Pd	Power Dissipation	8	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Vcc	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	Vcc+ 1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to Vss.

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DC CHARACTERISTICS

(TA= 0°C to 70°C, Vcc= 5V± 10%, Vss= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pin)	Vss ≤ VIN ≤ Vcc+ 1.0, other pins not under test= Vss		-80	80	µA	
ILO	Output Leakage Current (High Impedance State)	Vss ≤ VOUT ≤ Vcc, RAS & CAS at VIH		-20	20	µA	
Icc1	Vcc Supply Current, Operating	trC= trC (min.)	60 70 80	-	832 772 572	mA	1,2,3
Icc2	Vcc Supply Current, TTL Standby	RAS & CAS at VIH, other inputs ≥ Vss		-	24	mA	
Icc3	Vcc Supply Current, RAS-only refresh	trC= trC (min.)	60 70 80	-	832 772 572	mA	1,3
Icc4	Vcc Supply Current, Fast Page mode	thPC= thPC (min.)	60 70 80	-	752 652 412	mA	1,2,3
Icc5	Vcc Supply Current, CMOS Standby	RAS & CAS ≥ Vcc-0.2V	SL-part	-	12 3.2	mA	
Icc6	Vcc Supply Current, CAS-before-RAS refresh	trC= trC (min.)	60 70 80	-	832 772 572	mA	1,3
Icc7	Vcc Supply Current, Battery Back Up (SL-part only)	trC= 250µs, CAS= CBR cycling or 0.2V OE & WE= Vcc-0.2V,3.2 A0-A9= Vcc-0.2V, 0.2V DQ0-DQ71= 0.2V, Vcc-0.2V or open	trAS ≤ 300ns trAS ≤ 1µs	-	4 5.2	mA	1,4,5
Icc8	Vcc Supply Current Self Refresh (SL-part)	RAS&CAS= VIL OE & WE & A0-A9= Vcc 0.2V or 0.2V DQ0-DQ71= Vcc - 0.2V , 0.2V or open			4		
VoL	Output Low Voltage	IOL= 4.2mA		-	0.4	V	
VoH	Output High Voltage	IOH= -5mA		2.4	-	V	

NOTE :

- Icc1, Icc3, Icc4, Icc6 and Icc7 depend on cycle rate.
- Icc1, Icc3, Icc4, and Icc6 depend on output loading. Specified values are obtained with the output open.
- Icc is specified as average current. for Icc1, Icc3, and Icc6, address can be changed maximum two times while RAS= VIL. for Icc4, address can be changed maximum once while CAS= VIH.
- Only trAS(max.)= 1µs is applied to refresh of battery backup but trAS(max.)= 10s is applied to normal functional operation
- Icc5(max.)= 3.2mA, Icc7 and Icc8 are applied to SL-part (HYM572A224ASLTR/ASLTRG).

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AC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 5V± 10%, VSS = 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM572A224A R-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	105	-	125	-	145	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	142	-	167	-	187	-	ns	
3	tHPC	EDO Mode Cycle Time	25	-	30	-	35	-	ns	
4	tHPRWC	EDO Mode Read-Modify-Write Cycle Time	73	-	85	-	100	-	ns	
5	tRAC	Access Time from RAS	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from CAS	-	15	-	20	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	35	-	35	-	40	ns	4
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tCEZ	Output Buffer Turn-off Delay	0	15	0	15	0	15	ns	5
11	tT	Transition Time (Rise and Fall)	2.5	50	2.5	50	2.5	50	ns	3
12	tRP	RAS Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	RAS Pulse Width (EDO Mode)	60	100K	70	100K	80	100K	ns	
15	tRSH	RAS Hold Time	13	-	15	-	20	-	ns	
16	tCSH	CAS Hold Time	40	-	50	-	60	-	ns	
17	tCAS	CAS Pulse Width	13	10K	15	10K	20	10K	ns	
18	tRCD	RAS to CAS Delay	20	45	20	50	20	60	ns	9
19	tRAD	RAS to Column Address Delay Time	15	30	15	35	15	40	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	
21	tCP	CAS Precharge Time	7	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10	-	15	-	15	-	ns	
26	tAR	Column Address Hold Time from RAS	30	-	35	-	35	-	ns	
27	tRAL	Column Address to RAS Lead Time	30	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	10	-	15	-	15	-	ns	
32	tWCR	Write Command Hold Time from RAS	30	-	35	-	35	-	ns	
33	tWP	Write Command Pulse Width	10	-	10	-	10	-	ns	
34	tRWL	Write Command to RAS Lead Time	15	-	15	-	15	-	ns	
35	tCWL	Write Command to CAS Lead Time	13	-	15	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	10	-	15	-	15	-	ns	7
38	tDHR	Data-In Hold Time Referenced to RAS	30	-	35	-	35	-	ns	
39	tREF	Refresh Period (1024 cycles)		16		16		16	ms	
		SL-part		256		256		256	ms	12
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

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AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HYM572A224A R-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	CAS to WE Delay Time	37	-	45	-	45	-	ns	8
42	tRWD	RAS to WE Delay Time	80	-	95	-	105	-	ns	8
43	tAWD	Column Address to WE Delay Time	50	-	60	-	65	-	ns	8
44	tCSR	CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
45	tCHR	CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
46	tRPC	RAS to CAS Precharge Time	5	-	5	-	5	-	ns	
47	tCPT	CAS Precharge Time (CBR Counter Test)	30	-	35	-	40	-	ns	
48	tROH	RAS Hold Time Reference to OE	10	-	10	-	10	-	ns	
49	tOEA	OE Access Time	-	17	-	20	-	20	ns	
50	tOED	OE to Data Delay	15	-	20	-	20	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from OE	0	15	0	15	0	15	ns	5
52	tOEH	OE Command Hold Time	15	-	20	-	20	-	ns	
53	tCPWD	WE Delay Time from CAS Precharge	55	-	65	-	75	-	ns	8
54	tRHCP	RAS Hold Time from CAS Precharge	40	-	40	-	50	-	ns	
55	tWRP	WE to RAS Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
56	tWRP	WE to RAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	

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NOTE :

1. An initial pause of 200 μ s is required after power-up followed by 8 RAS cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS-before-RAS initialization cycles instead of 8 RAS-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. If RAS= Vss during power-up, the HYM572A224A could begin an active cycle. This condition results in higher power-up current than necessary demands from the power-up. It is recommended that RAS and CAS track with VCC during power-up or be held at a valid VIH in order to minimize the power-up current.
3. Refer to the HY514404B and HY5118164B data sheet for detailed information.
4. Measured with a load equivalent to 2 TTL loads and 100pF. (VOH= 2.0V, VOL= 0.8V)
5. tCEZ(max.) tOEZ(MAX), tREZ(MAX) and tWEZ(MAX) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either tRCH or tRRH must be satisfied for a read cycle.
7. These parameters are referenced to CAS leading edge in early write cycles and to WE leading edge in late write or read-modify-write cycles.
8. twcs is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If twcs \geq twcs(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
9. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
10. Operation within the tRAD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
11. Measured with the specified current load and 100pF.
12. A burst of 1024 CAS-before-RAS refresh cycles must be executed within 16ms after exiting self refresh (for SL-part).
13. If tcwd \geq twcs(MIN.), trwd \geq trwd(MIN.), tawd \geq tawd(MIN.) and tcpwd \geq tcpwd(MIN.), the cycle is a read modify write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time and until CAS goes back to VIH) is indeterminated.
14. In CAS before RAS self refresh mode.
 In case of using distributed CAS before RAS refresh, refresh 1024 times during a 256ms after reset
 In case of using burst CAS before RAS refresh, refresh 1024 times during a 16ms after reset
 In case of using RAS only refresh, refresh against all refresh address during a 16ms after reset
15. If RAS goes to high before CAS high going, the open circuit condition of the output is achieved by CAS high going. If CAS goes to high before RAS high going, the open circuit condition of the output is achieved by RAS high going.

CAPACITANCE

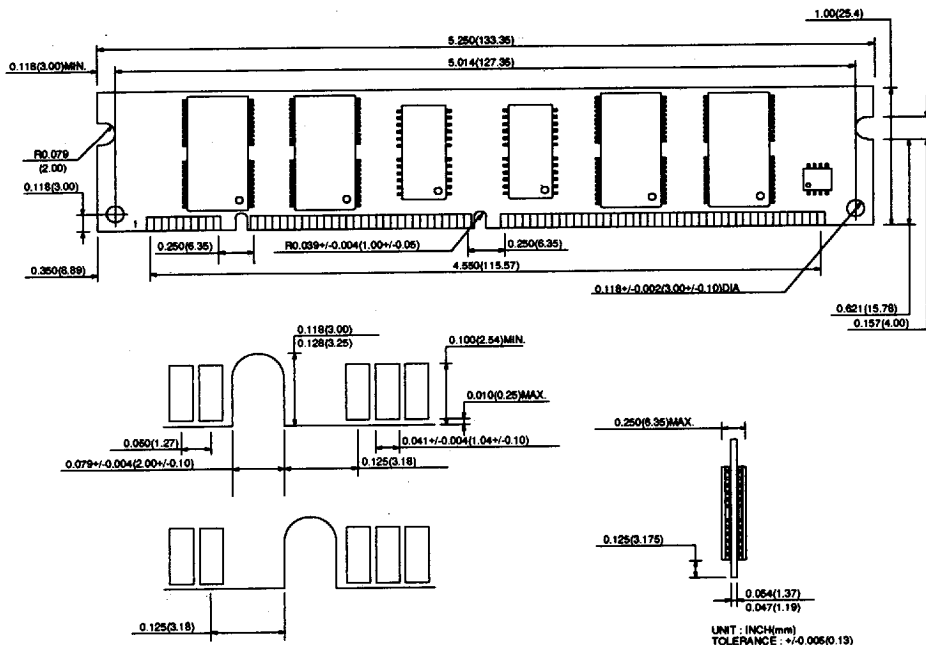
(TA= 25°C, Vcc= 5V \pm 10%, Vss= 0V, f= 1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A9)	-	80	pF
CIN2	Input Capacitance (WE0, WE2, OE0, OE2)	-	55	pF
CIN3	Input Capacitance (RAS0, RAS2)	-	55	pF
CIN4	Input Capacitance (CAS0-CAS7)	-	24	pF
CDQ	Data Input/output Capacitance (DQ0-DQ71)	-	24	pF

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PACKAGE INFORMATION

168 pin Dual In-line Memory Module (RG ; Gold plated)



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ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM572A224ARG	60/70/80		DIMM	Gold
HYM572A224ASLRG	60/70/80	SL-part	DIMM	Gold
HYM572A224ATRG	60/70/80		DIMM	Gold
HYM572A224ASLTRG	60/70/80	SL-part	DIMM	Gold

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