TOSHIBA CMOS Integrated Circuit   Silicon Monolithic

J T 6 N 4 6 S

Single-Chip System LSI for RFID Card

The JT6N46S is a system LSI for radio frequency identification (RFID) wireless cards. The JT6N46S incorporates an analog circuit, a data processing circuit and data memory in a single chip.
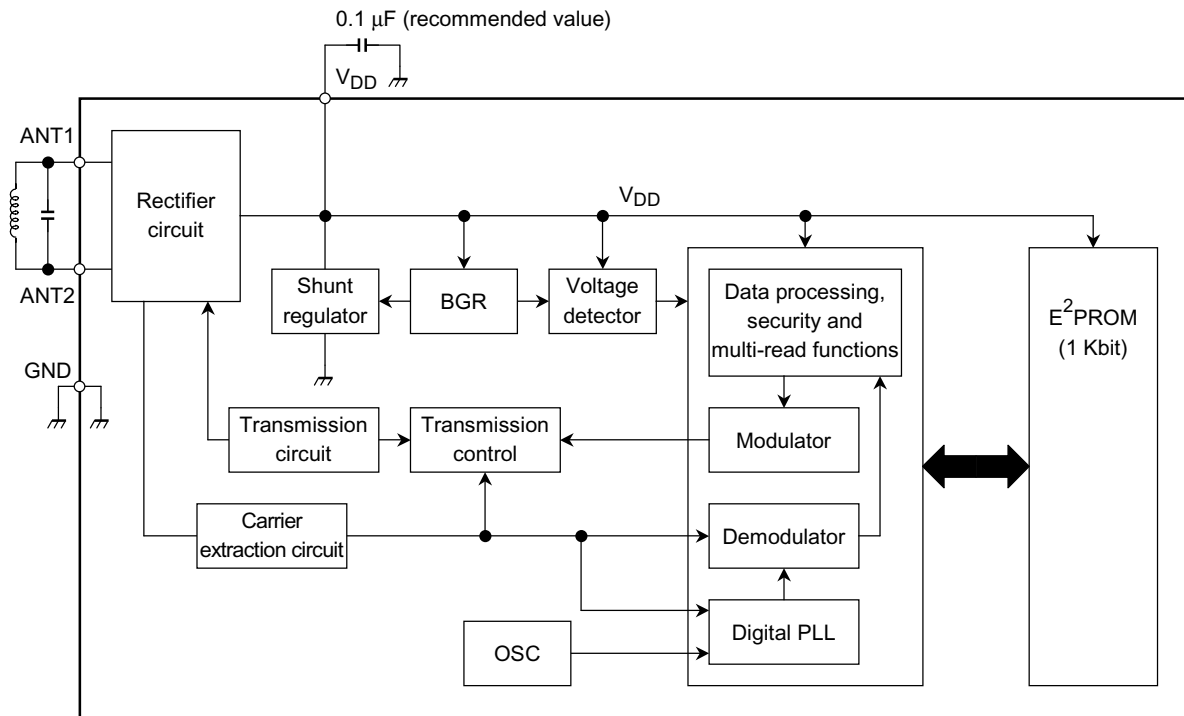
Features

- High-noise-resistant PSK modulation:
  binary phase-shift keying (BPSK) for both reader-to-RFID and RFID-to-reader transmission.
- Start-stop synchronization and half-duplex transmission: with parity, 1 stop bit
- High-efficiency power generation circuit using electromagnetic induction:
  battery less operation, full-wave rectifier circuit, shunt regulator
- Data processing logic circuit: digital PLL, security circuit
- High-reliability E²PROM: 4 Kbits
  - Maximum write time: 7 ms (16-byte batch write)
  - Overwrite: 100,000 times
  - Data retention: 10 years
- Selectable receive carrier frequency: 100 kHz to 500 kHz (when external antenna circuit is used)
- Programmable security circuit: security level can be set
- High-speed transfer rate of 25 kbps: 1/16 of receive carrier frequency = 400 kHz
- High-speed multi-read of 32 IDs per second: when receive carrier frequency = 400 kHz (ID only read)
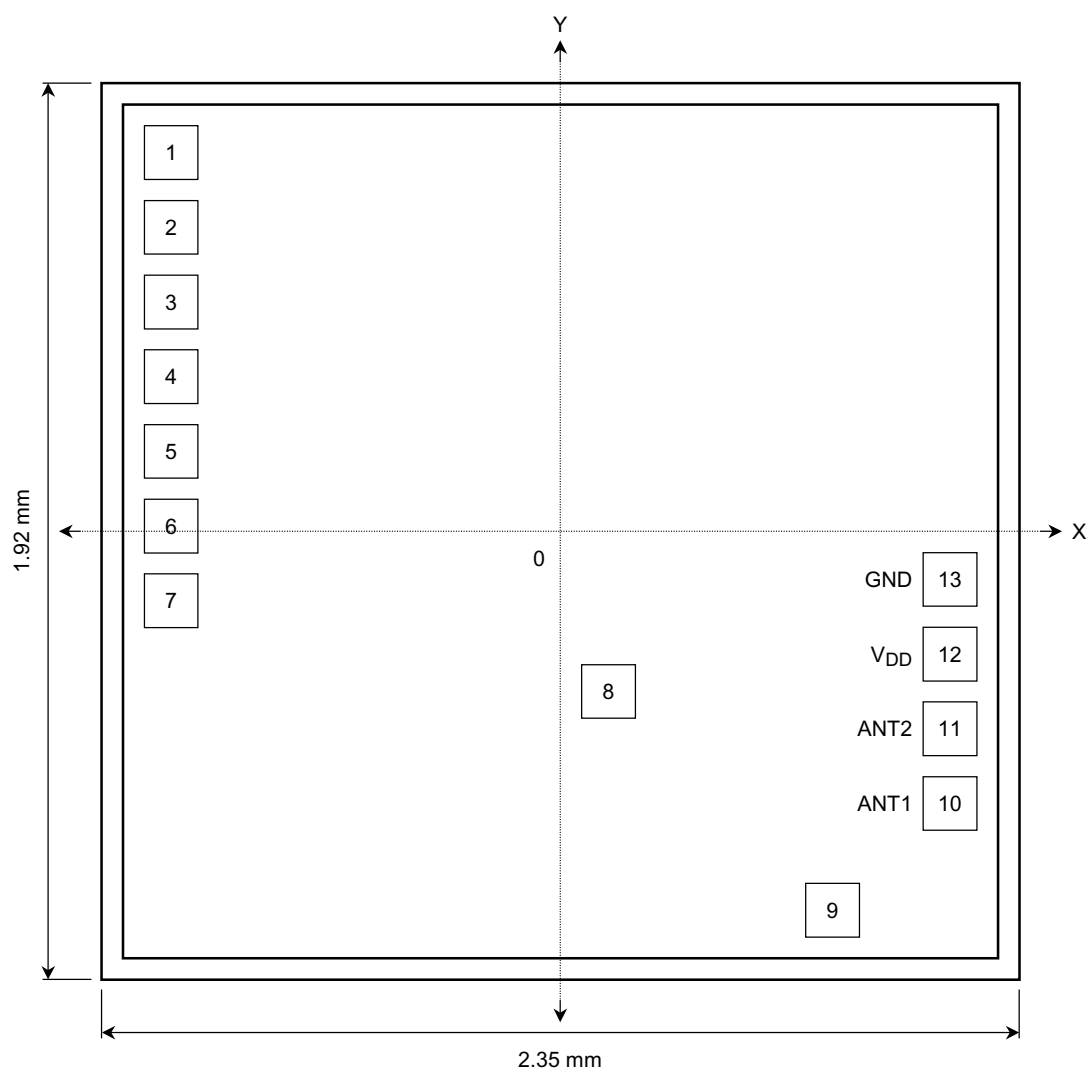- Supplied as chips or on wafer
  - Chip thickness: 175 μm (typ.)

System Block Diagram

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JT6N46S

Pad Allocation

1.92 mm

2.35 mm

Pad Coordinates

Pad No.	Pad Name	X-Coordinate (µm)	Y-Coordinate (µm)
1	Test pin	−1010	762
2	Test pin	−1010	622
3	Test pin	−1010	482
4	Test pin	−1010	342
5	Test pin	−1010	202
6	Test pin	−1010	62
7	Test pin	−1010	−78
8	Test pin	226	−363
9	ANAPSK0	770	−802
10	ANT1	1020	−466
11	ANT2	1020	−326
12	V_{DD}	1020	−186
13	GND	1020	−46

Note: Values for X-and Y-coordinates are pad center values.

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Pin Functions

Pin No.	Symbol	Function
10	ANT1	Rectifier diode input, antenna connection pin 1
11	ANT2	Rectifier diode input (carrier extraction input side), antenna connection pin 2
12	V_{DD}	Power supply for bridge circuit output, regulator voltage and internal circuits
13	GND	GND-internal circuit voltage reference
1~9	—	LSI test pins

LSI External Specifications

Parameter	Specifications
Power supply	Battery less-externally supplied by electromagnetic induction
Coupling type	Electromagnetic induction
Power feed frequency	100 kHz~200 kHz Note: An antenna and a capacitor are connected externally.
Communications method	Receive: PSK, Transmission: PSK (Reply carrier frequency is half the receive carrier frequency)
Transfer speed	7.8 kbps (when receive carrier frequency is 125 kHz) 1/16 of receive carrier frequency
Transfer method	Half-duplex start-stop synchronization transmission (with parity, 1 stop bit)
Memory size	1-Kbit E^2PROM (256 bits are used as security area.)
Write time	7 ms max (for batch write of 8 bytes)
Control circuit	Key checking and access level control by hardware • Incorporates two access keys (6-byte key and 2-byte status). • Using access keys, read-only or write/read privilege can be set independently for each 32-byte area (programmable security). • Block write in units of 8 bytes and block read in units of 16 bytes using an access key and physical address. • Controls multi-read using Multi-Read command.
Multi-read	10 reads/s (power feed frequency of 125 kHz when ID only is read)
Operating temperature	−20°C~+85°C

Functions and Specifications of the Core Block

The JT6N46S is comprised of the following: an RF analog block for power generation, carrier extraction and regulation, and a digital block for data modulation, demodulation and data processing an E^2PROM for data storage.

1. Analog Block

(1) Rectifier circuit
Receives radio wave via the (external) antenna circuit and generates DC power for operating internal circuits with full-wave rectification.

(2) Shunt regulator
Maintains the voltage generated by the rectifier circuit at a fixed voltage, 3.1 V (typ.).
The digital circuits and E^2PROM operate using the voltage supplied by the shunt regulator.
The shunt regulator also protects internal circuits from the effects of strong electric fields.

(3) Carrier extraction circuit
Shapes the PSK-processed received carrier in to a square wave which is then input to the logic circuits for demodulation.

(4) Oscillation circuit (OSC)
Generates a clock for the digital PLL in the logic block.
(Oscillation frequency range: 3 MHz~5 MHz)

(5) Transmission circuit (parallel transmitter circuit)
Modulates the reply using a resistance load from the ANT1 side of the rectifier circuit. The reply carrier frequency is half the receive carrier frequency.
At reply, the JT6N46S carries out modulation by halting all blocks except those needed for transmission and using all the power which would be dissipated by the halted blocks for reply.

(6) Voltage detector
Supports three types of voltage detector circuit for initializing the system and enabling/disabling E^2PROM writing. As a result, operation is always stable.

2. Digital Block

(1) Demodulator
Converts the PSK signal shaped by the carrier extraction circuit of the analog block into binary data.

(2) Digital PLL
Compares the frequency of the oscillator circuit in the analog block with the signal shaped by the carrier extraction circuit and generates a clock with a fixed frequency for operation of the entire digital block. Using the clock the internal LSI operates in synchronize with the carrier.

(3) Data processing
Processes data according to the commands received. Processes include parity check, E^2PROM write and read, and reset of the entire LSI.

(4) Security logic
Two keys can be set simultaneously using the security area allocated to the E^2PROM. Using the keys, write/read, read or no access can be set in units of 32-byte blocks (obtained by dividing E^2PROM memory area by four). (For example, with key A, read/write for a particular block can be set, while with key B, read/write for any blocks can be set.)

(5) Status reply
Replies to a command from the R/W consist of the status followed by data. The status represents, the internal status of the LSI to the R/W. If the LSI status is normal, status data 00H is inserted at the beginning (without any parity, start or end bits) followed by the data. If the LSI status is abnormal, no data follows and only the status indicating the abnormality is sent. The bit corresponding to each abnormality condition which has occurred is set to 1 in the status field.

(6) Multi-read
Multi-read is a function used for reading multiple RFIDs in the communications area using the same reader/writer (R/W). An RFID (LSI) generates a random number internally using the Multi-Read command transmitted by the R/W. The RFID replies using the response timing determined by the corresponding time slot. Thus, replies from the different RFIDs will not conflict, enabling data to be received properly by the R/W.
Note: Depending on the reading environment, the ability to read all the data may fluctuate . In some cases, some data may be left unread (since it cannot be undetected). Toshiba recommend the use of an additional chip with a detection function other than the multi-read function.

Electrical Characteristics

1. Ratings

Parameter	Symbol	Operating Rating	Unit
Input current (between ANT1 → GND → ANT2)	I_{ANT}	DC40	mA
Operating temperature range	T_{opr}	−20~+85	°C
Storage temperature range	T_{stg}	−50~+150	°C

*: Unless otherwise specified, the specifications are within the above operating temperature range.

2. DC Characteristics

Parameter	Symbol	Test Circuit	Description	Min	Typ.	Max	Unit
Minimum operating voltage 1	V_{DD} (min)	—	Minimum operating voltage excluding memory write (Voltage check pin is V_{DD}.)	—	2.0	2.2	V
Minimum operating voltage 2	V_{DD} (eew)	—	Minimum operating voltage including memory write (Voltage check pin is V_{DD}.)	—	2.7	2.9	V
Operating current dissipation 1	I_{DDopr1}	—	Current dissipation for operations excluding memory write (V_{DD} = 2.2 V)	—	350	450	µA
Operating current dissipation 2	I_{DDopr2}	—	Current dissipation for all operations including memory write (V_{DD} = 2.9 V)	—	400	500	µA

3. Operation Characteristics

Parameter	Symbol	Test Circuit	Description	Min	Typ.	Max	Unit
Receive carrier frequency	f_{crr}	—	Carrier frequency at which operation is possible	100	—	200	kHz
Reply carrier frequency	f_{psk}	—	Carrier frequency at reply	$f_{crr} \times 1/2$			kHz
Transfer rate	—	—	Transfer speed	$f_{crr} \times 1/16$			bps
Receive 1-bit frequency	—	—	Receiving carrier frequency per bit	16			Cycles
Reply 1-bit frequency	—	—	Reply carrier frequency per bit	8			Cycles
E^2PROM write time	t_{pw}	—	—	—	—	7	ms
E^2PROM overwrite	Ted	—	—	10^5	—	—	No. of times
E^2PROM data hold time	Pre	—	Ambient temperature: −20°C~+85°C	10	—	—	Years

Memory Map

Page No.	8-Byte Block	Page No.	8-Byte Block
00H	ATR data	01H	ATR data
02H	Key 0010	03H	Key 0101
04H	Any data	05H	Any data
06H	Any data	07H	Any data
08H	Any data	09H	Any data
0AH	Any data	0BH	Any data
0CH	Any data	0DH	Any data
0EH	Any data	0FH	Any data

Note 1: ATR: Answer to Reset. The LSI sends back the ATR data after receiving a reset command or self reset.

Note 2: Using the keys at 02H and 03H, access privileges can be set for the 32-byte blocks (enclosed by bold lines) from 04H to 1FH.

Note 3: Read is performed in units of 16 bytes from even-numbered addresses, 00H, 02H···0EH.

Note 4: Write to E^2PROM is performed in units of 8 bytes to addresses matching the page numbers above.

The advantage of using this LSI is that it can be supplied as a single LSI for RFID allowing the user to configure peripherals (e.g. antennae, and reader/writers) so as to develop the desired system. However, because the peripheral environment may be highly user-specific, incompatibilities between the LSI and the user-configured environment (communications failures) may occur. Please carry out sufficient research before using this LSI.