

14-STAGE BINARY RIPPLE COUNTER

FEATURES

- Output capability: standard
- ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4020 are high-speed Si-gate CMOS devices and are pin compatible with the "4020" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4020 are 14-stage binary ripple counters with a clock input (CP), an overriding asynchronous master reset input (MR) and twelve fully buffered parallel outputs (Q₀, Q₃ to Q₁₃). The counter is advanced on the HIGH-to-LOW transition of CP.

A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of CP.

Each counter stage is a static toggle flip-flop.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay CP to Q ₀ Q _n to Q _{n+1} MR to Q _n	C _L = 15 pF V _{CC} = 5 V	11	15	ns
			6	6	ns
f _{max}	maximum clock frequency		101	52	MHz
C _I	input capacitance		3.5	3.5	pF
CPD	power dissipation capacitance per package	notes 1 and 2	19	20	pF

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

Notes

1. CPD is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = CPD \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz C_L = output load capacitance in pF

f_o = output frequency in MHz V_{CC} = supply voltage in V

Σ(C_L × V_{CC}² × f_o) = sum of outputs

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

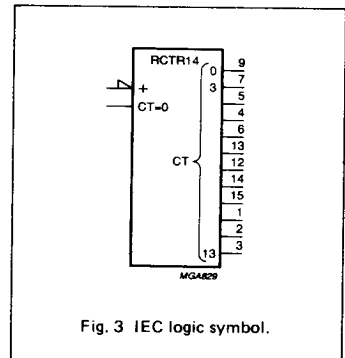
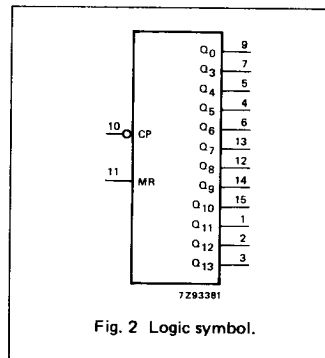
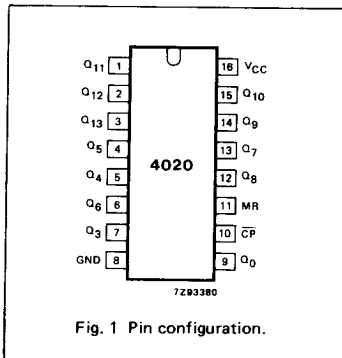
PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).

16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
9, 7, 5, 4, 6, 13, 12, 14, 15, 1, 2, 3	Q ₀ , Q ₃ to Q ₁₃	parallel outputs
8	GND	ground (0 V)
10	CP	clock input (HIGH-to-LOW, edge-triggered)
11	MR	master reset input (active HIGH)
16	V _{CC}	positive supply voltage



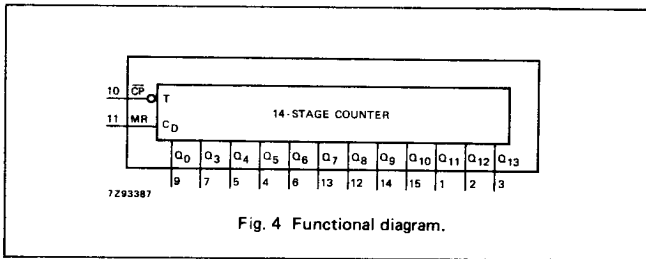


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS		OUTPUTS
\overline{CP}	MR	Q_0, Q_3 to Q_{13}
↑	L	no change
↓	L	count
X	H	L

H = HIGH voltage level
L = LOW voltage level
X = don't care
↑ = LOW-to-HIGH clock transition.
↓ = HIGH-to-LOW clock transition

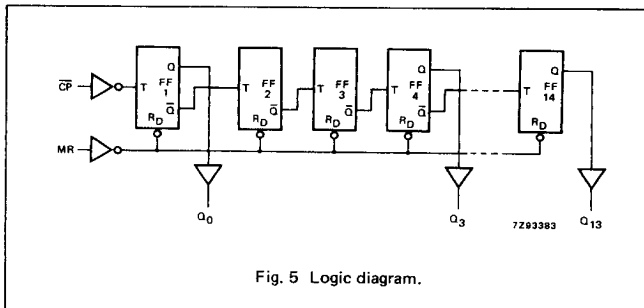


Fig. 5 Logic diagram.

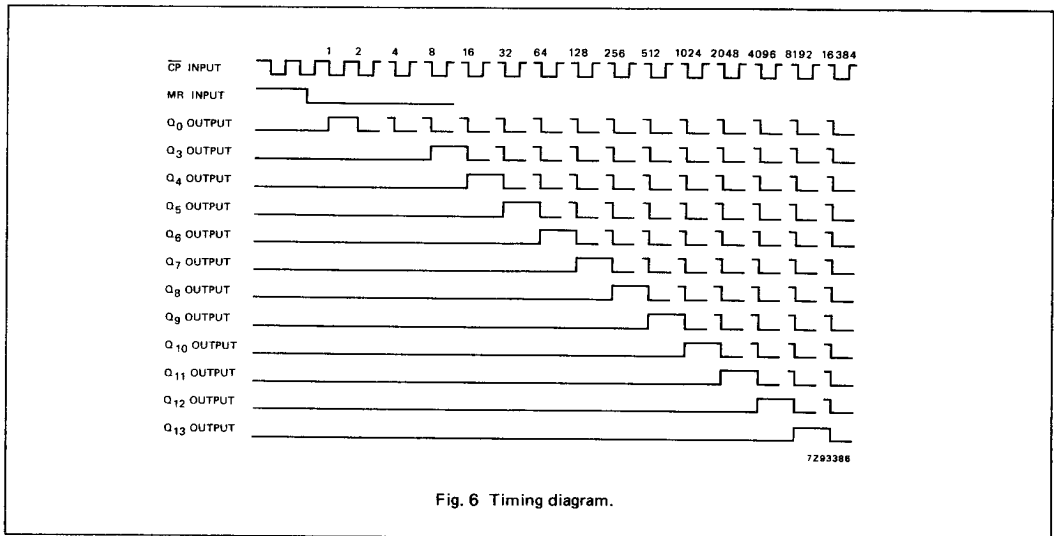


Fig. 6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.		max.		
t _{PHL} / t _{PLH}	propagation delay CP to Q ₀		39 14 11	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig. 7
t _{PHL} / t _{PLH}	propagation delay Q _n to Q _{n+1}		22 8 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7
t _{PHL}	propagation delay MR to Q _n		55 20 16	170 34 29		215 43 37		225 51 43	ns	2.0 4.5 6.0	Fig. 8
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7
t _W	clock pulse width HIGH or LOW	80 16 14	11 4 3		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t _W	master reset pulse width HIGH	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 8
t _{rem}	removal time MR to CP	50 10 9	6 2 2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig. 8
f _{max}	maximum clock pulse frequency	6.0 30 35	30 92 109		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 7

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

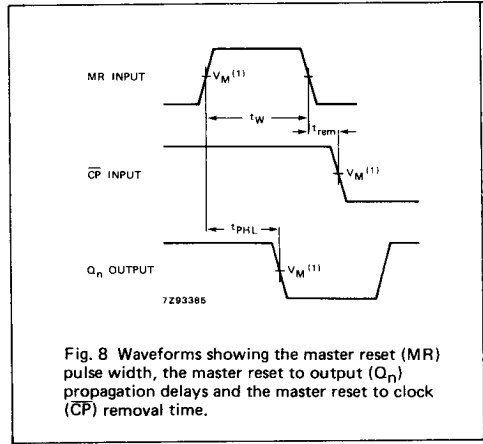
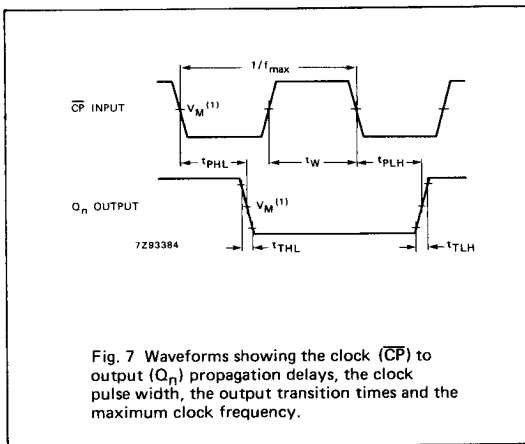
INPUT	UNIT LOAD COEFFICIENT
CP	0.85
MR	1.10

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HCT							V _{CC} V	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay CP to Q ₀		18	36		45		54	ns	4.5	Fig. 7
t _{PHL} / t _{PLH}	propagation delay Q _n to Q _{n+1}		8	15		19		22	ns	4.5	Fig. 7
t _{PHL}	propagation delay MR to Q _n		22	45		56		68	ns	4.5	Fig. 8
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 7
t _W	clock pulse width HIGH or LOW	20	7		25		30		ns	4.5	Fig. 7
t _W	master reset pulse width HIGH	20	8		25		30		ns	4.5	Fig. 8
t _{rem}	removal time MR to CP	10	2		13		15		ns	4.5	Fig. 8
f _{max}	maximum clock pulse frequency	25	47		20		17		MHz	4.5	Fig. 7

AC WAVEFORMS



Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
- HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.