T-46-13-09

*PRELIMINARY* **PLD20G10C**

CYPRESS SEMICONDUCTOR

# Generic 24-Pin PAL® Device

## Features

- **Ultra high speed supports today's and tomorrow's fastest microprocessors**
  - **$t_{PD}$ = 7.5 ns**
  - **$t_{SU}$ = 3 ns**
  - **$f_{MAX}$ = 105 MHz**
- **Reduced ground bounce and undershoot**
- **PLCC and LCC packages with additional $V_{CC}$ and $V_{SS}$ pins for lowest ground bounce**
- **Generic architecture to replace standard logic functions including: 20L10, 20L8, 20R8, 20R6, 20R4, 12L10, 14L8, 16L6, 18L4, 20L2, and 20V8**
- **Up to 22 inputs and 10 outputs for more logic power**
- **10 user-programmable output macrocells**
  - **— Output polarity control**
  - **— Registered or combinatorial operation**
  - **— Pin or product term output enable control**
- **Preload capability for flexible design and testability**
- **High reliability**
  - **— Proven Ti-W fuse technology**
  - **— AC and DC tested at the factory**
- **Security Fuse**

## Functional Description

The PLD20G10C is a generic 24-pin device that can be used in place of 24 PAL devices. Thus, the PLD20G10C provides significant design, inventory, and programming flexibility over dedicated 24-pin devices.

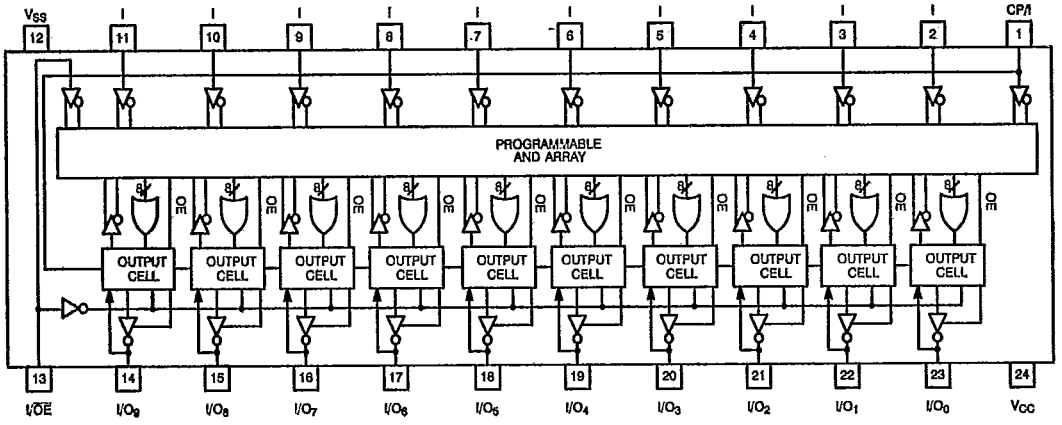
Using BiCMOS process and Ti-W fuses, the PLD20G10C implements the familiar sum-of-products (AND-OR) logic structure. It provides 12 dedicated input pins and 10 I/O pins (see Logic Block Diagram). By selecting each I/O pin as permanent or temporary input, up to 22 inputs can be achieved. Applications requiring up to 21 inputs and a single output, down to 12 inputs and 10 outputs can be realized. The output enable product term available on each I/O or a common pin controlled $\overline{OE}$ function allows this selection.

The PLD20G10C automatically resets on power-up. The Q output of all internal registers is set to a logic LOW and the $\overline{Q}$ output to a logic HIGH. In addition, the PRELOAD capability allows the registers to be set to any desired state during testing.

A security fuse is provided to prevent copying of the device fuse pattern.

PLDs

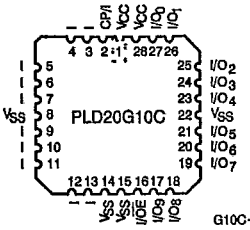
## Logic Block Diagram and PDIP (P)/CDIP (D) Pin Configuration




G10C-1

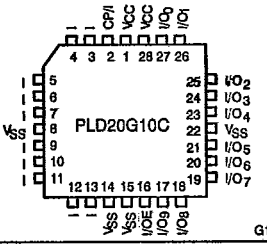
## Pin Configurations

LCC (L)
Top View




G10C-2

PLCC (J)/CLCC (Y)
Top View

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PAL is a registered trademark of Advanced Micro Devices.

## Selection Guide

| | | 20G10C–7 | 20G10C–10 | 20G10C–12 | 20G10C–15 |
|---|---|---|---|---|---|
| $I_{CC}$ (mA) | Commercial | 190 | 190 | 190 | |
| | Military | | 190 | 190 | 190 |
| $t_{PD}$ (ns) | Commercial | 7.5 | 10 | 12 | |
| | Military | | 10 | 12 | 15 |
| $t_S$ (ns) | Commercial | 3.0 | 3.6 | 4.5 | |
| | Military | | 3.6 | 4.5 | 7.5 |
| $t_{CO}$ (ns) | Commercial | 6.5 | 7.5 | 9.5 | |
| | Military | | 7.5 | 9.5 | 10 |
| $f_{MAX}$ (MHz) | Commercial | 105 | 90 | 71 | |
| | Military | | 90 | 71 | 57 |

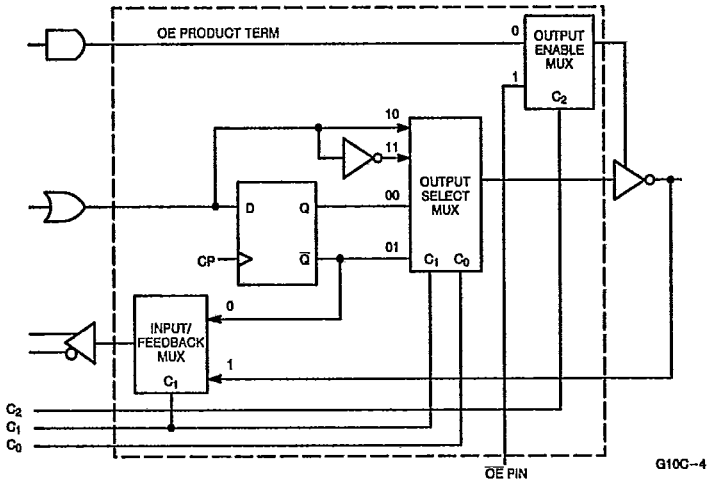
## Programmable Macrocell

The PLD20G10C has 10 programmable I/O macrocells (see Macrocell). Two fuses ($C_1$ and $C_0$) can be programmed to configure output in one of four ways. Accordingly, each output can be registered or combinatorial with an active HIGH or active LOW polarity. The feedback to the array is also from this output. An additional fuse ($C_2$) determines the source of the output enable signal. The signal can be generated either from the individual OE product term or from a common external $\overline{OE}$ pin.

## Programming

The PLD20G10C can be programmed using the QuickPro II™ programmer available from Cypress Semiconductor and also with Data I/O, Logical Devices, STAG, and other programmers. Please contact your local Cypress representative for further information.

## Macrocell



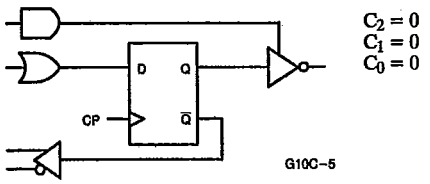

QuickPro II is a trademark of Cypress Semiconductor Corporation.

## Configuration Table

| Figure | $C_2$ | $C_1$ | $C_0$ | Configuration |
|---|---|---|---|---|
| 1 | 0 | 0 | 0 | Product Term OE/Registered/Active LOW |
| 2 | 0 | 0 | 1 | Product Term OE/Registered/Active HIGH |
| 5 | 0 | 1 | 0 | Product TermOE/Combinatorial/Active LOW |
| 6 | 0 | 1 | 1 | Product TermOE/Combinatorial/Active HIGH |
| 3 | 1 | 0 | 0 | Pin $\overline{OE}$/Registered/Active LOW |
| 4 | 1 | 0 | 1 | Pin $\overline{OE}$/Registered/Active HIGH |
| 7 | 1 | 1 | 0 | Pin $\overline{OE}$/Combinatorial/Active LOW |
| 8 | 1 | 1 | 1 | Pin $\overline{OE}$/Combinatorial/Active HIGH |

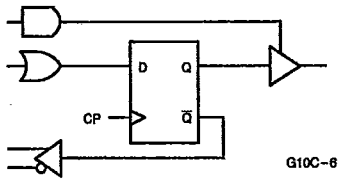


## Registered Output Configurations



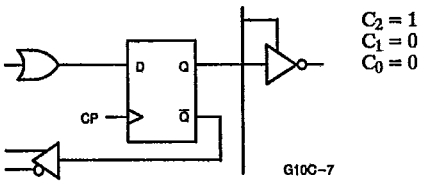

$C_2 = 0$
$C_1 = 0$
$C_0 = 0$

**Figure 1. Product Term OE/Active LOW**



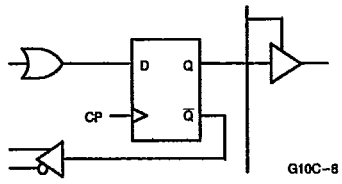

$C_2 = 0$
$C_1 = 0$
$C_0 = 1$

**Figure 2. Product Term OE/Active HIGH**




$C_2 = 1$
$C_1 = 0$
$C_0 = 0$

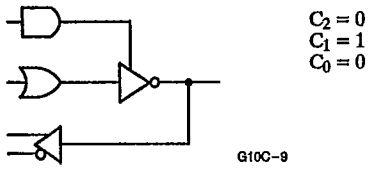
**Figure 3. Pin $\overline{OE}$/Active LOW**




$C_2 = 1$
$C_1 = 0$
$C_0 = 1$

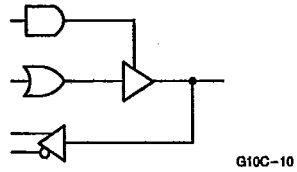
**Figure 4. Pin $\overline{OE}$/Active HIGH**

## Combinatorial Output Configurations[1]



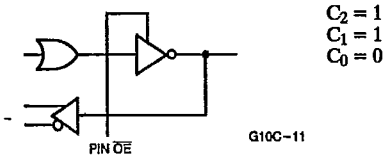

$C_2 = 0$
$C_1 = 1$
$C_0 = 0$

**Figure 5. Product Term OE/Active LOW**



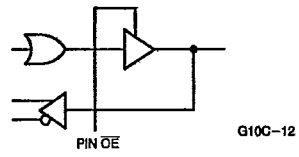

$C_2 = 0$
$C_1 = 1$
$C_0 = 1$

**Figure 6. Product Term OE/Active HIGH**




$C_2 = 1$
$C_1 = 1$
$C_0 = 0$

**Figure 7. Pin $\overline{OE}$/Active LOW**




$C_2 = 1$
$C_1 = 1$
$C_0 = 1$

**Figure 8. Pin $\overline{OE}$/Active HIGH**

**Notes:**
1. Bidirectional I/O configurations are possible only when the combinatorial output option is selected.

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## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C

Ambient Temperature with Power Applied ..... – 55°C to +125°C

Supply Voltage to Ground Potential ..... – 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... – 0.5V to $V_{CC}$

DC Input Voltage ..... – 0.5V to $V_{CC}$

DC Input Current ..... – 30 mA to +5 mA (except during programming)

DC Program Voltage ..... 10V

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 5V ± 5% |
| Military[2] | – 55°C to +125°C | 4.75V to 5.5V |

## DC Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | | | Min. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = – 3.2 mA | Com'l | 2.4 | | V |
| | | | $I_{OH}$ = – 2 mA | Mil | | | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 16 mA | Com'l | | 0.5 | V |
| | | | $I_{OL}$ = 12 mA | Mil | | | |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for All Inputs[3] | | | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for All Inputs[3] | | | | 0.8 | V |
| $I_{IX}$ | Input Leakage Current | $V_{SS} \le V_{IN} \le 2.7V$, $V_{CC}$ = Max. | | | – 250 | 50 | µA |
| $I_I$ | Maximum Input Current | $V_{IN}$ = $V_{CC}$, $V_{CC}$ = Max. | | Com'l | | 100 | µA |
| | | | | Mil | | 250 | |
| $I_{OZ}$ | Output Leakage Current | $V_{CC}$ = Max., $V_{SS} \le V_{OUT} \le V_{CC}$ | | | – 100 | 100 | µA |
| $I_{SC}$ | Output Short Circuit Current | $V_{CC}$ = Max., $V_{OUT}$ = 0.5V[4] | | | – 30 | – 120 | mA |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = Max., $V_{IN}$ = GND, Outputs Open | | Com'l | | 190 | mA |
| | | | | Mil | | 190 | |

**Notes:**

2. $T_A$ is the "instant on" case temperature.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. $V_{OUT}$ = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

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## Switching Characteristics PLD20G10C[5]

| Parameters | Description | -7 | | -10 | | -12 | | -15 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| $t_{PD}$ | Input to Output Propagation Delay[6] | 2 | 7.5 | 2 | 10 | 2 | 12 | 2 | 15 | ns |
| $t_{EA}$ | Input to Output Enable Delay | 2 | 7.5 | 2 | 10 | 2 | 12 | 2 | 15 | ns |
| $t_{ER}$ | Input to Output Disable Delay[7] | 2 | 7.5 | 2 | 10 | 2 | 12 | 2 | 15 | ns |
| $t_{PZX}$ | $\overline{OE}$ Input to Output Enable Delay | 2 | 7.5 | 2 | 10 | 2 | 12 | 2 | 15 | ns |
| $t_{PXZ}$ | $\overline{OE}$ Input to Output Disable Delay | 2 | 7.5 | 2 | 10 | 2 | 12 | 2 | 15 | ns |
| $t_{CO}$ | Clock to Output Delay[6] | 1 | 6.5 | 1 | 7.5 | 1 | 9.5 | 1 | 10 | ns |
| $t_S$ | Input or Feedback Set-Up Time | 3 | | 3.6 | | 4.5 | | 7.5 | | ns |
| $t_H$ | Input Hold Time | 0 | | 0 | | 0 | | 0 | | ns |
| $t_P$ | External Clock Period ($t_{CO} + t_S$) | 9 | | 11.1 | | 14 | | 17.5 | | ns |
| $t_{WH}$ | Clock Width HIGH[8] | 3 | | 3 | | 3 | | 6 | | ns |
| $t_{WL}$ | Clock Width LOW[8] | 3 | | 3 | | 3 | | 6 | | ns |
| $f_{MAX1}$ | External Maximum Frequency ($1/(t_{CO} + t_S)$)[9] | 105 | | 90 | | 71 | | 57 | | MHz |
| $f_{MAX2}$ | Data Path Maximum Frequency ($1/(t_{WH} + t_{WL})$)[8, 10] | 166 | | 166 | | 166 | | 83 | | MHz |
| $f_{MAX3}$ | Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[11] | 133 | | 100 | | 83 | | 66 | | MHz |
| $t_{CF}$ | Register Clock to Feedback Input[12] | | 4.5 | | 6.4 | | 7.5 | | 7.5 | ns |
| $t_{PR}$ | Power-Up Reset Time[13] | 1 | | 1 | | 1 | | 1 | | µs |

## Capacitance[8]

| Parameters | Description | Max. | Units |
|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 8 | pF |
| $C_{OUT}$ | Output Capacitance | 10 | pF |

**Notes:**

5. AC test load used for all parameters except where noted.
6. This specification is guaranteed for all device outputs changing state in a given access cycle.
7. This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below $V_{OH}$ min. or a previous LOW level has risen to 0.5 volts above $V_{OL}$ max.
8. Tested initially and after any design or process changes that may affect these parameters.
9. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
10. This specification indicates the guaranteed maximum frequency at which an individual output register can be cycled.
11. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal only feedback can operate. This parameter is tested periodically by sampling production product.
12. This parameter is calculated from the clock period at $f_{MAX}$ internal ($f_{MAX3}$) as measured (see Note 11) minus $t_S$.
13. The registers in the PLD20G10C have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic LOW state. The output state will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in $V_{CC}$ must be monotonic and the timing constraints depicted in power-up reset waveforms must be satisfied.

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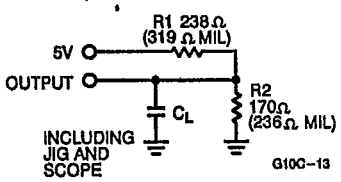
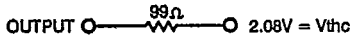
## AC Test Loads and Waveforms



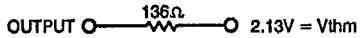

| $C_L$[14] | Package |
|---|---|
| 15 pF | P/D |
| 50 pF | J/K/L/Y |

Equivalent to: THÉVENIN EQUIVALENT

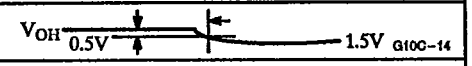
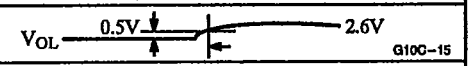
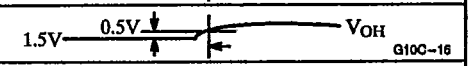
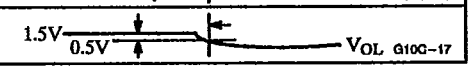



**Commercial**

Equivalent to: THÉVENIN EQUIVALENT



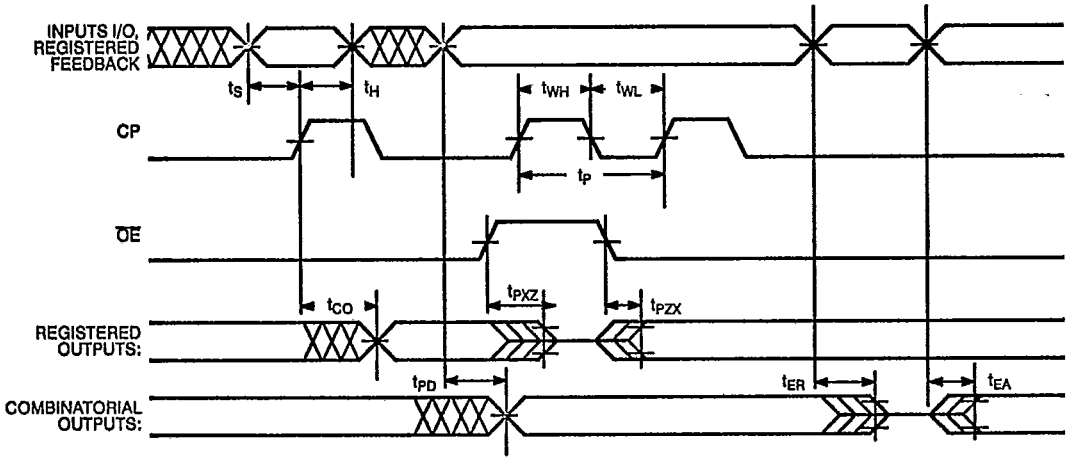

**Military**

| Parameter | $V_{th}$ | Output Waveform—Measurement Level |
|---|---|---|
| $t_{ER}$ (–), $t_{PHZ}$ | 1.5V |  |
| $t_{ER}$ (+), $t_{PLZ}$ | 2.6V |  |
| $t_{EA}$ (+), $t_{PZH}$ | 1.5V |  |
| $t_{EA}$ (–), $t_{PZL}$ | 1.5V |  |

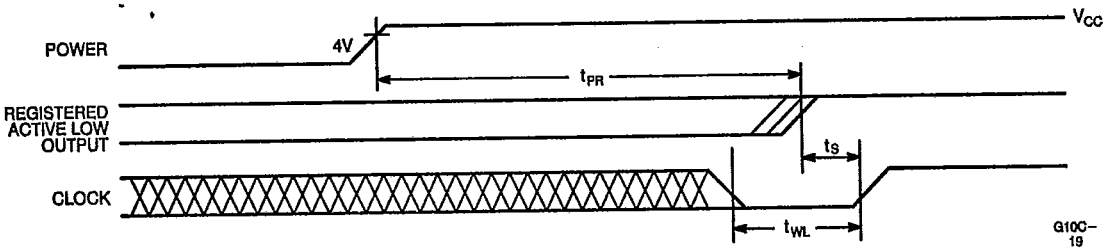


**Notes:**
14. $C_L$ = 5 pF for $t_{ER}$ and $t_{PXZ}$ measurements for all packages.

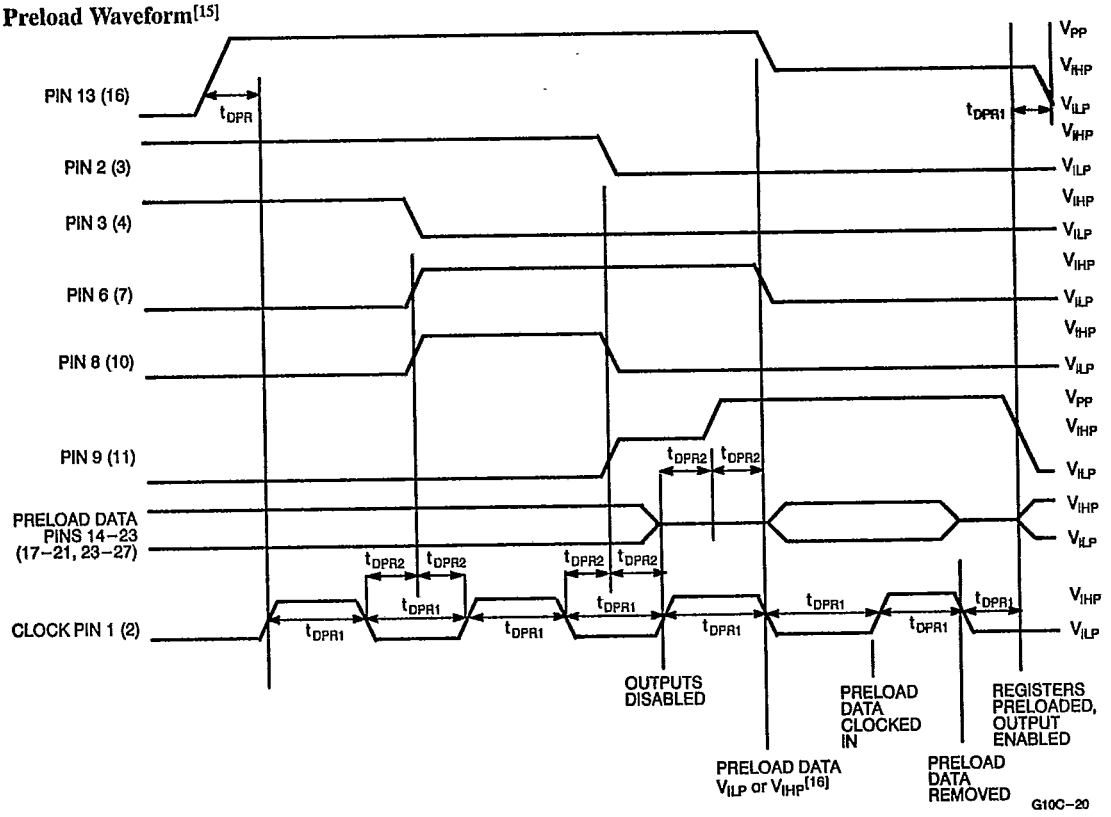
## Switching Waveform



**Power-Up Reset Waveform**[13]




**Preload Waveform**[15]




**Notes:**

15. Pins 4 (5), 5 (6), 7 (9) at $V_{ILP}$; Pins 10 (12) and 11 (13) at $V_{IHP}$; $V_{CC}$ (Pin 24 (1 and 28)) at $V_{CCP}$.
16. Pins 2–8 (3–7, 9, 10), 10 (12), 11 (13) can be set at $V_{IHP}$ or $V_{ILP}$ to insure asynchronous reset is not active.

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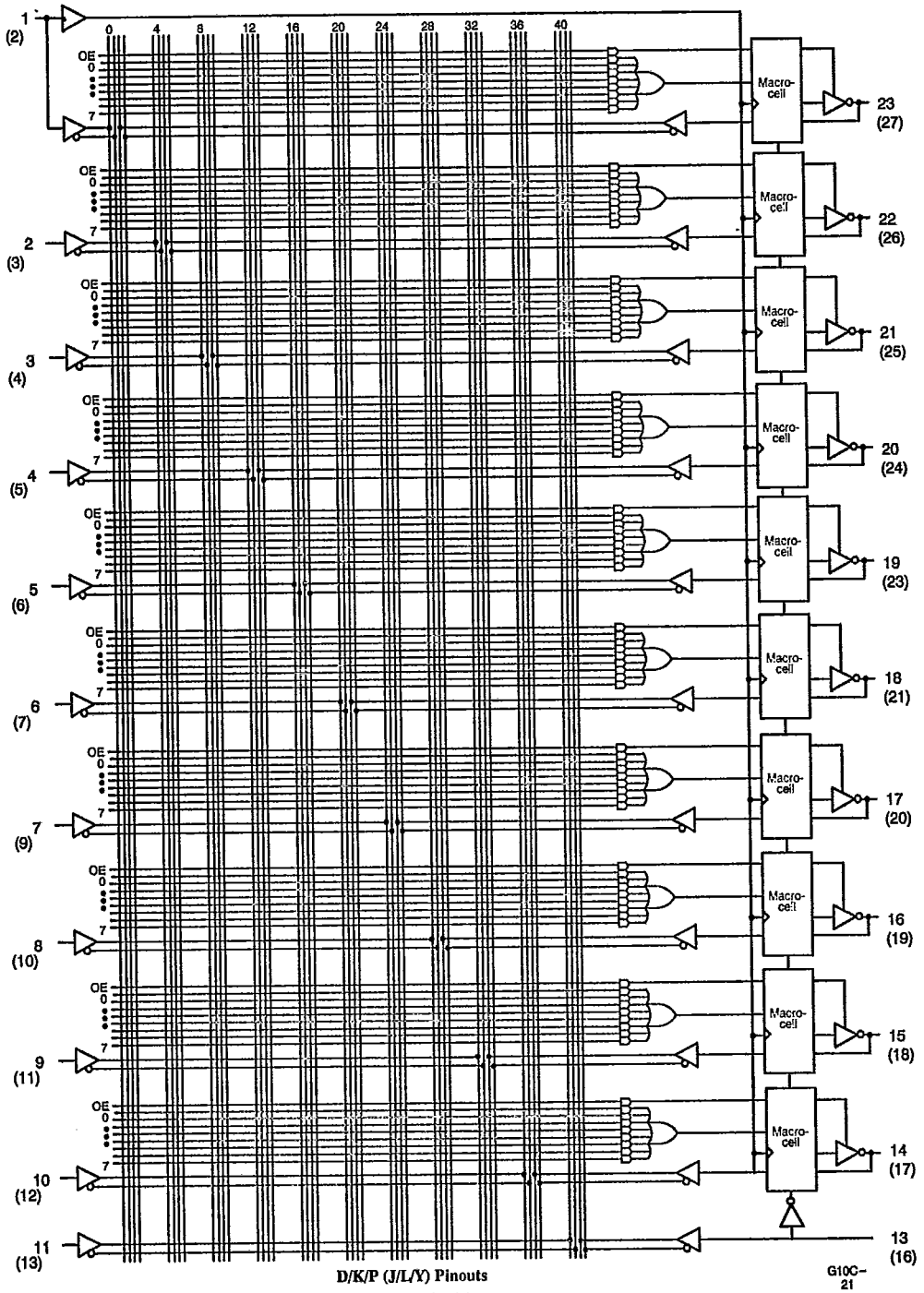
### D/K/P (J/L/Y) Pinouts

| Forced level on register pin during preload | Register Q output state after preload |
|---|---|
| $V_{IHP}$ | HIGH |
| $V_{ILP}$ | LOW |

| Name | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{PP}$ | Programming Voltage | 9.25 | 9.75 | V |
| $t_{DPR1}$ | Delay for Preload | 1 | | µs |
| $t_{DPR2}$ | Delay for Preload | 0.5 | | µs |
| $V_{ILP}$ | Input LOW Voltage | 0 | 0.4 | V |
| $V_{IHP}$ | Input HIGH Voltage | 3 | 4.75 | V |
| $V_{CCP}$ | $V_{CC}$ for Preload | 4.75 | 5.25 | V |

**Functional Logic Diagram for PLD20G10C** T-46-19-09

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D/K/P (J/L/Y) Pinouts

## Ordering Information

| $I_{CC}$ (mA) | $t_{PD}$ (ns) | $f_{MAX}$ (MHz) | Ordering Code | Package Type | Operating Range |
|---|---|---|---|---|---|
| 190 | 7.5 | 105 | PLD20G10C–7DC | D14 | Commercial |
| | | | PLD20G10C–7JC | J64 | |
| | | | PLD20G10C–7PC | P13 | |
| | | | PLD20G10C–7YC | Y64 | |
| | 10 | 90 | PLD20G10C–10DC | D14 | Commercial |
| | | | PLD20G10C–10JC | J64 | |
| | | | PLD20G10C–10PC | P13 | |
| | | | PLD20G10C–10YC | Y64 | |
| | | | PLD20G10C–10DMB | D14 | Military |
| | | | PLD20G10C–10KMB | K73 | |
| | | | PLD20G10C–10LMB | L64 | |
| | | | PLD20G10C–10YMB | Y64 | |
| | 12 | 71 | PLD20G10C–12DC | D14 | Commercial |
| | | | PLD20G10C–12JC | J64 | |
| | | | PLD20G10C–12PC | P13 | |
| | | | PLD20G10C–12YC | Y64 | |
| | | | PLD20G10C–12DMB | D14 | Military |
| | | | PLD20G10C–12KMB | K73 | |
| | | | PLD20G10C–12LMB | L64 | |
| | | | PLD20G10C–12YMB | Y64 | |
| | 15 | 57 | PLD20G10C–15DMB | D14 | Military |
| | | | PLD20G10C–15KMB | K73 | |
| | | | PLD20G10C–15LMB | L64 | |
| | | | PLD20G10C–15YMB | Y64 | |

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

### DC Characteristerics

| Parameters | Subgroups |
|---|---|
| $V_{OH}$ | 1, 2, 3 |
| $V_{OL}$ | 1, 2, 3 |
| $V_{IH}$ | 1, 2, 3 |
| $V_{IL}$ | 1, 2, 3 |
| $I_{IX}$ | 1, 2, 3 |
| $I_{OZ}$ | 1, 2, 3 |
| $I_{CC}$ | 1, 2, 3 |

### Switching Characteristics

| Parameters | Subgroups |
|---|---|
| $t_{PD}$ | 7, 8, 9, 10, 11 |
| $t_{CO}$ | 7, 8, 9, 10, 11 |
| $t_S$ | 7, 8, 9, 10, 11 |
| $t_H$ | 7, 8, 9, 10, 11 |

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