32-Bit, 300 MSPS Phase Accumulator for DDS

AD9950

FEATURES
300 MSPS Clock Rate
32-Bit Frequency Resolution
Low Power: 1.5 W
On-Board Quad Logic
16- or 32-Bit Bus Compatible

APPLICATIONS
Frequency Synthesizers
Waveform Generators
Frequency Hopping Systems
Communications and Radar Receivers

GENERAL DESCRIPTION

The AD9950 is a 32-bit, 300 MSPS phase accumulator for direct digital synthesis (DDS) applications. The twelve most significant bits (MSBs) of the accumulator are provided to address an external phase-to-amplitude conversion table for waveform synthesis.

Frequency control signals are TTL compatible, and the internal accumulator can operate at rates up to 300 MSPS because of the high speed bipolar process used in fabricating the device. Output phase data is ECL compatible and can be interfaced with either ROM or RAM. An external look-up table can contain data to generate standard functions such as sines, cosines, etc.

On-board quadrature logic reduces the amount of external memory required to implement the phase-to-amplitude conversions in applications which generate periodic waveforms symmetrical about their 90° phase points.

The AD9950KJ is packaged in a 68-pin J-leaded ceramic chip carrier for a commercial temperature range of 0°C to +70°C; the model AD9950TJ is available for military applications with a temperature range of −55°C to +125°C in the same package. Contact the factory for information on devices meeting the requirements of MIL-STD-883.

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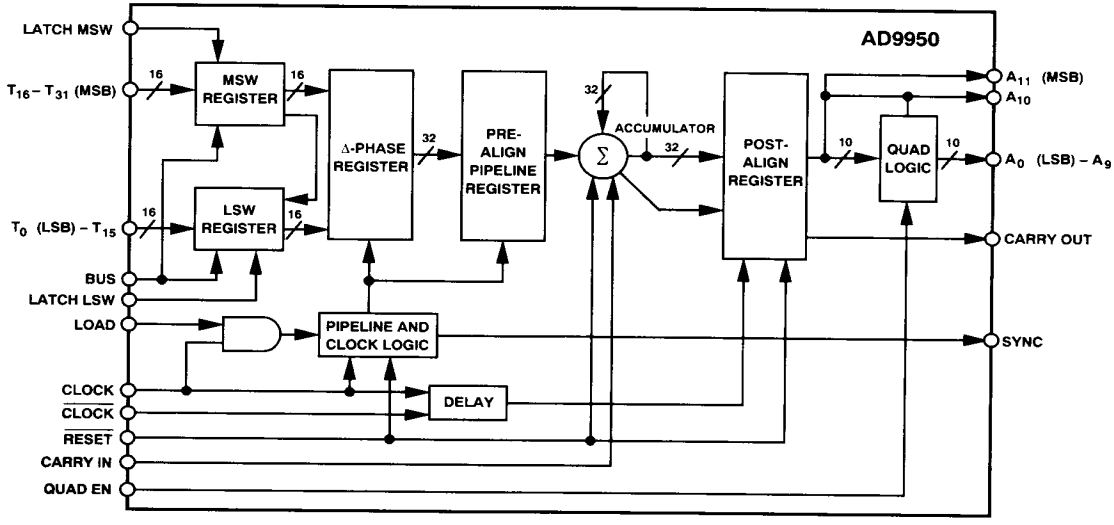
AD9950 DDS PHASE ACCUMULATOR BLOCK DIAGRAM



AD9950—SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($\pm V_S$) . . . . . ±7 V
TTL Inputs . . . . . $+V_S$ to −0.5 V
ECL Inputs . . . . . 0 V to $-V_S$
Operating Temperature Range
AD9950KJ . . . . . 0°C to +70°C
AD9950TJ . . . . . −55°C to +125°C
Storage Temperature
AD9950KJ . . . . . −65°C to +150°C
AD9950TJ . . . . . −65°C to +150°C
Junction Temperature[1]
AD9950KJ . . . . . +175°C
AD9950TJ . . . . . +175°C
Lead Soldering Temperature (10 sec) . . . . . +300°C

DC ELECTRICAL CHARACTERISTICS (unless otherwise noted, $+V_S = +5$ V; $-V_S = -5.2$ V)

Parameter	Temp	Test Level	AD9950KJ Min	AD9950KJ Typ	AD9950KJ Max	AD9950TJ Min	AD9950TJ Typ	AD9950TJ Max	Units
ECL INPUTS									
Logic "1" Voltage	Full	VI	−1.1			−1.1			V
Logic "0" Voltage	Full	VI			−1.5			−1.5	V
Logic "1" Current	Full	VI			200			200	µA
Logic "0" Current	Full	VI			200			200	µA
Input Capacitance	+25°C	V		2			2		pF
ECL OUTPUTS									
Logic "1" Voltage	Full	VI	−1.1			−1.1			V
Logic "0" Voltage	Full	VI			−1.5			−1.5	V
TTL INPUTS									
Logic "1" Voltage	Full	VI	+2			+2			V
Logic "0" Voltage	Full	VI			+0.8			−0.8	V
Logic "1" Current	Full	VI			300			300	µA
Logic "0" Current	Full	VI			500			500	µA
Input Capacitance	+25°C	V		2			2		pF
POWER SUPPLIES									
$-V_S$ Supply Current	+25°C	I		288	350		288	350	mA
	Full	VI			375			375	mA
$+V_S$ Supply Current	+25°C	I		11	14		11	14	mA
	Full	VI			16			16	mA
Nominal Power Dissipation	+25°C	V		1.5			1.5		W

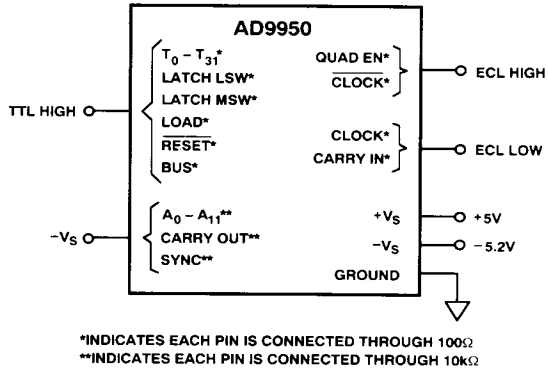
AC ELECTRICAL CHARACTERISTICS (unless otherwise noted, $+V_S = +5$ V; $-V_S = -5.2$ V)

Parameter	Temp	Test Level	AD9950KJ Min	AD9950KJ Typ	AD9950KJ Max	AD9950TJ Min	AD9950TJ Typ	AD9950TJ Max	Units
ECL INPUTS									
CLOCK Update Rate[2]	+25°C	I	250	300		250	300		MSPS
	Full	V		250			250		MSPS
CLOCK Pulse Width HIGH	+25°C	IV	2.0	1.7		2.0	1.7		ns
	Full	V		2.0			2.0		ns
CLOCK Pulse Width LOW	+25°C	IV	2.0	1		2.0	1		ns
	Full	V		2.0			2.0		ns
CARRY IN Set-Up Time[3]	+25°C	IV	0.2	0		0.2	0		ns
	Full	V		0.5			0.5		ns
CARRY IN Hold[3]	+25°C	IV	2.0	1.25		2.0	1.25		ns
	Full	V		1.5			1.5		ns
ECL OUTPUTS[4]									
Rise Time[5]	+25°C	IV		1	1.6		1	1.6	ns
	Full	V		1.2			1.2		ns
Fall Time	+25°C	IV		1	1.6		1	1.6	ns
	Full	V		1.2			1.2		ns
Data Skew[6]	+25°C	V		0.4			0.4		ns
Output Capacitance	+25°C	V		2			2		pF
A_0–A_{11} Delay[3]	+25°C	IV	3.7	4.5	5.3	3.7	4.5	5.3	ns
	Full	V		5.0			5.0		ns
SYNC Propagation Delay[3]	+25°C	IV	3.5	4.2	5.0	3.5	4.2	5.0	ns
	Full	V		4.6			4.6		ns
CARRY OUT Propagation Delay[3]	+25°C	IV	3.6	4.4	5.2	3.6	4.4	5.2	ns

Parameter	Temp	Test Level	AD9950KJ Min	AD9950KJ Typ	AD9950KJ Max	AD9950TJ Min	AD9950TJ Typ	AD9950TJ Max	Units
TTL INPUTS—Bus Mode									
T_{16}–T_{31} Set-Up Time[7]	+25°C	IV	5.0	3.8		5.0	3.8		ns
(t_{TSU})	Full	V		4.3			4.3		ns
T_{16}–T_{31} Hold Time[7]	+25°C	IV	0.5	−0.5		0.5	−0.5		ns
(t_{TH})	Full	V		0.5			0.5		ns
LOAD Set-Up Time[3]	+25°C	IV	0.75	0.2		0.75	0.2		ns
(t_{LSU})	Full	V		0.5			0.5		ns
LOAD Hold Time[3]	+25°C	IV	0.2	0		0.2	0		ns
(t_{LH})	Full	V		0.2			0.2		ns
TTL INPUTS—Parallel Mode									
T_1–T_{31} Set-Up Time[3]	+25°C	IV	3.0	1.5		3.0	1.5		ns
(t_{TSU})	Full	V		2.5			2.5		ns
T_1–T_{31} Hold Time[3]	+25°C	IV	0.5	−0.5		0.5	−0.5		ns
(t_{TH})	Full	V		1.0			1.0		ns
LOAD Set-Up Time[3]	+25°C	IV	0.75	0.2		0.75	0.2		ns
(t_{LSU})	Full	V		0.5			0.5		ns
LOAD Hold Time[3]	+25°C	IV	0.2	0		0.2	0		ns
(t_{LH})	Full	V		0.2			0.2		ns
RESET									
Minimum Pulse Width	+25°C	IV	2.5	1.6		2.5	1.6		ns
(Low)	Full	V		2			2		ns

NOTES
[1]Typical thermal impedances (part in socket): θ_{JA} = 42°C/W; θ_{JC} = 11°C/W.
[2]Minimum specification with 50% duty cycle on clock. Typical can be achieved with duty cycle adjustment to 70% HIGH.
[3]Referenced to CLOCK/$\overline{\text{CLOCK}}$ differential signal crossing point (CLOCK rising; $\overline{\text{CLOCK}}$ falling).
[4]ECL outputs terminated to −2 V through 100 Ω.
[5]Measured as the 10% to 90% transition time.
[6]Measured as the worst case difference between the 50% points of both falling and rising edges.
[7]Referenced to the 50% point of the rising edge of LATCH MSW or LATCH LSW.
Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS
Test Level
I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.



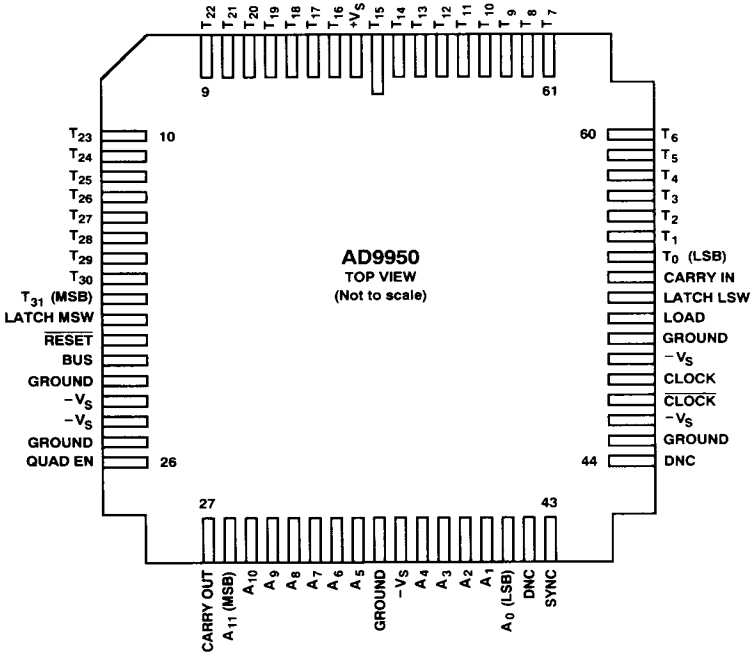
AD9950 Burn-In Connections

AD9950 TRUTH TABLE
BUS MODE
(Data Inputs = T_{16}–T_{31})

BUS	$\overline{\text{RESET}}$	LATCH MSW	LATCH LSW	LOAD	OPERATION
1	1	0	1	0	Transfers Most Significant 16-Bit Tuning Word into MSW Register
1	1	1	0	0	Transfers Least Significant 16-Bit Tuning Word into LSW Register
1	1	1	1	1	Load MSW and LSW Registers (32 Bits) Into Δ-Phase Register on Next CLOCK Cycle
X	0	X	X	X	Asynchronous Reset

PARALLEL MODE
(Data Inputs = T_0–T_{31})

BUS	$\overline{\text{RESET}}$	LATCH MSW	LATCH LSW	LOAD	OPERATION
0	1	X	X	1	Load 32-Bit Tuning Word into Δ-Phase Register on Next CLOCK Cycle
X	0	X	X	X	Asynchronous Reset



AD9950 Pin Designations

AD9950 PIN DESCRIPTIONS

Pin	Name	Function
1, 3–18 and 54–68	T_0–T_{31}	TTL-compatible word that determines the phase step of the accumulator. The tuning word can be loaded in parallel (32 bits) or bus (16 bits) mode. In bus mode, the two 16-bit words are loaded into the MSW and LSW registers through T_{16}–T_{31}.
2	$+V_S$	Positive power supply, nominally +5 V.
19	LATCH MSW	TTL-compatible latch command for the 16 most significant bits (MSBs) of the tuning word. In parallel mode, the MSW register is always transparent. In bus mode, the MSW register is transparent when LATCH MSW is LOW.
20	$\overline{\text{RESET}}$	TTL-compatible asynchronous reset command. See text.
21	BUS	TTL-compatible control pin. Logic HIGH enables the MSW and LSW registers, and multiplexes the data from T_{16}–T_{31} into both registers. Logic LOW enables the parallel load mode; the MSW and LSW registers are transparent, and T_0–T_{31} are latched directly into the delta-phase register by the LOAD signal.
22, 25, 35, 45, 50	GROUND	Ground return for the device. Ground for the ECL output stages is Pin 35.
23, 24, 36, 46, 49	$-V_S$	Negative power supply, nominally −5.2 V. Power for the ECL output stages is from Pin 36.
26	QUAD EN	ECL-compatible control pin. Logic HIGH enables the quadrature logic, which reduces the amount of memory required to implement the external phase-to-amplitude look-up table. The quadrature logic is used when generating waveforms symmetrical about the 90° and 180° phase points (i.e., a sine wave). See text.
27	CARRY OUT	ECL-compatible overflow flag. Logic HIGH at this pin indicates an overflow condition exists for the output data during that clock cycle. For applications in which two AD9950 units are cascaded to obtain 64 bits of phase resolution, CARRY OUT of the lower-order accumulator should be connected to CARRY IN of the higher-order accumulator.
47	$\overline{\text{CLOCK}}$	ECL-compatible input; should be driven differentially with CLOCK.
48	CLOCK	ECL-compatible input; should be driven differentially with $\overline{\text{CLOCK}}$. The contents of the delta-phase register are added to the output register after each rising edge of the CLOCK input.
28–34 and 37–41	A_0–A_{11}	Twelve bits of ECL-compatible output data from the phase accumulator output register.
42, 44	DNC	Internal test points. Do not connect; let pins float.
43	SYNC	ECL-compatible output signal. SYNC will go HIGH for one clock cycle following the prealignment of new tuning data. SYNC serves as a flag to indicate the completion of the minimum period for loading new data. See Theory Section.
51	LOAD	TTL-compatible latch control for the delta-phase register. Data is transferred into the delta-phase register on the first rising edge of CLOCK after LOAD has gone HIGH.
52	LATCH LSW	TTL-compatible latch command for the 16 least significant (LSBs) of the tuning word. In parallel mode, the LSW register is always transparent. In bus mode, the LSW register is transparent when LATCH LSW is LOW.
53	CARRY IN	ECL-compatible input. The effective value of the tuning word is increased by one LSB when CARRY IN is HIGH. For applications in which two AD9950 units are cascaded to obtain 64 bits of phase resolution, CARRY OUT of the lower-order accumulator should be connected to CARRY IN of the higher-order accumulator.

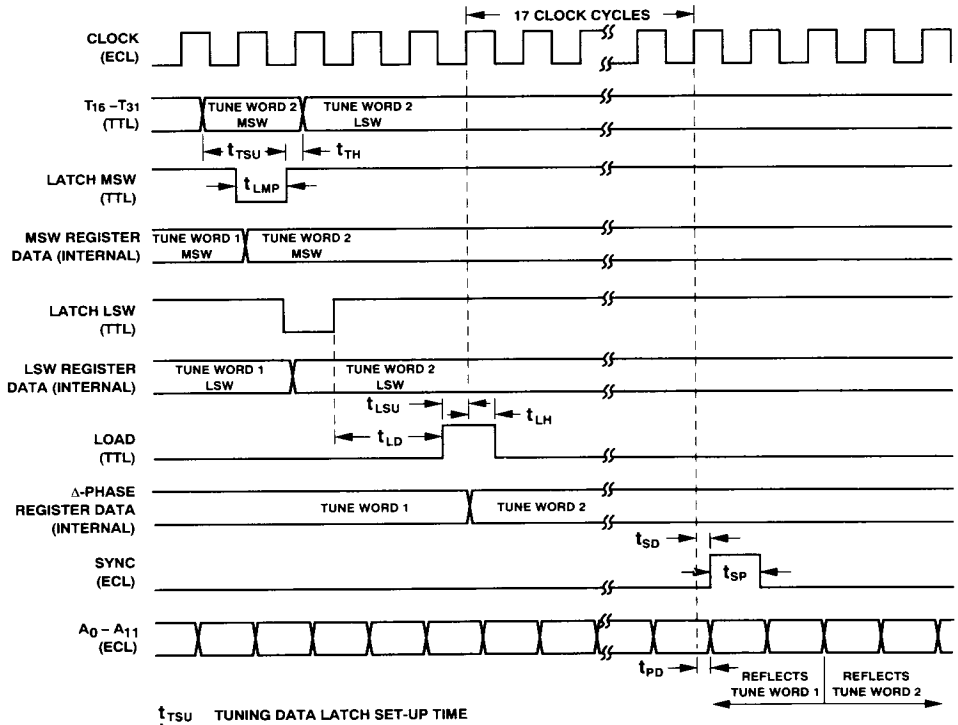
AD9950 THEORY OF OPERATION

Refer to the block diagram of the AD9950 on the first page of this data sheet.

The heart of the AD9950 is a 32-bit carry-save adder accumulator, implemented with 2-bit ripple-carry adder cores. The 32-bit input for this adder is stored in the Δ-phase registers.

Registers for the most significant word (MSW) and least significant word (LSW) are controlled by the BUS command. In the parallel mode (BUS @ logic LOW), these registers are transparent, and serve only to buffer the tuning data. In the bus mode (BUS @ logic HIGH), they operate as level-triggered latches; and data is strobed into the registers on the leading edge of LATCH MSW or LATCH LSW. In the bus mode, data for both registers is multiplexed through T_{16}–T_{31}.

In either mode, new data is strobed into the Δ-Phase register by the rising edge of the first clock cycle after the LOAD command goes high. These and other timing relationships are illustrated in the timing diagrams.



t_{TSU}	TUNING DATA LATCH SET-UP TIME
t_{TH}	TUNING DATA HOLD TIME
t_{LMP}	MSW/LSW LATCH MINIMUM PULSE WIDTH LOW = 2ns
t_{LSU}	LOAD COMMAND SET-UP TIME
t_{LH}	LOAD COMMAND HOLD TIME
t_{LD}	MINIMUM LOAD COMMAND DELAY, MEASURED FROM MOST RECENT MSW/LSW REGISTER UPDATE
t_{SD}	SYNC PROPAGATION DELAY (DOES NOT INCLUDE 17 CLOCK CYCLE PIPELINE DELAY)
t_{SP}	SYNC PULSE WIDTH
t_{PD}	OUTPUT DATA (A_0 – A_{11}) PROP DELAY

Figure 1. AD9950 Bus Mode Timing Diagram

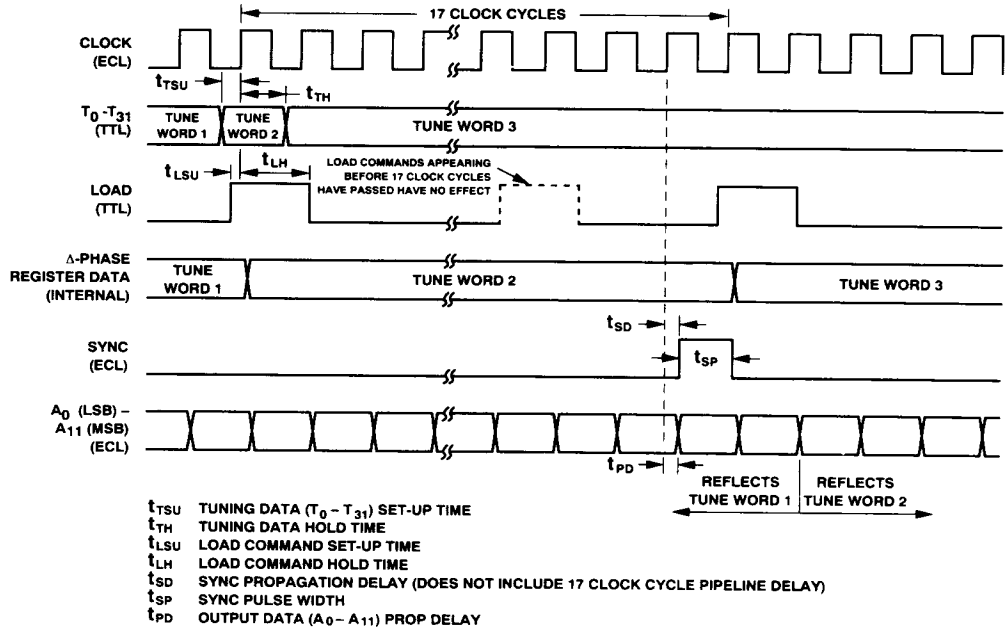


Figure 2. AD9950 Parallel Mode Timing Diagram

When new data is presented to the Δ-Phase register, the carry-save architecture requires that the data for the 2-bit cores be staggered in time, and this delay is provided by the block labeled Pre-Align Pipeline Register. The scheme used to prealign the data requires the Δ-Phase Register to remain constant for 16 clock cycles after each update.

Timing circuits in the AD9950 latch the contents of the Δ-phase register for 16 clock cycles after the LOAD command goes HIGH, preventing corruption of the data during the prealignment process. After the 16-clock-cycle delay, the SYNC output will go high for one clock cycle to indicate that new data has completed the prealignment, and a new tuning word can be loaded into the Δ-phase register. It should be noted that the tuning speed (frequency update rate) of the DDS is limited by this architecture to one-seventeenth of the clock rate.

The data from the 2-bit cores must also be realigned to provide the 12-bit output of the AD9950, and this delay is provided by the block labeled Post-Align Register. When the quad logic is enabled (QUAD EN @ logic HIGH), the 10 LSBs (A_0–A_9) are inverted when A_{10} is HIGH. This logic is used with similar external logic to reduce the size of a sine look-up table.

Pre- and post-alignment delays combine to form a 17-clock-cycle delay of the output data. In addition to this delay, the loading of the Δ-phase register and the adder accumulator each add an additional clock cycle delay, bringing the total delay through the AD9950 to 19 clock cycles.

The $\overline{\text{RESET}}$ (active LOW) command is asynchronous, and will reset the adder accumulator and the post-align logic. The Δ-phase register and the pre-align logic are not affected by the $\overline{\text{RESET}}$ command, even though the timing (SYNC) circuits are reset. A complete reset of the AD9950 should be executed whenever power is applied. This resetting consists of loading the Δ-phase register with all zeros; allowing the data to propagate through the prealign registers (16 clock cycles, as described above); and then taking the $\overline{\text{RESET}}$ pin LOW.

Timing for the reset circuits is shown in Figure 3.

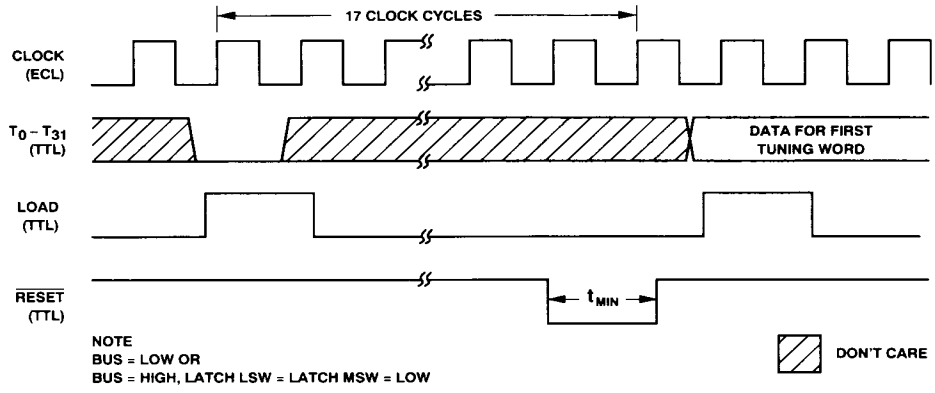


Figure 3. AD9950 $\overline{RESET}$ Timing Diagram

DIRECT DIGITAL SYNTHESES

Direct digital synthesis (DDS) is a method of deriving a wide-band, digitally controlled frequency (sine wave) synthesizer from a single reference frequency (system clock).

The circuit has three major components:
1. Phase Accumulator
2. Phase-to-Amplitude Converter
3. Digital-to-Analog Converter

These major stages and their relationships to one another are illustrated in the block diagram shown below.

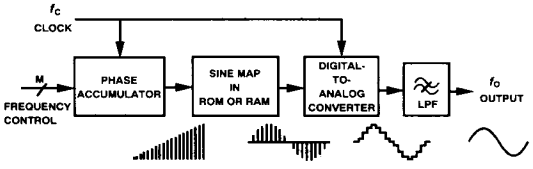


Figure 4. Block Diagram of DDS Generator

The phase accumulator is a digital device which generates the phase increment of the output waveform. Its input is a digital word which (with the reference oscillator) determines the frequency of the output waveform. The output of the phase accumulator stage represents the current phase of the generated waveform. In effect, the accumulator serves as a variable-frequency oscillator generating a digital signal.

Translating phase information from the phase accumulator into amplitude data takes place in the phase-to-amplitude converter; this is most commonly accomplished by means of a look-up table (LUT) stored in memory.

In the final step of frequency synthesis, amplitude data is converted into an analog signal. This is done by a digital-to-analog (D/A) converter which must have good linearity; low glitch impulse; and fast, symmetrical rise and fall times. When it does, the frequency synthesizer is able to produce a spectrally pure waveform.

The AD9950 is a digital phase accumulator intended for use in DDS applications. A simplified block diagram of an accumulator is shown below.

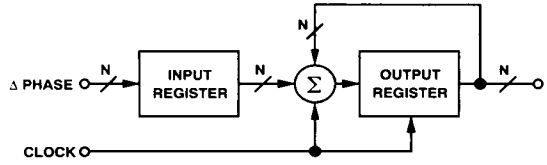


Figure 5. Accumulator Simplified Block Diagram

Operation of the device is straightforward: the contents of the input register are added to the output register on each clock cycle.

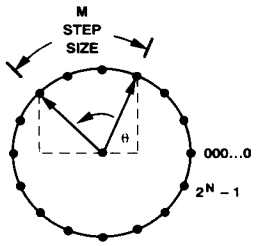
Input data represents a phase step, and is referred to as Δ-phase. The output data is a digital ramp whose frequency is a fraction of the clock frequency:

$$f_{OUT} = \frac{Phase\ Step}{2\pi} f_{CLOCK} = \frac{\Delta\ Phase}{2^N} f_{CLOCK},$$

$$\Delta\ Phase \leq 2^N - 1$$

where N is the resolution (number of bits) of the accumulator. (N determines the resolution to which the output frequency can be adjusted: $f_{CLOCK}/2^N$.)

The output data of the phase accumulator can be considered a phase vector moving around a circle, as shown graphically in Figure 6.



ACCUMULATOR RESOLUTION

BITS	NUMBER OF POINTS
8	256
12	4096
16	65536
20	1048576
24	16777216
28	268435456
32	4294967296

Figure 6. Vector Representation of Phase Accumulator State

In this analogy, the vector will move around the circle in fixed steps, called Δ-Phase, in response to each clock cycle. The number of phase points which is available is determined by N, the resolution of the accumulator. The frequency of the output waveform is determined by the number of clock cycles required to move the phase vector around the circle one time.

Phase data at the output of the accumulator is converted to amplitude data by means of a look-up table (LUT); that data, in turn, is converted to an analog signal by a digital-to-analog converter (DAC).

To avoid aliasing, the output frequency should be limited to less than one-half the clock frequency. This translates to limiting Δ-Phase $\leq 2^{(N-1)}$. The majority of DDS systems limit output frequency to less than 40% of the clock rate to make design of the low-pass filter (LPF) easier. Practical DDS designs often limit the output frequency to less than 25% to minimize the effects of ac limitations in the DAC.

The DAC is the only analog component in the circuit, and its resolution determines the amplitude quantization of the generated waveform. This amplitude quantization places a theoretical limit on the signal-to-noise ratio (SNR) of the DDS system. In addition to quantization effects, the DAC has static and dynamic nonlinearities which corrupt the converter's ideal transfer function. DC nonlinearity, slew rate, glitch impulse, settling time, and digital feedthrough are all DAC characteristics which can reduce the dynamic range of the overall DDS system.

Implementing the Look-Up Table

Using the full resolution of the phase accumulator in the phase-to-amplitude conversion is both impractical and unnecessary. As an example, using the full resolution of the AD9950 would require a look-up table >4G × 12.

It is preferable to have the LUT only large enough to insure that the dc error of the output waveform is dominated by the quantization error of the DAC. In most DDS applications, the conversion is to a sine (or cosine) wave. This requires the look-up table to have two more bits of resolution than the DAC. In the AD9950, phase output data is truncated to 12 bits, supporting a 10-bit DAC for sine wave applications (4k × 10 LUT).

Using the Quad Logic

In sine wave applications, the amount of memory needed to implement the LUT can be reduced by taking advantage of the known characteristics of a sine wave. The AD9950 incorporates on-board "quad logic" to simplify using this technique. This logic is enabled by taking the QUAD EN (Pin 26) input high.

First, the look-up table does not need to store the most significant bit (MSB) of the amplitude data because it is the same as the MSB of the phase accumulator data; this reduces the amount of memory which is required to 4k × 9.

The symmetrical properties of sine waves allow further reduction. Only the first quadrant (90°) of the sine wave is required, as shown. This reduces the memory of the LUT addressed by the 10 LSBs of the AD9950 to 1k × 9.

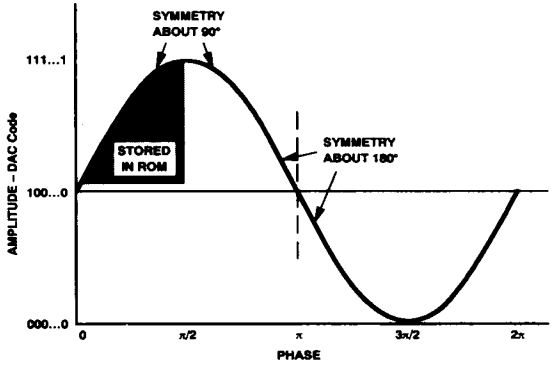


Figure 7. AD9950 Sinewave Phase-Amp Converter

Because the second quadrant of the sine wave is the mirror image of the first, it can be addressed by inverting the 10 least significant bits (LSBs) of the AD9950. This address inversion is performed on board the AD9950 by the quadrature logic, a set of inverters which are transparent when data is in the first quadrant, but functional when data is in the second quadrant. The second-most significant bit (A_{10}) of the accumulator determines in which quadrant the data is located and controls the inverters.

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Each inverter is actually a two-input exclusive-or (XOR) gate driven by one of the LSBs (A_0–A_9) and A_{10}. Its operation is illustrated in Figure 8.

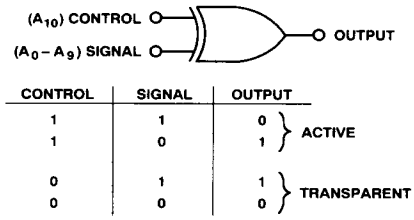


Figure 8. XOR as Controlled Inverter

Quadrants three and four of the sine wave are the inverse of quadrants one and two. Amplitude data for the LSBs in these quadrants is obtained by inverting the data from the LUT. This step is similar to the inversion described earlier, and is controlled by the complement of the accumulator's MSB. In the Analog Devices model AD9720, this operation is integrated into the DAC. The complete phase-to-amplitude conversion process using quad logic is illustrated below.

The memory used to construct the look-up table must have a fast read access time; 3 ns ECL RAM (10E474, 1k × 4) will support the update rate of the AD9950. Most applications will require a separate read-only memory (ROM) to store the data permanently and an initialization process to load this data into the RAM during the time the DDS circuit is being initialized.

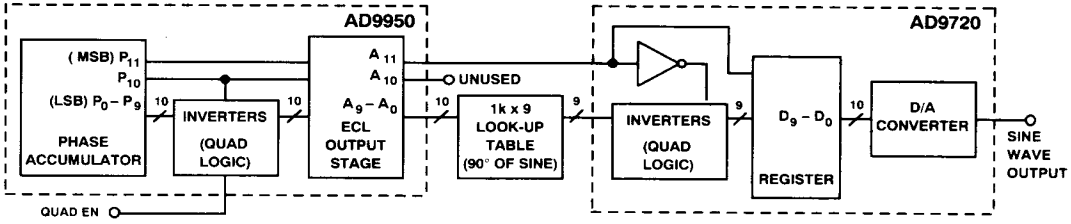


Figure 9. Phase-to-Sine Amplitude Conversion, Using Quad Logic

Layout and Power Supplies

Proper layout of high speed circuits is always critical, but is particularly important when both analog and digital signals are involved (i.e., DDS systems).

Analog signal paths should be kept as short as possible, and be properly terminated to avoid reflections. The analog input voltage and the voltage references should be kept away from digital signal paths; this reduces the amount of digital switching noise that is capacitively coupled into the analog section of the circuit.

Digital signal paths should also be kept short, and run lengths should be matched to avoid propagation delay mismatch. Terminations for ECL signals should be as close as possible to the receiving gate.

In high speed circuits, layout of the ground circuit is a critical factor. A single, low impedance ground plane, on the component side of the board, will reduce noise on the circuit ground. Power supplies should be capacitively coupled to the ground plane to reduce noise in the circuit. Multilayer boards allow designers to lay out signal traces without interrupting the ground plane, and provide low impedance power planes.

AD9950 APPLICATION

The diagram shown below illustrates implementation of a 300 MSPS direct digital synthesizer using the AD9950 32-bit phase accumulator and the AD9720 10-bit 300 MSPS digital-to-analog converter (DAC). The AD9950 is controlled by a 16-bit microprocessor, which provides tuning data for the system.

Phase-to-amplitude conversion uses a 1k × 9 LUT and is stored in very fast (3 ns access time) ECL RAM. Data for the ECL RAM is stored permanently in a CMOS ROM and is transferred into the RAM as part of the initilization process discussed earlier.

Sine data for the LUT is based on the 12-bit phase data from the AD9950 and is calculated as:

$$ROUND\left[511.5 \times sin\left(\frac{A_0\text{–}A_9}{4096} \times 2\pi\right)\right]$$

This provides data for the AD9720 DAC that has a spectral purity of ≤ 76 dBFS.

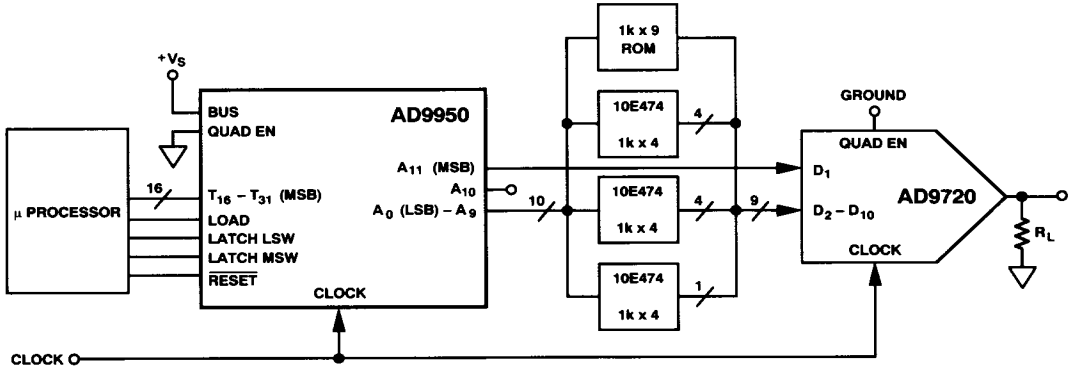
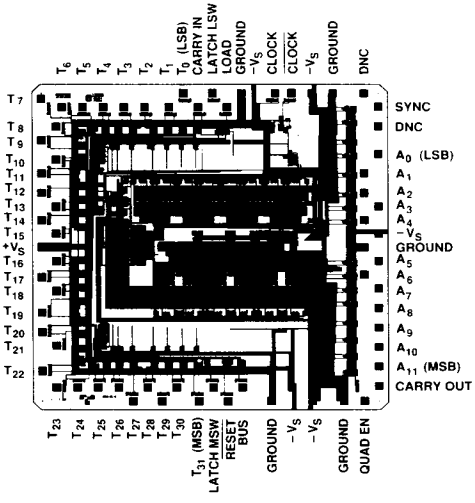


Figure 10. AD9950 10-Bit DDS Application

DIE LAYOUT AND MECHANICAL INFORMATION



Die Dimensions	175 × 172 × 15 (±2) mils
Pad Dimensions	4 × 4 mils
Metalization	Gold
Backing	None
Substrate Potential	$-V_S$
Passivation	Nitride
Die Attach	Gold Eutectic (Ceramic)
Bond Wire	1–1.3 mil, Gold; Gold Ball Bonding

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9950KJ	0°C to +70°C	68-Pin J-Leaded Ceramic	J-68
AD9950TJ	−55°C to +125°C	68-Pin J-Leaded Ceramic	J-68

*J = J-leaded ceramic package; hermetically sealed ceramic package, similar to PLCC. For outline information see Package Information section.