TRI-STATE® Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources, and feature a strobe-controlled TRI-STATE output. The strobe must be at a low logic level to enable these devices. The TRI-STATE outputs permit direct connection to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transitors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

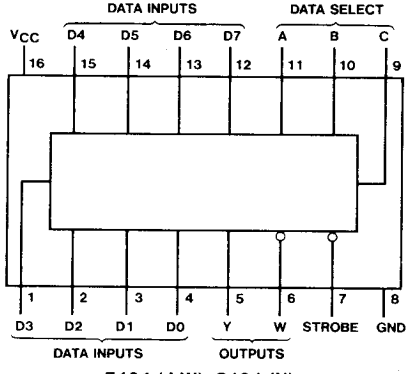
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

Features

- TRI-STATE versions of DM54/74151
- Interface directly with system bus
- Perform parallel-to-serial conversion
- Permit multiplexing from N-lines to one line
- Complementary outputs provide true and inverted data
- Pin equivalent DM54251/DM74251

Type	Max No. of Common Outputs	Typical Prop Delay Time (D to Y)	Typical Power Dissipation
DM7121	49	17 ns	155 mW
DM8121	129	17 ns	155 mW

Connection Diagram



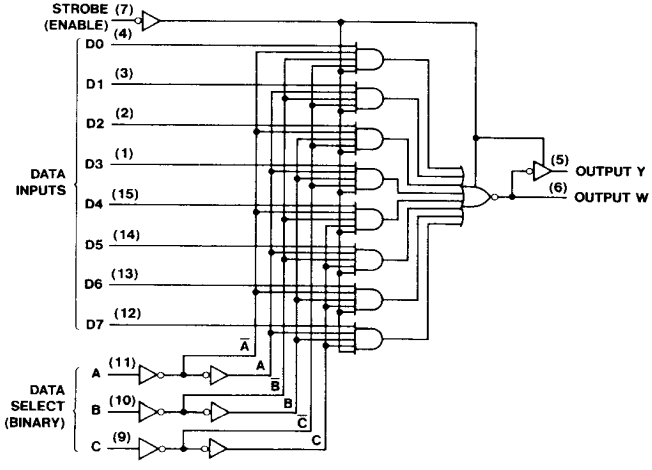
7121 (J,W); 8121 (N)

Truth Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Logic Level, L = Low Logic Level
X = Don't Care, Z = High Impedance (Off)
D0, D1...D7 = The level of the respective D input.

Logic Diagram



Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Conditions		DM71/81 21 Min	DM71/81 21 Typ (1)	DM71/81 21 Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{OH}	High Level Output Current		DM54			−2	mA
			DM74			−5.2	
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = Max		2.4			V
I_{OL}	Low Level Output Current					16	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
$I_{O(OFF)}$	Off-State (High-Impedance State) Output Current	V_{CC} = Max, V_{IH} = 2 V	V_O = 0.4 V			−40	μA
			V_O = 2.4 V			40	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5 V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4 V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4 V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (2)		−18		−70	mA
I_{CC}	Supply Current	V_{CC} = Max (3)			31	51	mA

Note 1: All typical values are at V_{CC} = 5 V, T_A = 25°C.
Note 2: Not more than one output should be shorted at a time.
Note 3: All inputs at 4.5 V and all outputs open.

7

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

Parameter		From (Input)	To (Output)	Conditions	DM71/81 21 Min	DM71/81 21 Typ	DM71/81 21 Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A, B, or C (4 levels)	Y	C_L = 50 pF, R_L = 400 Ω		22	36	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					23	36	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A, B, or C (3 levels)	W			18	29	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					16	27	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any D	Y			17	28	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					18	28	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		W			11	15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					10	15	ns
t_{ZH}	Output Enable Time to High Level	Strobe	Y			15	27	ns
t_{ZL}	Output Enable Time to Low Level					18	36	ns
t_{ZH}	Output Enable Time to High Level		W			15	27	ns
t_{ZL}	Output Enable Time to Low Level					19	38	ns
t_{HZ}	Output Disable Time from High Level		Y	C_L = 5 pF, R_L = 400 Ω		4	8	ns
t_{LZ}	Output Disable Time from Low Level					14	23	ns
t_{HZ}	Output Disable Time from High Level		W			4	8	ns
t_{LZ}	Output Disable Time from Low Level					15	23	ns