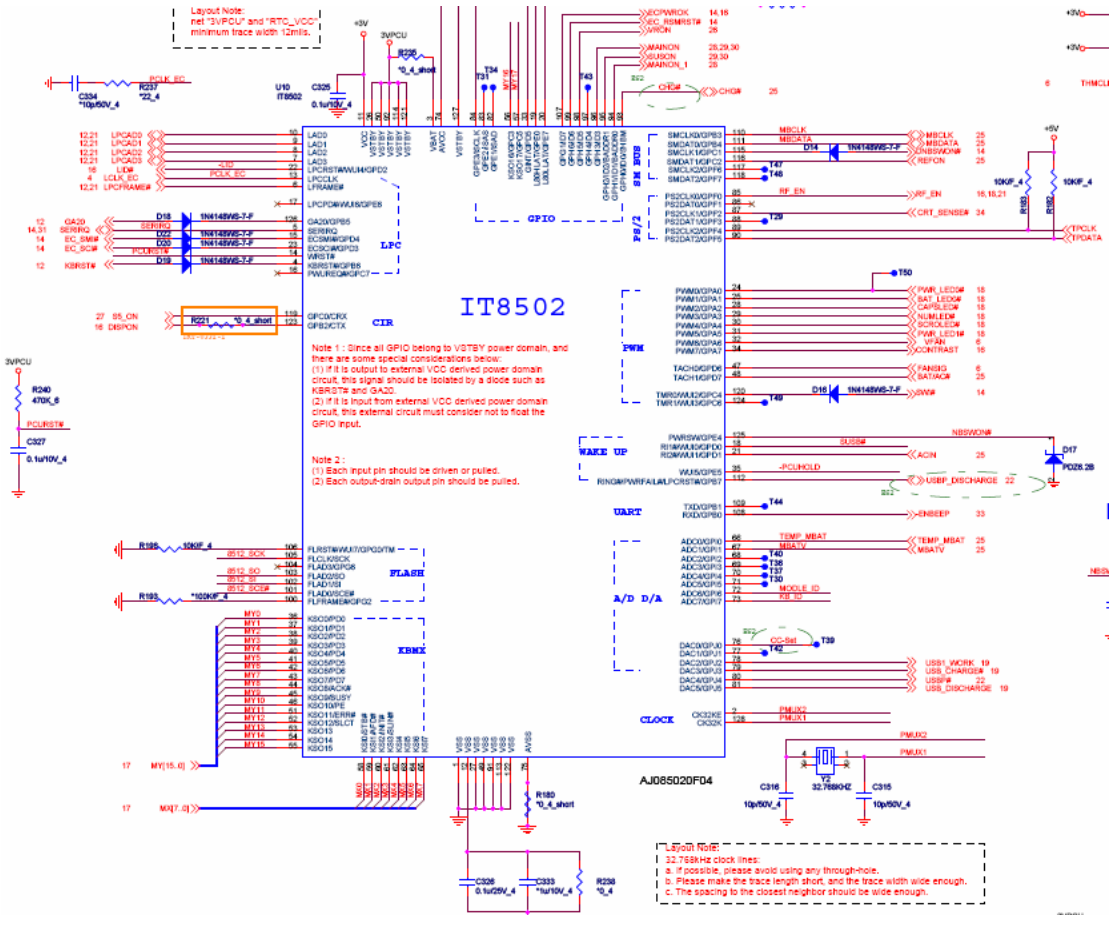
ITE IT8502E/JX-L　EC 外围线路图：



EC reset timing 和 warm reset timing 图：

Figure 10-2. Reset Timing

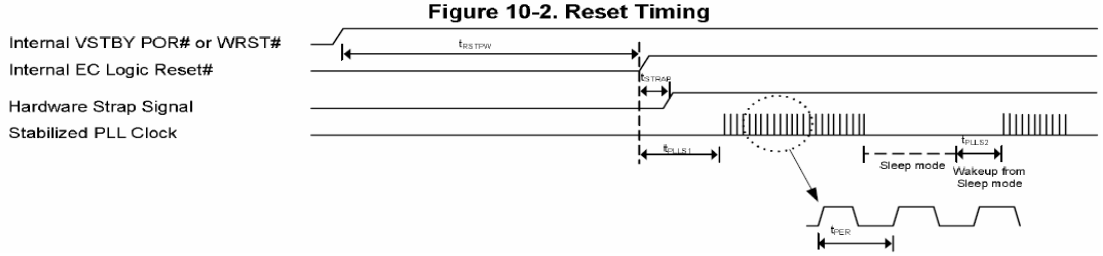


Table 10-2. Reset AC Table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RSTPW}	Internal EC logic reset after VSTBY POR or WRST#	—	1650	—	Tick (by 32.768 KHz)
t_{STRAP}	Strap sampling time	0	—	—	ns
t_{PLLS1}	PLL stabilization time hardware	—	5	—	ms
t_{PLLS2}	PLL stabilization time after waking up from Sleep mode	—	5	—	ms
t_{PER}	PLL clock period	—	$1/_{FreqPLL}$	—	ns
FreqPLL	PLL clock frequency if PLLFREQ = 0011b	—	32.3	—	MHz
	PLL clock frequency if PLLFREQ = 0101b	—	46.0	—	MHz
	PLL clock frequency if PLLFREQ = 0111b	—	64.5	—	MHz
FreqEC	EC clock frequency if PLLFREQ = 0111b	—	9.2	—	MHz

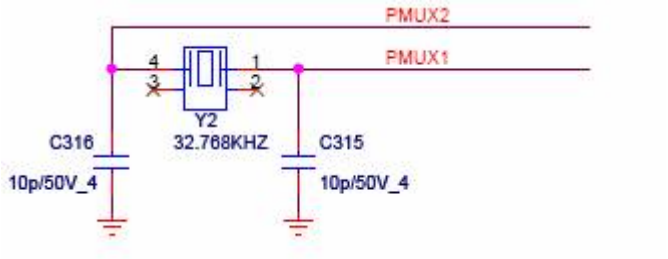
Figure 10-3. Warm Reset Timing

Table 10-3. Warm Reset AC Table

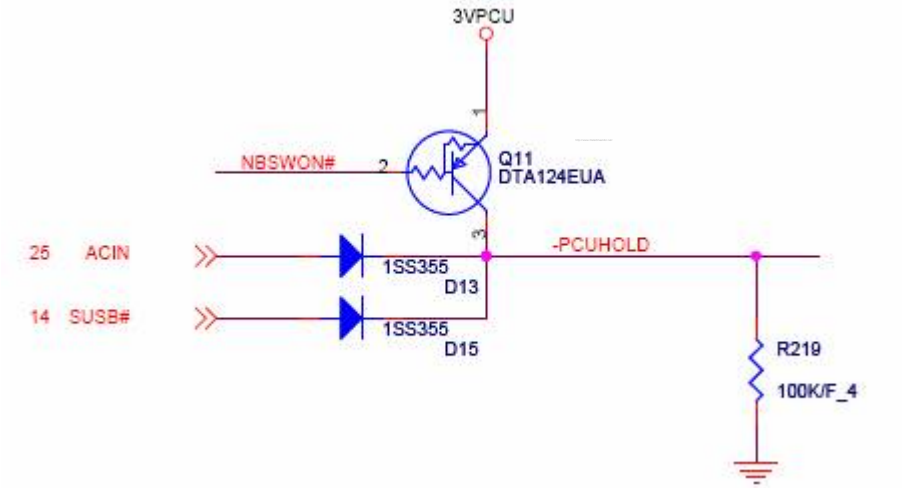
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WRSTW}	Warm reset width	10	—	—	μs

EC 不动先确认一下几个地方：

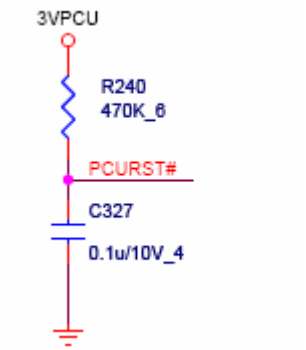
1.Y2 开机后是否有起振？



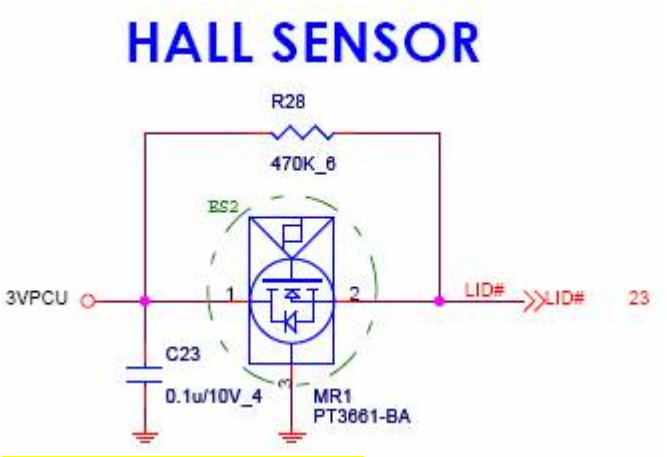
2. –PCUHOLD 是否为高电平？



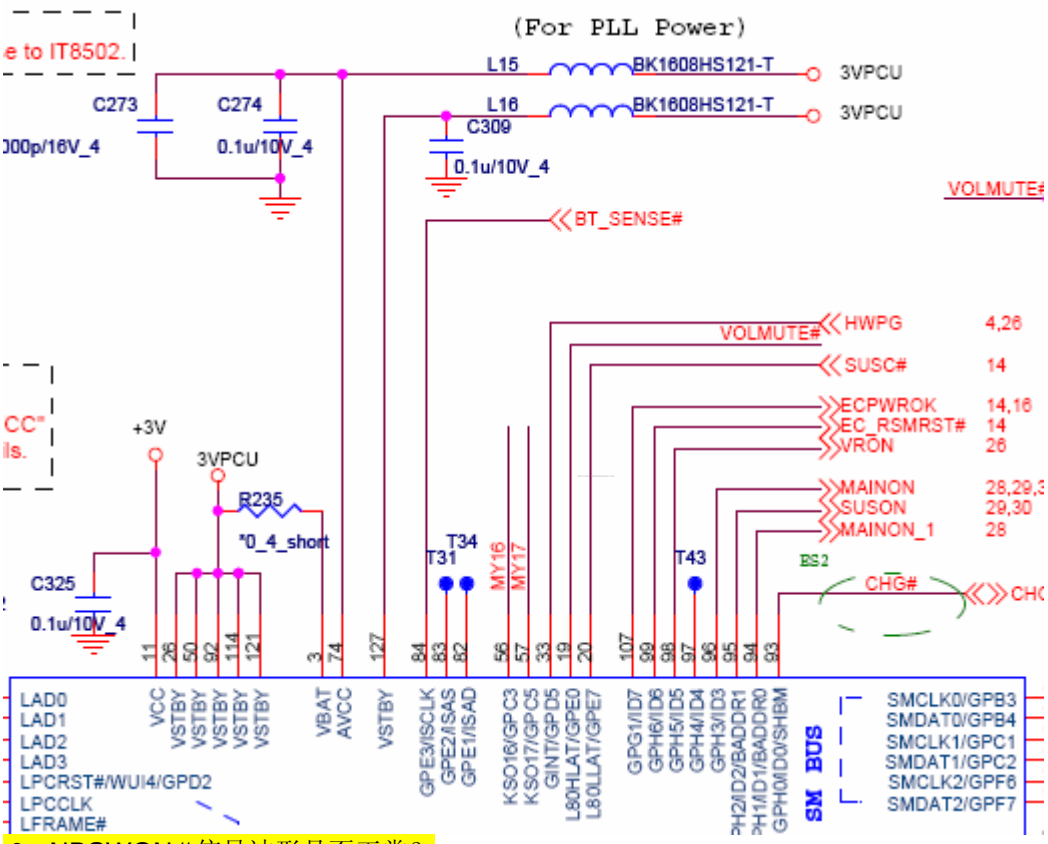
3. PCURST#信号是否为高电平？



4. LID#信号是否为高电平？



5. 3VPCU 是否正常供给 EC?



6. NBSWON#信号波形是否正常?

7. LFRAME#信号是否有动起来?