M80C51BH/M80C31BH
## CMOS SINGLE-CHIP 8-BIT MICROCOMPUTER
Military

- M80C31BH—Control Oriented CPU with RAM and I/O
- M80C51BH—An M80C31BH with Factory Mask-Programmable ROM
- Power Control Modes
- 128 x 8-Bit RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- Available in 40-Pin CERDIP, 44-Pin Leadless Chip Carrier, 44-Pin Gullwing and 44-Pin J-Lead Packages

- 64K Program Memory Space
- High Performance CHMOS Process
- Boolean Processor
- 5 Interrupt Sources
- Programmable Serial Port
- 64K Data Memory Space
- Military Temperature Range: −55°C to + 125°C (T$_C$)

The MCS®-51 CHMOS products are fabricated on Intel's CHMOS III process and are functionally compatible with the standard MCS-51 HMOS and EPROM products. CHMOS III is a technology which combines the high speed and density characteristics of HMOS with the low power attributes of CHMOS. This combination expands the effectiveness of the powerful MCS-51 architecture and instruction set.

Like the MCS-51 HMOS versions, the MCS-51 CHMOS products have the following features: 4K byte of ROM (M80C51BH only); 128 bytes of RAM; 32 I/O lines; two 16-bit timer/counters; a five-source two-level interrupt structure; a full duplex serial port; and on-chip oscillator and clock circuitry. In addition, the MCS-51 CHMOS products have two software selectable modes of reduced activity for further power reduction—Idle and Power Down.

The Idle mode freezes the CPU while allowing the RAM, timer/counters serial port and interrupt system to continue functioning. The Power Down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

Figure 1. Block Diagram

*For complete Rochester ordering guide, please refer to page 2 *
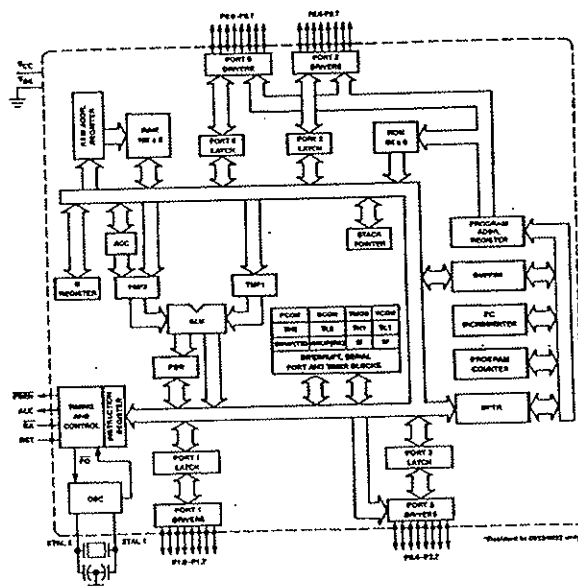
Rochester Ordering Guide

Rochester Part Number	OCM Part Number	Package	Temperature
MC80C31BH	MC80C31BH	DIP-40	-55° to +125°C
MD80C31BH	MD80C31BH	DIP-40	-55° to +125°C
MR80C31BH	MR80C31BH	LLCC-44	-55° to +125°C
MT80C31BH	MT80C31BH	LDCC-44	-55° to +125°C
MZ80C31BH	MZ80C31BH	QFP-44	-55° to +125°C
MD80C51BH	MD80C51BH	DIP-40	-55° to +125°C
MR80C51BH	MR80C51BH	LLCC-44	-55° to +125°C
MT80C51BH	MT80C51BH	LDCC-44	-55° to +125°C
MZ80C51BH	MZ80C51BH	QFP-44	-55° to +125°C

ABSOLUTE MAXIMUM RATINGS*

Case Temperature Under Bias... $-55°C$ to $+125°C$

Storage Temperature .... $-65°C$ to $+150°C$

Voltage on Any Pin to V_{SS} .... $-0.5V$ to $V_{CC} +0.5V$

Voltage on V_{CC} to V_{SS} .... $-0.5V$ to $+6.5V$

Power Dissipation .... 200 mW

Operating Conditions

Symbol	Description	Min	Max	Units
T_C	Case Temperature (Instant On)	-55	$+125$	°C
V_{CC}	Digital Supply Voltage	4.0	6.0	V
f_{OSC}	Oscillator Frequency	3.5	12	MHz

D.C. CHARACTERISTICS (Over Specified Operating Conditions)

Symbol	Parameter	Min	Max	Units	Comments
V_{IL}	Input Low Voltage (Except EA)	-0.5	$0.2 V_{CC} - 0.25$	V	
V_{IL1}	Input Low Voltage (EA)	-0.5	$0.2 V_{CC} - 0.45$		
V_{IH}	Input High Voltage (Except XTAL1, RST)	$0.2 V_{CC} + 1.1$	$V_{CC} + 0.5$	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	$0.7 V_{CC} + 0.2$	$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage (Ports 1, 2, 3)		0.45	V	$I_{OL} = 1.6$ mA (Note 1)
V_{OL1}	Output Low Voltage (Port 0, ALE, PSEN)		0.45	V	$I_{OL} = 3.2$ mA (Note 1)
V_{OH}	Output High Voltage (Ports 1, 2, 3)	2.4		V	$I_{OH} = -60 \mu A$, $V_{CC} = 5V \pm 10\%$
		$0.75 V_{CC}$		V	$I_{OH} = -25 \mu A$
		$0.9 V_{CC}$		V	$I_{OH} = -10 \mu A$
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode, ALE, PSEN)	2.4		V	$I_{OH} = -400 \mu A$, $V_{CC} = 5V \pm 10\%$
		$0.75 V_{CC}$		V	$I_{OH} = -150 \mu A$
		$0.9 V_{CC}$		V	$I_{OH} = -40 \mu A$ (Note 2)
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)		-75	μA	$V_{in} = 0.45V$
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, 3)		-750	μA	$V_{in} = 2V$
I_{LI}	Input Leakage Current (Port 0, EA)		± 10	μA	$0.45 < V_{in} < V_{CC}$
R_{RST}	Reset Pulldown Resistor	50	150	$K\Omega$	
C_{IO}	Pin Capacitance		10	pF	Test Freq = 1 MHz, $T_C = 25°C$
I_{PD}	Power Down Current		75	μA	$V_{CC} = 2V$ to $6V$ (Note 5)

*See "Notes" on next page.

MAXIMUM I$_{CC}$ (mA)

Freq. V$_{CC}$	Operating (Note 3)			Idle (Note 4)		
	4V	5V	6V	4V	5V	6V
3.5 MHz	4.3	5.7	7.5	1.1	1.6	2.2
8.0 MHz	8.3	11	14	1.8	2.7	3.7
12 MHz	12	16	20	2.5	3.7	5

NOTES:
1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V$_{OLS}$ of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
2. Capacitive loading on Ports 0 and 2 may cause the V$_{OH}$ on ALE and $\overline{PSEN}$ to momentarily fall before the 0.9 V$_{CC}$ specification when the address bits are stabilizing.
3. I$_{CC}$ is measured with all output pins disconnected; XTAL1 driven with TCLCH, TCHCL = 5 ns, V$_{IL}$ = V$_{SS}$ + 0.5V, V$_{IH}$ = V$_{CC}$ − 0.5V; XTAL2 N.C.; $\overline{EA}$ = RST = Port 0 = V$_{CC}$. I$_{CC}$ would be slightly higher if a crystal oscillator is used (see Figure 5).
4. Idle I$_{CC}$ is measured with all output pins disconnected; XTAL1 driven with TCLCH, TCHCL = 5 ns, V$_{IL}$ = V$_{SS}$ + 0.5V, V$_{IH}$ = V$_{CC}$ − 0.5V; XTAL2 N.C.; Port 0 = V$_{CC}$; $\overline{EA}$ = RST = V$_{SS}$ (see Figure 6).
5. Power Down I$_{CC}$ is measured with all output pins disconnected; XTAL1 = V$_{SS}$; XTAL2 N.C.; Port 0 = V$_{CC}$; $\overline{EA}$ = RST = V$_{SS}$ (see Figure 8).

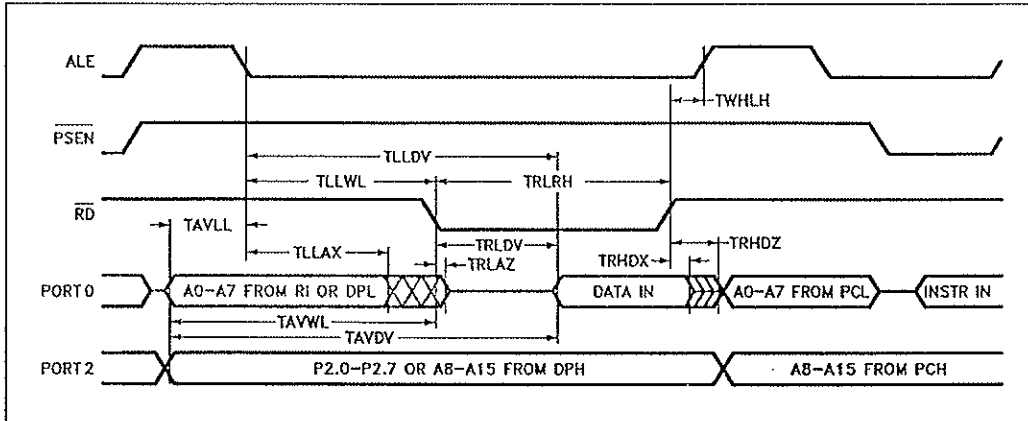## A.C. CHARACTERISTICS (Over Specified Operating Conditions)

Capacitance for Port 0, ALE, and PSEN = 100 pF, Load Capacitance for All Other Outputs = 80 pF

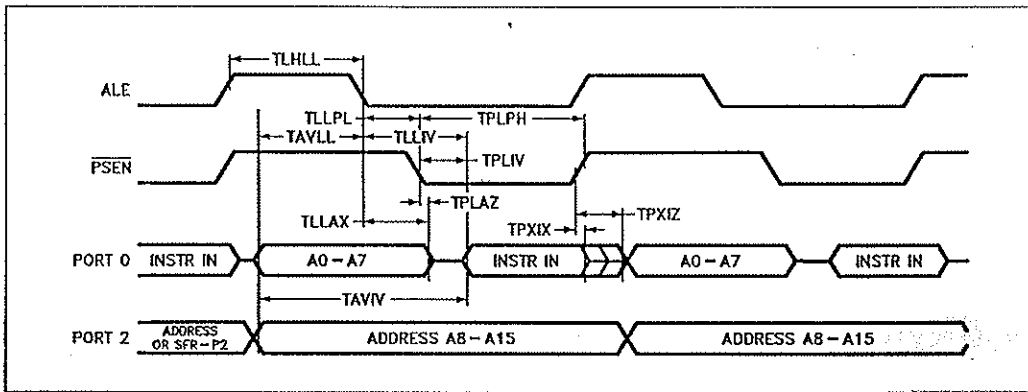### EXTERNAL PROGRAM AND DATA MEMORY CHARACTERISTICS

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
1/TCLCL	Oscillator Frequency			3.5	12	MHz
TLHLL	ALE Pulse Width	127		2TCLCL−40		ns
TAVLL	Address Valid to ALE Low	28		TCLCL−55		ns
TLLAX	Address Hold After ALE Low	48		TCLCL−35		ns
TLLIV	ALE Low to Valid Instr In		223		4TCLCL−110	ns
TLLPL	ALE Low to PSEN Low	43		TCLCL−40		ns
TPLPH	PSEN Pulse Width	205		3TCLCL−45		ns
TPLIV	PSEN Low to Valid Instr In		135		3TCLCL−115	ns
TPXIX	Input Instr Hold After PSEN	0		0		ns
TPXIZ	Input Instr Float After PSEN		58		TCLCL−25	ns
TAVIV	Address to Valid Instr In		302		5TCLCL−115	ns
TPLAZ	PSEN Low to Address Float		10		10	ns
TRLRH	RD Pulse Width	400		6TCLCL−100		ns
TWLWH	WR Pulse Width	400		6TCLCL−100		ns
TRLDV	RD Low to Valid Data In		242		5TCLCL−175	ns
TRHDX	Data Hold After RD	0		0		ns
TRHDZ	Data Float After RD		97		2TCLCL−70	ns
TLLDV	ALE Low to Valid Data In		507		8TCLCL−160	ns
TAVDV	Address to Valid Data In		575		9TCLCL−175	ns
TLLWL	ALE Low to RD or WR Low	200	300	3TCLCL−50	3TCLCL+50	ns
TAVWL	Address to RD or WR Low	203		4TCLCL−130		ns
TQVWX	Data Valid to WR Transition	23		TCLCL−60		ns
TWHQX	Data Hold After WR	33		TCLCL−50		ns
TRLAZ	RD Low to Address Float		0		0	ns
TWHLH	RD or WR High to ALE High	43	123	TCLCL−40	TCLCL+40	ns

EXTERNAL DATA MEMORY READ CYCLE

EXTERNAL PROGRAM MEMORY READ CYCLE

EXTERNAL DATA MEMORY WRITE CYCLE

SHIFT REGISTER MODE TIMING WAVEFORMS

CLOCK WAVEFORMS

NOTE:
This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component to component.
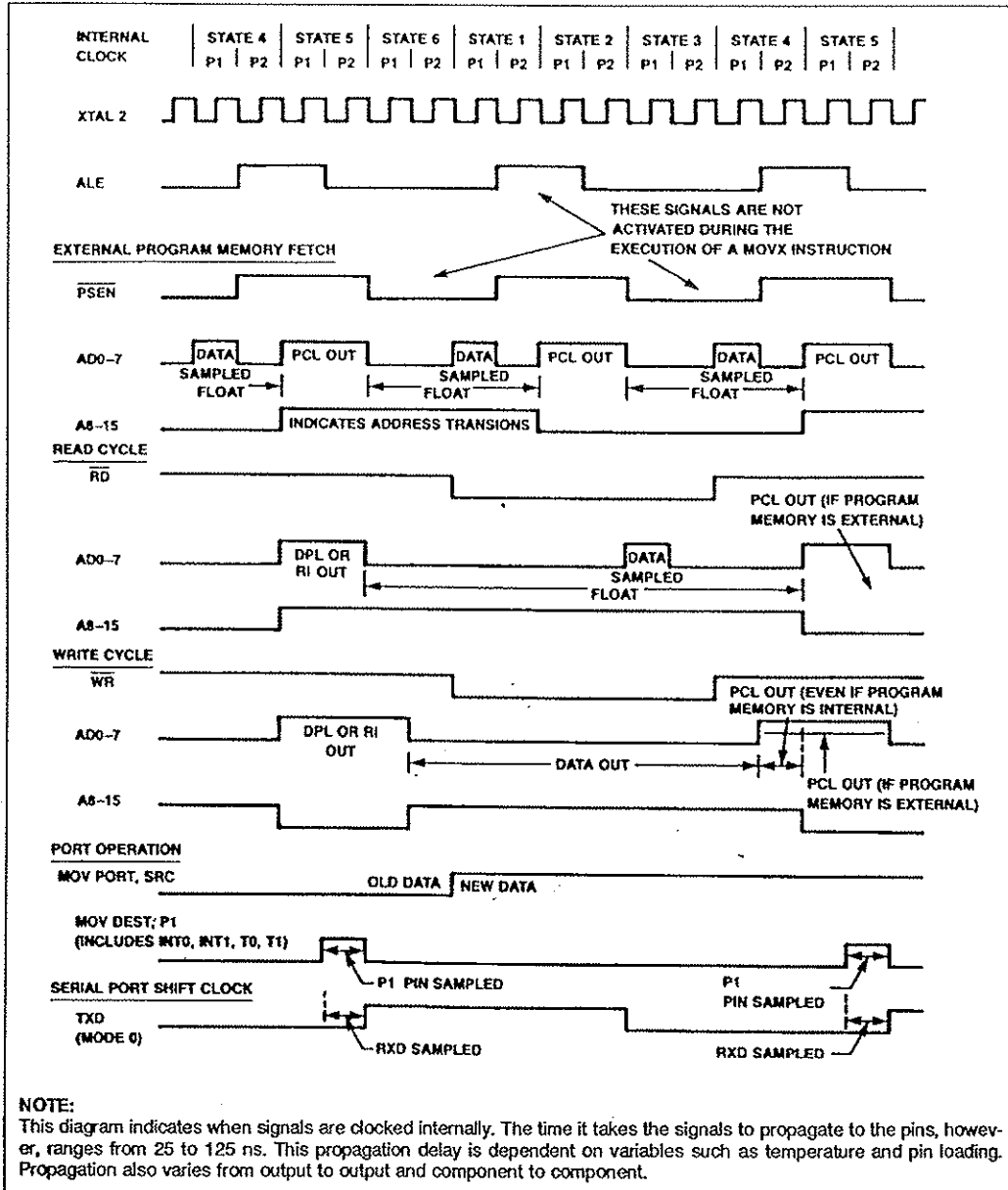
EXTERNAL CLOCK DRIVE

Symbol	Parameter	Min	Max	Units
1/TCLCL	Oscillator Frequency	3.5	12	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

SERIAL PORT TIMING—SHIFT REGISTER MODE (Over Specified Operating Conditions)

Symbol	Parameter	12 MHz Osc Min	12 MHz Osc Max	Variable Oscillator Min	Variable Oscillator Max	Units
TXLXL	Serial Port Clock Cycle Time	1.0		12TCLCL		μs
TQVXH	Output Data Setup to Clock Rising Edge	700		10TCLCL − 133		ns
TXHQX	Output Data Hold After Clock Rising Edge	50		2TCLCL − 117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		700		10TCLCL − 133	ns

EXTERNAL CLOCK DRIVE WAVEFORMS
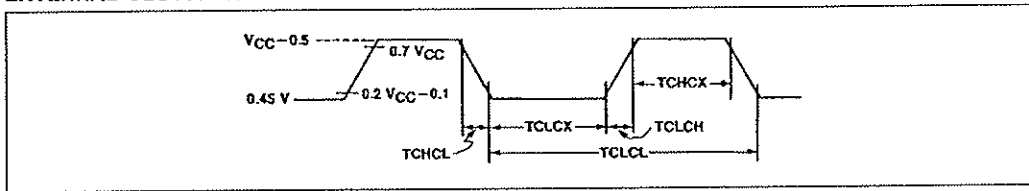
A.C. TESTING: INPUT/OUTPUT WAVEFORMS

AC inputs during testing are driven at V_{CC} −0.5 for a Logic "1" and 0.45V for a Logic "0". Timing measurements are made at V_{IH} min. for a Logic "1" and V_{IL} max. for a Logic "0".

FLOAT WAVEFORM

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.
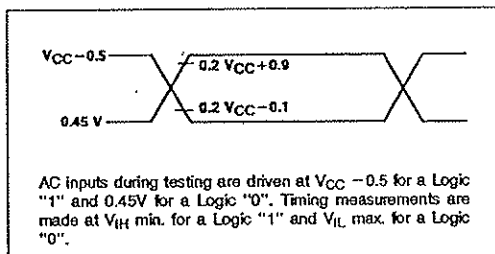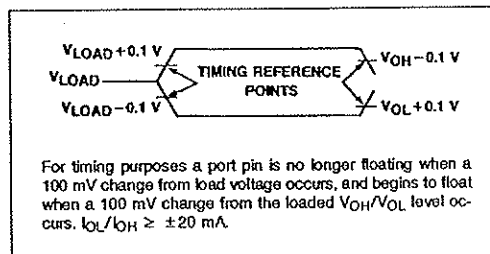
Serial Port Timing is tested functionally only, but guaranteed to specified limits.