

NCP112

Supervisory IC for Desktop Power Supply Monitoring

The NCP112 is a highly integrated supervisory circuit that incorporates all the functions necessary for monitoring and controlling a multi-output switch-mode power supply system. The NCP112 provides an ability to monitor the status of the power supply outputs and communicate it to the system controller. The programmable output delays protect against spurious fault indicators.

Features

- Under and Overvoltage Protection for 3.3 V, 5.0 V and 12 V Outputs
- Additional Adjustable Overvoltage Protection Input
- Built-in Hysteresis on all Input Pins
- Programmable Undervoltage Blanking During Power-Up
- Fault Output with 20 mA Sink Capability
- Programmable Remote On/Off Delay Time
- Programmable Power Good Delay Time
- Precision Voltage Reference with 20 mA Source Capability
- Optimized for Low-Cost 100 nF Capacitors
- Enhanced Replacement to the TSM112
- Pb-Free Packages are Available

Typical Applications

- Personal Computer Switch Mode Power Supply Monitoring
- Multi-Output Power Supplies Requiring System Supervision



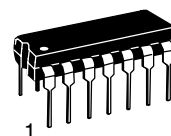
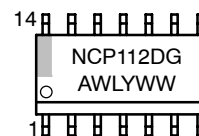
ON Semiconductor®

<http://onsemi.com>

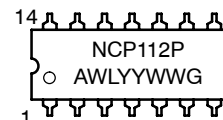
MARKING DIAGRAMS



**SOIC-14
D SUFFIX
CASE 751A**

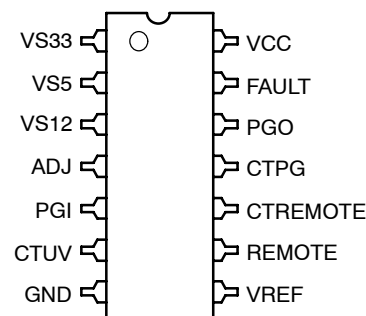


**PDIP-14
P SUFFIX
CASE 646**



A = Assembly Location
 WL = Wafer Lot
 Y, YY = Year
 WW = Work Week
 G = Pb-Free Package

PIN CONNECTIONS



PDIP-14, SOIC-14

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

NCP112

PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Function	Description
1	VS33	3.3 V SENSE INPUT	Over/undervoltage sense input for 3.3 V.
2	VS5	5.0 V SENSE INPUT	Over/undervoltage sense input for 5.0 V.
3	VS12	12 V SENSE INPUT	Over/undervoltage sense input for 12 V.
4	ADJ	ADJUSTABLE OVP INPUT	May be used for an additional overvoltage protection signal.
5	PGI	POWER GOOD INPUT	Power good input signal.
6	CTUV	ADJUSTABLE TIMING CAPACITOR	Adjustable undervoltage blanking delay during power-up.
7	GND	GROUND	Ground
8	VREF	VOLTAGE REFERENCE	Precision 2.5 V reference output.
9	REMOTE	REMOTE ON/OFF INPUT	Input remote control from the microcontroller. Acts as a reset signal after a fault condition.
10	CTREMOTE	ADJUSTABLE REMOTE ON/OFF CAPACITOR	Adjustable remote delay.
11	CTPG	ADJUSTABLE POWER GOOD CAPACITOR	Adjustable power good delay.
12	PGO	POWER GOOD OUTPUT	Power good output. Active high when no fault conditions are present.
13	FAULT	FAULT OUTPUT	Detects over/undervoltage conditions. Active high during a fault condition.
14	VCC	POWER SUPPLY VOLTAGE	Power supply voltage.

NCP112

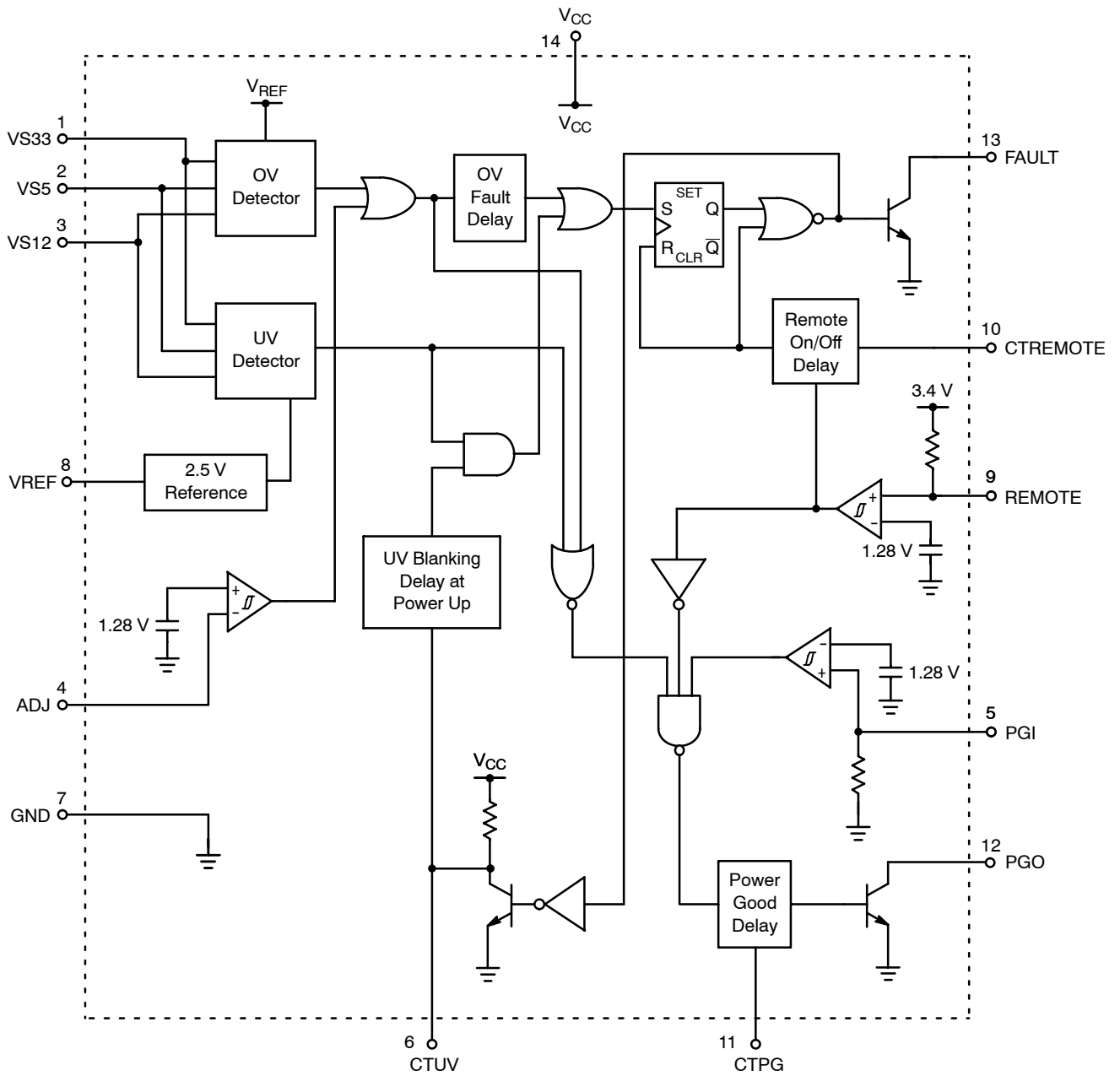


Figure 1. Block Diagram

NCP112

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage (Note 1)	V_{CC}	18	V
Power Good Output Current	I_{PGO}	30	mA
Fault Output Current	I_{FAULT}	30	mA
Voltage Reference Output Current	I_{REF}	20	mA
Voltage Rating (Pins 4, 5, 6, 9, 10, 11)	ADJ, PGI, CTUV, REMOTE, CTREMOTE, CTPG	V_{CC}	V
Voltage Rating (Pins 12, 13)	PGO, FAULT	18	V
Power Dissipation and Thermal Characteristics (PDIP-14) Thermal Resistance, Junction-to-Air Thermal Resistance, Junction-to-Case Maximum Power Dissipation @ 25°C	$R_{\theta JA}$ $R_{\theta JC}$ P_D	100 45 1.25	°C/W °C/W W
Power Dissipation and Thermal Characteristics (SOIC-14) Thermal Resistance, Junction-to-Air Thermal Resistance, Junction-to-Case Maximum Power Dissipation @ 25°C	$R_{\theta JA}$ $R_{\theta JC}$ P_D	125 30 1.0	°C/W °C/W W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A	-40 to +125	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$ for typical values and $T_A = 0^\circ\text{C}$ to 85°C for min and max values, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OPERATING CONDITIONS

DC Power Supply	V_{CC}	4.5	-	16	V
Power Supply Current	I_{CC}	-	3.0	5.0	mA

OVERVOLTAGE/UNDERVOLTAGE PROTECTION

Overvoltage Protection					
3.3 V Output Sense Hysteresis*	VOV_{33} VOV_{hys33}	3.8 -	4.0 40	4.2 -	V mV
5.0 V Output Sense Hysteresis*	VOV_5 VOV_{hys5}	5.8 -	6.1 60	6.4 -	V mV
12 V Output Sense Hysteresis*	VOV_{12} VOV_{hys12}	13.4 -	14.2 130	15 -	V mV
Undervoltage Protection					
3.3 V Output Sense Hysteresis*	VUV_{33} VUV_{hys33}	2.3 -	2.5 100	2.7 -	V mV
5.0 V Output Sense Hysteresis*	VUV_5 VUV_{hys5}	3.7 -	4.0 100	4.3 -	V mV
12 V Output Sense Hysteresis*	VUV_{12} VUV_{hys12}	9.2 -	10 100	10.8 -	V mV

*Hysteresis is measured in direction from threshold point back to nominal value of input voltage (i.e. 3.3 V, 5.0 V or 12 V).

- This device contains ESD protection and exceeds the following tests:
Human Body Model JESD 22-A114-B: 2.0 kV
Machine Model JESD 22-A115-A: 200 V

NCP112

ELECTRICAL CHARACTERISTICS (continued) ($V_{CC} = 5.0\text{ V}$, $T_A = 25^\circ\text{C}$ for typical values and $T_A = 0^\circ\text{C}$ to 85°C for min and max values, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OVERVOLTAGE/UNDERVOLTAGE PROTECTION (continued)

Undervoltage Protection (continued) Adjustable Overvoltage Protection Threshold Hysteresis	V_{ADJth}	–	1.28	–	V
	V_{ADJth}	–	100	–	mV

UNDERVOLTAGE BLANKING DURING POWER UP

Undervoltage Blanking Time ($C_{TUV} = 100\text{ nF}$)	T_{UV}	100	300	500	ms
Undervoltage Blanking Threshold Voltage (Pin 6)	T_{UVth}	–	2.5	–	V

POWER GOOD

Power Good Input Threshold Voltage	V_{PGIth}	–	1.28	–	V
Power Good Input Hysteresis	V_{PGIhys}	–	25	–	mV
Low State Open Collector Saturation Voltage ($I = 20\text{ mA}$)	V_{Lsat}	–	–	0.4	V
High State Open Collector Leakage Current ($V = 5.0\text{ V}$)	I_{Hleak}	–	–	1.0	μA
Power Good Transient (See Application Note Section) Rise Time	$T_{PGraise}$	–	1.0	–	μs
Fall Time	T_{PGfall}	–	1.0	–	μs
Adjustable Delay Time ($C_{TPG} = 100\text{ nF}$)	T_{PG}	100	300	500	ms
Power Good Threshold Voltage (Pin 11)	T_{PGth}	–	2.5	–	V

FAULT

Fault Sink Current	I_{FAULT}	20	–	–	mA
Fault Saturation Voltage ($I = 20\text{ mA}$)	$V_{FAULTsat}$	–	–	0.4	V
Fault Leakage Current ($V = 5.0\text{ V}$)	$I_{FAULTleak}$	–	–	1.0	μA
Fault Delay Time Before Latching	T_{FAULT}	–	100	–	μs

REMOTE CONTROL

Remote Input Voltage Threshold	V_{Rth}	–	1.28	–	V
Remote Hysteresis	V_{Rhys}	–	25	–	mV
Remote Pin Internal Pull-Up Voltage	V_{Rh}	3.3	3.4	3.6	V
Remote Low State Saturation Current	I_{RI}	–	–	0.5	mA
Remote Time Delay ($C_{REMOTE} = 100\text{ nF}$) Remote On	T_{REMon}	35	45	60	ms
Remote Off	T_{REMOff}	35	45	60	ms
Remote Delay Threshold Voltage (Pin 10) Low Level	$T_{REMth lo}$	–	0.2	–	V
High Level	$T_{REMth hi}$	–	2.3	–	V

VOLTAGE REFERENCE

Internal Voltage Reference ($I_O = 1.0\text{ mA}$) @ 25°C	V_{REF}	2.46	2.50	2.54	V
Internal Voltage Reference ($I_O = 1.0\text{ mA}$) 0°C to 85°C	V_{REF}	2.42	2.50	2.58	V
Line Regulation ($4.5\text{ V} < V_{CC} < 16\text{ V}$) $I_{out} = 0\text{ mA}$	$V_{REFline}$	–	4.0	10	mV
$I_{out} = 10\text{ mA}$	$V_{REFline}$	–	15	–	mV
Load Regulation ($V_{CC} = 5.0\text{ V}$) $0\text{ mA} < I_{out} < 10\text{ mA}$	$V_{REFload}$	–	25	–	mV

NCP112

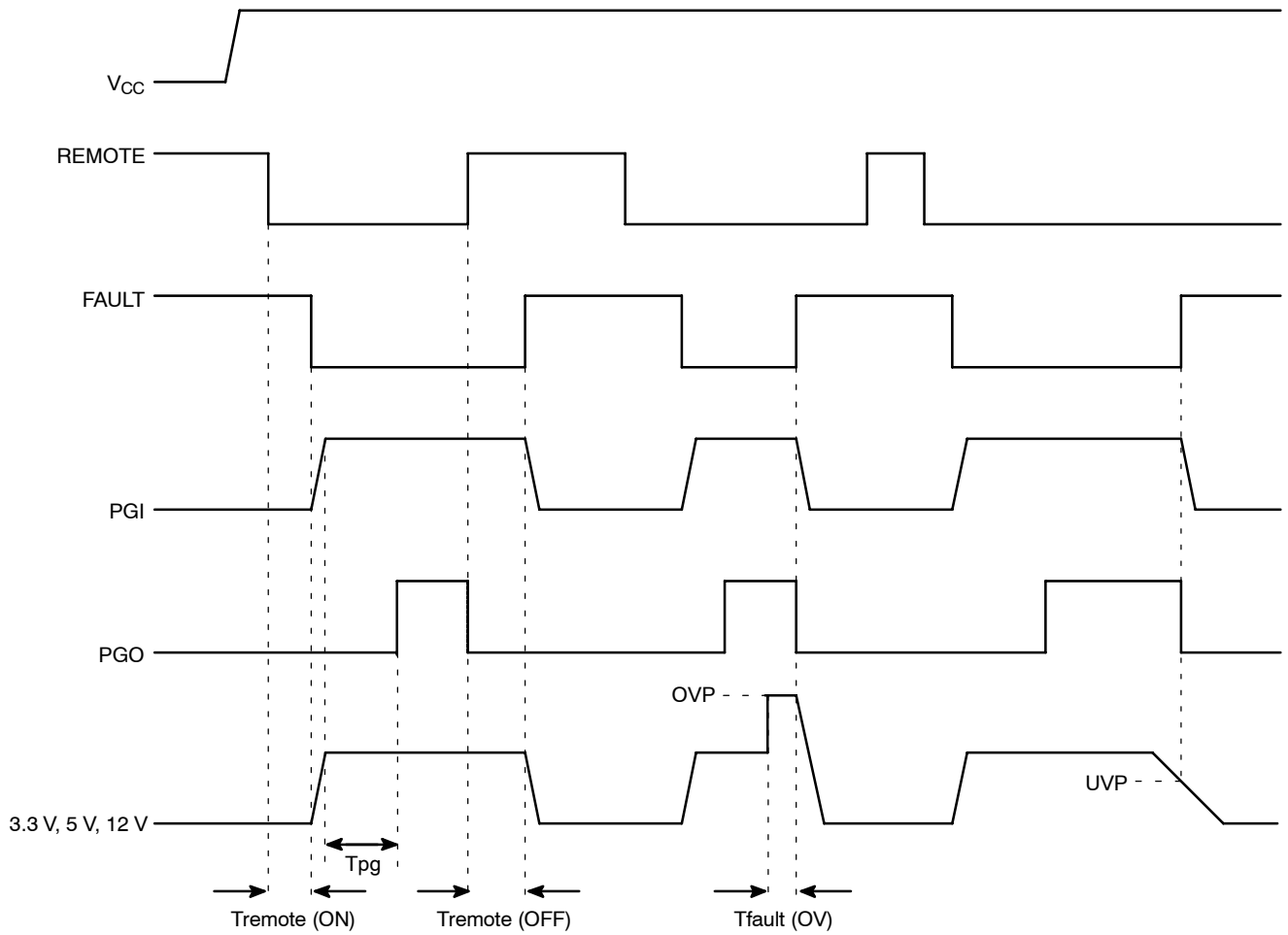


Figure 2. Timing Diagram

Table 1. FUNCTION TABLE

PGI	REMOTE	ADJ	Undervoltage	Overvoltage	FAULT	PGO
<1.28 V (L)	L	<1.28 V (L)	No	No	H	L
<1.28 V (L)	L	<1.28 V (L)	No	Yes	H	L
<1.28 V (L)	L	<1.28 V (L)	Yes	No	H	L
<1.28 V (L)	L	>1.28 V (H)	No	No	L	L
<1.28 V (L)	L	>1.28 V (H)	No	Yes	H	L
<1.28 V (L)	L	>1.28 V (H)	Yes	No	H	L
>1.28 V (H)	L	<1.28 V (L)	No	No	H	L
>1.28 V (H)	L	<1.28 V (L)	No	Yes	H	L
>1.28 V (H)	L	<1.28 V (L)	Yes	No	H	L
>1.28 V (H)	L	>1.28 V (H)	No	No	L	H
>1.28 V (H)	L	>1.28 V (H)	No	Yes	H	L
>1.28 V (H)	L	>1.28 V (H)	Yes	No	H	L
X	H	X	X	X	H	L

2. X = > Don't care.
3. FAULT = L means main PWM is Enable.
4. PGO = H means power supply is working within ATX specifications.

NCP112

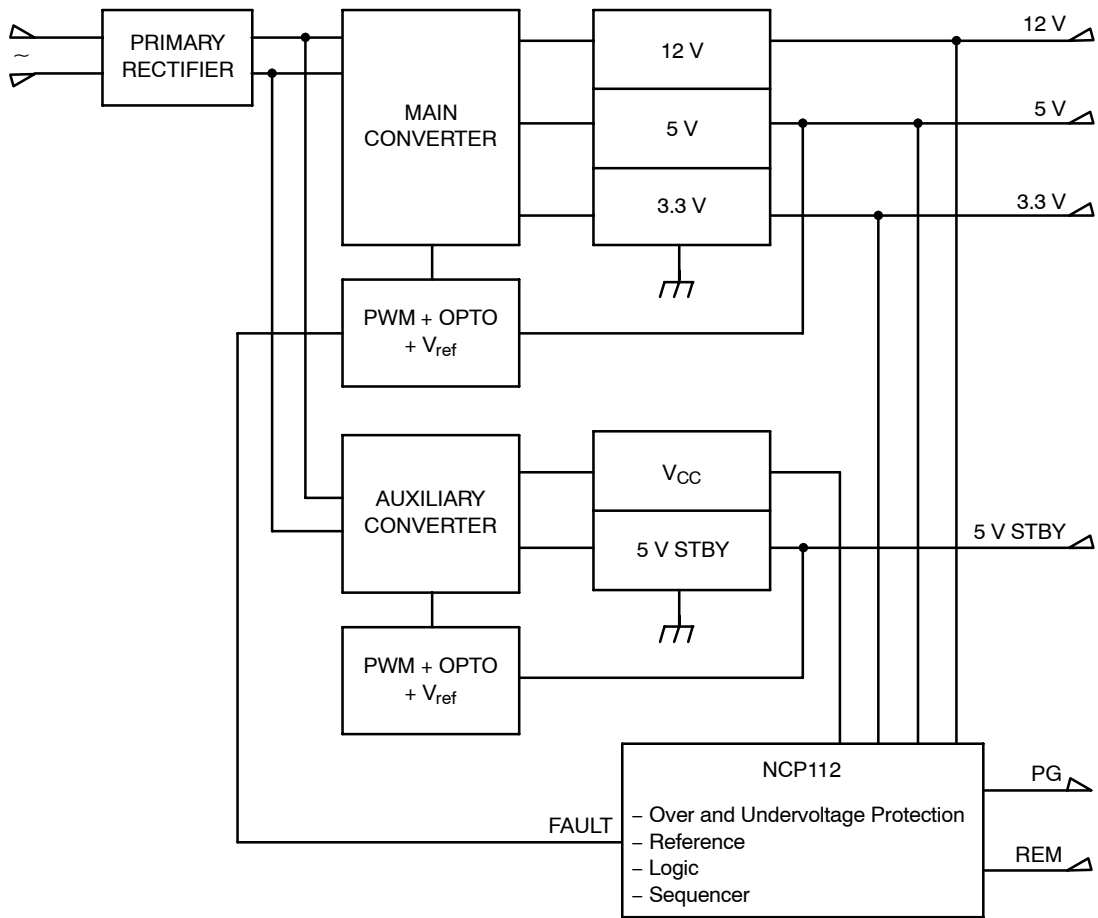


Figure 3. Simplified Application Schematic

NCP112

PIN FUNCTION DESCRIPTION

Main Line Sensing – VS33, VS5 and VS12

These pins are used to monitor the main power outputs. The internal circuitry of the NCP112 provides over and undervoltage detection and indicates an error state. The over and undervoltage levels meet the ATX specification. In order to avoid unexpected oscillation of the device, the NCP112 features both over and undervoltage hysteresis. The overvoltage detection circuitry incorporates a fault delay, which helps to filter short positive voltage spikes below 100 μ s. To avoid triggering a false undervoltage signal during power-up, a timing capacitor (CTUV) may be used to introduce a user defined blanking delay.

Additional Overvoltage Protection – ADJ

This pin can be used as another user-defined monitoring input and has a hysteresis feature similar to VS33, VS5 and VS12. When the input voltage is below the threshold level of 1.28 V, a fault condition is asserted. Note that the ADJ pin is logically ORed with the overvoltage detector output, thus there is a 100 μ s fault delay.

Power Good Input – PGI

The Power Good Input (PGI) can be used to monitor an additional logic event, for example, the temperature inside an ATX power supply unit. When the input voltage at the PGI input is below the threshold level of 1.28 V, the Power Good Output (PGO) signal remains in a low state, even if all three sense inputs are within voltage limits. The PGI signal, along with the REMOTE, and the over and undervoltage singles encounter a power good delay circuit as depicted in Figure 1.

Timing Capacitors – CTUV, CTREMOTE, CTPG

The NCP112 timing circuitry is optimized for utilizing low cost, 100 nF ceramic capacitors. The time delays of CTUV, CTREMOTE, and CTPG can be adjusted by simply changing external capacitor values. The time delay is a linear function of the capacitance because the NCP112 uses

internal current sources for charging and/or discharging capacitors.

Remote Control – REMOTE

A reset signal can be realized with the REMOTE pin. When the Remote pin is in the active low state, the external link (the Fault signal) between the NCP112 and the Pulse Width Modulator (PWM) generator of the external power supply is enabled (Figure 3). In order to effectively reset the latch, a minimum width remote pulse should be applied. The width of this pulse should be greater than T_{REM} , which is determined by adding an external capacitor (CTREMOTE). Note that the REMOTE pin is internally pulled up to 3.4 V.

Power Good Output – PGO

The purpose of the PGO function is to warn the motherboard that the voltage of at least one of the three main power lines is out of range, independent of the ADJ input. Please refer to Table 1 for a functional Truth table. The PGO is subject to a delay T_{PG} , which can be adjusted with an external capacitor (CTPG). The Power Good Output pin is capable of sinking 20 mA of current.

Fault Output – FAULT

In a typical application such as Figure 3, the fault pin (FAULT), is activated when any one of the three main power lines (3.3 V, 5.0 V, 12 V) is out of range or the ADJ pin is below 1.28 V. This is independent of the PGI input. The Fault output is the external link between the NCP112 and the primary PWM. In the event of a short circuit condition, the overvoltage circuitry provides an additional delay time T_{FAULT} which provides adequate protection.

Voltage Reference – VREF

The VREF is a 2.5V precision reference output, with current sourcing capability of 20 mA. No bypass capacitor or minimum output current is required to maintain stability.

ORDERING INFORMATION

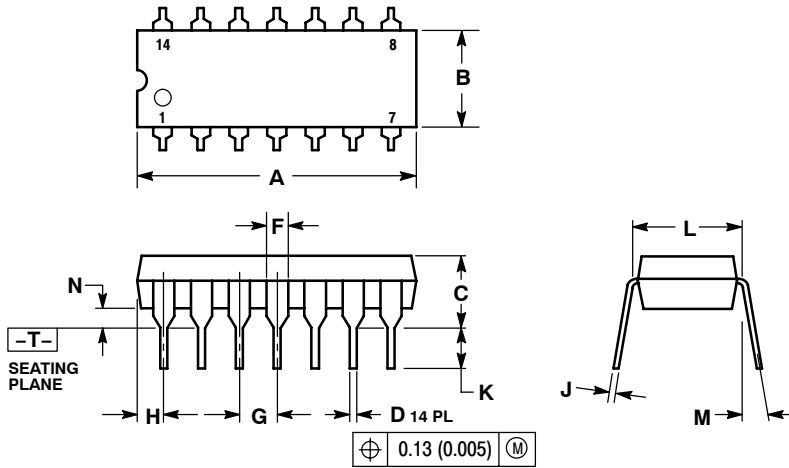
Device	Package	Shipping [†]
NCP112P	PDIP-14	25 Units / Rail
NCP112PG	PDIP-14 (Pb-Free)	
NCP112D	SOIC-14	55 Units / Rail
NCP112DG	SOIC-14 (Pb-Free)	
NCP112DR2	SOIC-14	2500 / Tape & Reel
NCP112DR2G	SOIC-14 (Pb-Free)	

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCP112

PACKAGE DIMENSIONS

PDIP-14
CASE 646-06
ISSUE P



NOTES:

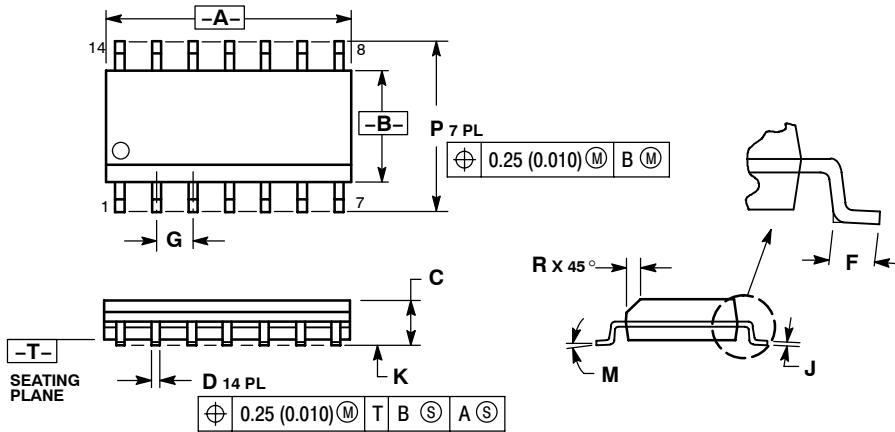
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10°	---	10°
N	0.015	0.039	0.38	1.01

NCP112

PACKAGE DIMENSIONS

SOIC-14
CASE 751A-03
ISSUE H

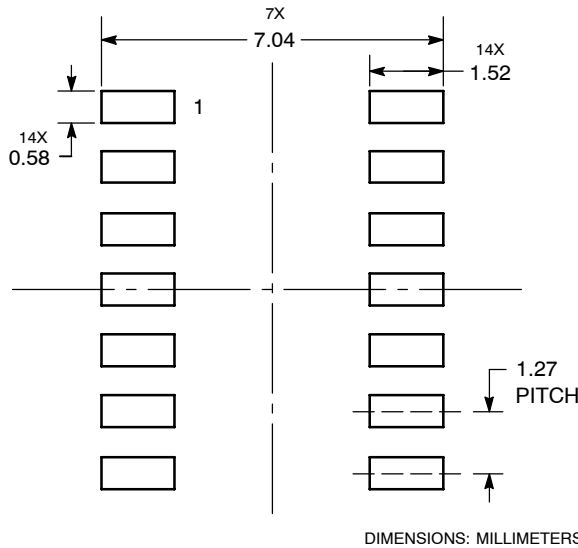


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	BSC	0.050	BSC
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative