16. ELECTRICAL SPECIFICATIONS

★ **Applied standard**

The electrical characteristics shown below are applied to devices other than the old models conforming to K mask.

Therefore, these characteristics are different from those conforming to the K mask. For the electrical characteristics of the K mask, consult NEC.

"Others" in the table below means products conforming to the masks other than E, P, X, and M (but conforming to the L mask).

16.1 AT 5 V OPERATION

★ **OPERATING RANGE**

	E, P, X, M mask model	Others
μPD70208H, 70216H-10/12/16	V_{DD} = 5 V ±10%	
μPD70208H, 70216H-20	—	V_{DD} = 5 V ±5%

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Test Conditions	Rating	Unit
Supply voltage	V_{DD}		−0.5 to +7.0	V
Input voltage	V_I	V_{DD} = 5 V ±10% (μPD70208H, 70216H-10/12/16) V_{DD} = 5 V ±10% (μPD70208H, 70216H-20)	−0.5 to V_{DD}+0.3	V
Clock input voltage	V_K		−0.5 to V_{DD}+1.0	V
Output voltage	V_O		−0.5 to V_{DD}+0.3	V
Operating ambient temperature	T_A		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

Cautions 1. **Do not directly connect the output pins of two or more IC products and do not directly connect the output pins to V_{DD} or V_{CC} and GND. However, open-drain pins or open-collector pins may be connected directly. Moreover, an external circuit whose timing is designed to avoid output collision can be connected to pins that go into a high-impedance state.**

2. **If even one of the above parameters exceeds the absolute maximum rating even momentarily, the quality of the program may be degraded. Absolute maximum ratings, therefore, are the values exceeding which the product may be physically damaged. Use the program keeping all the parameters within these rated values.**

The standards and conditions shown in DC and AC Characteristics below specify the range within which the normal operation of the product is guaranteed.

DC CHARACTERISTICS

(T_A = −40 to +85 °C, V_{DD} = 5 V ±10% (μPD70208H, 70216H-10/12/16), V_{DD} = 5 V ±5% (μPD70208H, 70216H-20))

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit	
Input voltage high	V_{IH}	E, P, X, M masks	Except $\overline{RESET}$	2.2		V_{DD}+0.3	V	
			$\overline{RESET}$	0.8 V_{DD}		V_{DD}+0.3		
		Others	Except $\overline{RESET}$, INTP1 to INTP7	2.2		V_{DD}+0.3		★
			$\overline{RESET}$	0.8 V_{DD}		V_{DD}+0.3		★
			INTP1 to INTP7	2.4		V_{DD}+0.3		★
Input voltage low	V_{IL}	Except $\overline{RESET}$		−0.5		+0.8	V	
		$\overline{RESET}$		−0.5		0.2V_{DD}		
Clock input voltage high	V_{KH}			3.9		V_{DD}+1.0	V	
Clock input voltage low	V_{KL}			−0.5		+0.6	V	
Output voltage high	V_{OH}	I_{OH} = −2.5 mA		0.7 V_{DD}			V	
		I_{OH} = −100 μA		V_{DD} − 0.4				
Output voltage low	V_{OL}	Except $\overline{END}/\overline{TC}$: I_{OL} = 2.5 mA				0.4	V	
		$\overline{END}/\overline{TC}$: I_{OL} = 5.0 mA						
Input leak current high	I_{LIH}	V_I = V_{DD}				10	μA	
Input leak current low	I_{LIL}	Except INTP : V_I = 0 V				−10	μA	
INTP input current low	I_{LIPL}	INTP input : V_I = 0 V				−300	μA	
Output leak current high	I_{LOH}	V_O = V_{DD}				10	μA	
Output leak current low	I_{LOL}	V_O = 0 V				−10	μA	
Latch leak current high	I_{LLH}	V_I = 3.0 V		−50		−300	μA	
Latch leak current low	I_{LLL}	V_I = 0.8 V		50		300	μA	
Latch inversion current (L → H)	I_{ILH}					400	μA	
Latch inversion current (H → L)	I_{ILL}					−400	μA	
Supply current[Note]	I_{DD}	E, P, X, M masks	On operation		5.5 fx	9.0 fx	mA	
			On standby (HALT)		1.5 fx	2.5 fx		
			On standby (STOP)			50	μA	
		Others	On operation		4.5 fx	6.0 fx	mA	★
			On standby (HALT)		1.5 fx	2.2 fx		★
			On standby (STOP)			50	μA	★

Note The unit of values of constans 1.5, 2.2, 2.5, 4.5, 5.5, 6.0 and 9.0 is mA/MHz.

CAPACITANCE (T_A = 25 °C, V_{DD} = 0 V) ★

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz			10	pF
Input/output capacitance	C_{IO}	0 V other than test pin.			15	pF

AC CHARACTERISTICS

(1) μPD70208H, 70216H-10/12/16 (T_A = −40 to +85 °C, V_{DD} = 5 V ±10%) (1/3)

Output Pin Load Capacitance: C_L = 100 pF

Parameter		Symbol		μPD70208H-10 μPD70216H-10		μPD70208H-12 μPD70216H-12		μPD70208H-16 μPD70216H-16		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
External clock input cycle		①	t_{CYX}	50	DC	40	DC	31.25	DC	ns
External clock input high-level width (V_{KH}=3.0 V)		②	t_{XXH}	19		14		12		ns
External clock input low-level width (V_{KL}=1.5 V)		③	t_{XXL}	19		14		12		ns
External clock input rise time (1.5→3.0 V)		④	t_{XR}		5		5		5	ns
External clock input fall time (3.0→1.5 V)		⑤	t_{XF}		5		5		5	ns
Clock output cycle		⑥	t_{CYK}	100	DC	80	DC	62.5	DC	ns
Clock output high-level width (V_{OH}=3.0 V)		⑦	t_{KKH}	0.5t_{CYK}−5		0.5t_{CYK}−5		0.5t_{CYK}−5		ns
Clock output low-level width (V_{OL}=1.5 V)		⑧	t_{KKL}	0.5t_{CYK}−5		0.5t_{CYK}−5		0.5t_{CYK}−5		ns
Clock output rise time (1.5→3.0 V)		⑨	t_{KR}		5		5		5	ns
Clock output fall time (3.0→1.5 V)		⑩	t_{KF}		5		5		5	ns
CLKOUT delay time (vs. external clock)		⑪	t_{DXK}		40		35		20	ns
Input rise time (except external clock) (0.8→2.2 V)		⑫	t_{IR}		15		15		15	ns
Input fall time (except external clock) (2.2→0.8 V)		⑬	t_{IF}		10		10		10	ns
Output rise time (except CLKOUT) (0.8→2.2 V)	E, P, X, M masks	⑭	t_{OR}		15		15		15	ns
★	Others				10		10		10	ns
Output fall time (except CLKOUT) (2.2→0.8 V)		⑮	t_{OF}		10		10		10	ns
$\overline{\text{RESET}}$ setup time (vs. CLKOUT↓)Note		⑯	t_{SRESK}	20		20		20		ns
$\overline{\text{RESET}}$ hold time (vs. CLKOUT↓)Note		⑰	t_{HKRES}	25		25		15		ns
RESOUT output delay time (vs. CLKOUT↓)		⑱	t_{DKRES}	5	50	5	40	5	30	ns
READY inactive setup time (vs. CLKOUT↑)		⑲	t_{SRYLK}	15		10		7		ns
READY inactive hold time (vs. CLKOUT↑)		⑳	t_{HKRYL}	20		15		15		ns
READY active setup time (vs. CLKOUT↑)		㉑	t_{SRYHK}	15		10		7		ns
READY active hold time (vs. CLKOUT↑)		㉒	t_{HKRYH}	20		20		15		ns
NMI setup time (vs. CLKOUT↑)		㉓	t_{SNMIK}	15		15		15		ns
POLL setup time (vs. CLKOUT↑)		㉔	t_{SPOLK}	20		20		20		ns
Data setup time (vs. CLKOUT↓)		㉕	t_{SDK}	15		10		7		ns
Data hold time (vs. CLKOUT↓)		㉖	t_{HKD}	5		5		5		ns
CLKOUT → address delay time		㉗	t_{DKA}	5	50	5	40	5	28	ns
CLKOUT → address hold time		㉘	t_{HKA}	10		10		10		ns
CLKOUT↓ → PS delay time		㉙	t_{DKP}	5	50	5	40	5	30	ns
CLKOUT↓ → PS float delay time		㉚	t_{FKP}	5	50	5	40	5	30	ns
Address setup time (vs. ASTB↓)		㉛	t_{SAST}	t_{KKL}−20		t_{KKL}−10		t_{KKL}−10		ns
CLKOUT↓ → address float delay time		㉜	t_{FKA}	t_{HKA}	50	t_{HKA}	40	t_{HKA}	30	ns
CLKOUT↓ → ASTB↑ delay time		㉝	t_{DKSTH}		40		30		25	ns

Note When reset with the minimum pulse width or when guaranteeing the RESOUT output timing.

(1) μPD70208H, 70216H-10/12/16 (T_A = −40 to +85 °C, V_{DD} = 5 V ±10%) (2/3)

Output Pin Load Capacitance: C_L = 100 pF

Parameter		Symbol		μPD70208H-10 μPD70216H-10		μPD70208H-12 μPD70216H-12		μPD70208H-16 μPD70216H-16		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
CLKOUT↑ → ASTB↓ delay time		㉞	t_{DKSTL}		45		35		30	ns
ASTB high-level width		㉟	t_{STST}	t_{KKL}−10		t_{KKL}−10		t_{KKL}−10		ns
ASTB↓ → address hold time		㊱	t_{HSTA}	t_{KKH}−20		t_{KKH}−10		t_{KKH}−10		ns
CLKOUT → control 1[Note 1] delay time		㊲	t_{DKCT1}	5	60	5	50	5	40	ns
CLKOUT → control 2[Note 2] delay time		㊳	t_{DKCT2}	5	55	5	45	5	35	ns
Address float → $\overline{RD}$↓ delay time		㊴	t_{DAFRL}	0		0		0		ns
CLKOUT↓ → $\overline{RD}$↓ delay time		㊵	t_{DKRL}	5	65	5	50	5	40	ns
CLKOUT↓ → $\overline{RD}$↑ delay time		㊶	t_{DKRH}	5	60	5	45	5	35	ns
$\overline{RD}$↑ → address delay time		㊷	t_{DRHA}	t_{CYK}−40		t_{CYK}−20		t_{CYK}−10		ns
$\overline{RD}$ low-level width		㊸	t_{RR}	2t_{CYK}−40		2t_{CYK}−20		2t_{CYK}−20		ns
$\overline{BUFEN}$↑ → BUF$\overline{R}$/W delay time (read cycle)		㊹	t_{DBECT}	t_{KKL}−20		t_{KKL}−10		t_{KKL}−10		ns
CLKOUT↓ → data output delay time		㊺	t_{DKD}	5	55	5	40	5	30	ns
CLKOUT↓ → data float delay time		㊻	t_{FKD}	5	55	5	40	5	30	ns
$\overline{WR}$ low-level width		㊼	t_{WW}	2t_{CYK}−40		2t_{CYK}−20		2t_{CYK}−20		ns
$\overline{WR}$↑ → $\overline{BUFEN}$↑ or BUF$\overline{R}$/W↓ (write cycle)		㊽	t_{DWCT}	t_{KKL}−20		t_{KKL}−10		t_{KKL}−10		ns
CLKOUT↑ → BS↓ delay time		㊾	t_{DKBL}	5	55	5	40	5	30	ns
CLKOUT↓ → BS↑ delay time		㊿	t_{DKBH}	5	55	5	40	5	30	ns
HLDRQ setup time (vs. CLKOUT↓)		(51)	t_{SHQK}	15		10		7		ns
CLKOUT↓ → HLDAK delay time		(52)	t_{DKHA}	5	60	5	50	5	40	ns
CLKOUT↑ → $\overline{DMAAK}$ delay time		(53)	t_{DKHDA}	5	55	5	45	5	35	ns
CLKOUT↓ → $\overline{DMAAK}$ delay time (cascade mode)		(54)	t_{DKLDA}	5	80	5	70	5	55	ns
$\overline{WR}$ low-level width (DMA cycle)	DMA expansion write	(55)	t_{WW1}	2t_{CYK}−40		2t_{CYK}−20		2t_{CYK}−20		ns
	DMA normal write	(56)	t_{WW2}	t_{CYK}−40		t_{CYK}−20		t_{CYK}−15		ns
$\overline{RD}$↓, $\overline{WR}$↓ delay time (vs. $\overline{DMAAK}$↓)		(57)	t_{DDARW}	t_{KKH}−30		t_{KKH}−20		t_{KKH}−15		ns
$\overline{DMAAK}$↑ delay time (vs. $\overline{RD}$↑)		(58)	t_{DRHDAH}	t_{KKL}−30		t_{KKL}−20		t_{KKL}−15		ns
$\overline{RD}$↑ delay time (vs. $\overline{WR}$↑)		(59)	t_{DWHRH}	3		3		3		ns
$\overline{TC}$ output delay time (vs. CLKOUT↑)		(60)	t_{DKTCL}		55		45		35	ns
$\overline{TC}$ OFF delay time (vs. CLKOUT↑)		(61)	t_{DKTCF}		55		45		35	ns
$\overline{TC}$ low-level width		(62)	t_{TCTCL}	t_{CYK}−15		t_{CYK}−10		t_{CYK}−10		ns
$\overline{TC}$ pull-up delay time (vs. CLKOUT↑)		(63)	t_{DKTCH}		Note 3		Note 4		Note 4	ns
$\overline{END}$ setup time (vs. CLKOUT↑)		(64)	t_{SEDK}	30		25		20		ns
$\overline{END}$ low-level width		(65)	t_{EDEDL}	80		65		50		ns
DMARQ setup time (vs. CLKOUT↑)		(66)	t_{SDQK}	30		20		15		ns
INTPn low-level width		(67)	t_{IPIPL}	80		80		80		ns
RxD setup time (vs. SCU internal clock↓)		(68)	t_{SRX}	500		500		500		ns

Notes 1. $\overline{MWR}$ and $\overline{IOWR}$ signals in DMA cycle

2. $\overline{MWR}$ and $\overline{IOWR}$ signals in $\overline{BUFEN}$, BUF$\overline{R}$/W, $\overline{INTAK}$, $\overline{REFRQ}$ and CPU cycles.

3. t_{KKH}+2t_{CYK} − 10 (Reference value when a 1.1-kΩ pull-up resistor is connected.)

4. t_{KKH}+2t_{CYK} − 5 (Reference value when a 1.1-kΩ pull-up resistor is connected.)

(1) μPD70208H, 70216H-10/12/16 (T_A = −40 to +85 °C, V_{DD} = 5 V ±10%) (3/3)

Output Pin Load Capacitance: C_L = 100 pF

	Parameter	Symbol		μPD70208H-10 μPD70216H-10		μPD70208H-12 μPD70216H-12		μPD70208H-16 μPD70216H-16		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
	RxD hold time (vs. SCU internal clock↓)	⑥⑨	t_{HRX}	500		500		500		ns
	CLKOUT↓ → $\overline{SRDY}$ delay time	⑦⓪	t_{DKSR}		100		100		100	ns
	TOUT1↓ → TxD delay time	⑦①	t_{DTX}		200		200		200	ns
	TCTL2 setup time (vs. CLKOUT↓)	⑦②	t_{SGK}	40		40		40		ns
	TCTL2 setup time (vs. TCLK↑)	⑦③	t_{SGTK}	40		40		40		ns
	TCTL2 hold time (vs. CLKOUT↓)	⑦④	t_{HKG}	80		80		80		ns
	TCTL2 hold time (vs. TCLK↑)	⑦⑤	t_{HTKG}	40		40		40		ns
	TCTL2 high-level width	⑦⑥	t_{GGH}	40		40		40		ns
	TCTL2 low-level width	⑦⑦	t_{GGL}	40		40		40		ns
	TOUT output delay time (vs. CLKOUT↓)	⑦⑧	t_{DKTO}		150		150		150	ns
	TOUT output delay time (vs. TCLK↓)	⑦⑨	t_{DTKTO}		100		100		100	ns
	TOUT output delay time (vs. TCTL2↓)	⑧⓪	t_{DGTO}		90		90		90	ns
	TCLK rise time	⑧①	t_{TKR}		25		25		25	ns
	TCLK fall time	⑧②	t_{TKF}		25		25		25	ns
	TCLK high-level width	⑧③	t_{TKTKH}	45		40		30		ns
	TCLK low-level width	⑧④	t_{TKTKL}	45		40		30		ns
	TCLK cycle	⑧⑤	t_{CYTK}	100	DC	80	DC	62.5	DC	ns
	Access interval[Note 1]	⑧⑥	t_{AI}	$2t_{CYK}$−40		$2t_{CYK}$−25		$2t_{CYK}$−20		ns
	$\overline{REFRQ}$↑ delay time (vs. $\overline{MRD}$↑)[Note 2]	⑧⑦	t_{DRQHRH}	t_{KKL}−30		t_{KKL}−15		t_{KKL}−10		ns
★	$\overline{RESET}$ pulse width[Note 3]	⑧⑧	t_{WRESL}	$4t_{CYK}$		$4t_{CYK}$		$4t_{CYK}$		ns

Notes 1. Specification to guarantee read/write recovery time for I/O device.

2. Specification to guarantee that $\overline{REFRQ}$↑ is always later than $\overline{MRD}$↑.
   Only guaranteed when the EREF bit of the SCTL register is 0.

3. The oscillation stabilization time must be added when the power-ON reset or STOP mode has been released. Because the oscillation stabilization time varies depending on the characteristics of the oscillator and oscillation circuit used, evaluate the oscillation stabilization time with the oscillator and oscillation circuit actually used.

(2) μPD70208H, 70216H-20 (T_A = −40 to +85 °C, V_{DD} = 5 V ±5%) (1/3) ★

Output Pin Load Capacitance: C_L = 100 pF

Parameter	Symbol		μPD70208H-20 μPD70216H-20		Unit
			MIN.	MAX.	
External clock input cycle	①	t_{CYX}	25	DC	ns
External clock input high-level width (V_{KH}=3.0 V)	②	t_{XXH}	10		ns
External clock input low-level width (V_{KL}=1.5 V)	③	t_{XXL}	10		ns
External clock input rise time (1.5→3.0 V)	④	t_{XR}		5	ns
External clock input fall time (3.0→1.5 V)	⑤	t_{XF}		5	ns
Clock output cycle	⑥	t_{CYK}	50	DC	ns
Clock output high-level width (V_{OH}=3.0 V)	⑦	t_{KKH}	0.5t_{CYK}−5		ns
Clock output low-level width (V_{OL}=1.5 V)	⑧	t_{KKL}	0.5t_{CYK}−5		ns
Clock output rise time (1.5→3.0 V)	⑨	t_{KR}		5	ns
Clock output fall time (3.0→1.5 V)	⑩	t_{KF}		5	ns
CLKOUT delay time (vs. external clock)	⑪	t_{DXK}		20	ns
Input rise time (except external clock) (0.8→2.2 V)	⑫	t_{IR}		15	ns
Input fall time (except external clock) (2.2→0.8 V)	⑬	t_{IF}		10	ns
Output rise time (except CLKOUT) (0.8→2.2 V)	⑭	t_{OR}		10	ns
Output fall time (except CLKOUT) (2.2→0.8 V)	⑮	t_{OF}		10	ns
$\overline{\text{RESET}}$ setup time (vs. CLKOUT↓)[Note]	⑯	t_{SRESK}	20		ns
$\overline{\text{RESET}}$ hold time (vs. CLKOUT↓)[Note]	⑰	t_{HKRES}	10		ns
RESOUT output delay time (vs. CLKOUT↓)	⑱	t_{DKRES}	5	25	ns
READY inactive setup time (vs. CLKOUT↑)	⑲	t_{SRYLK}	7		ns
READY inactive hold time (vs. CLKOUT↑)	⑳	t_{HKRYL}	10		ns
READY active setup time (vs. CLKOUT↑)	㉑	t_{SRYHK}	7		ns
READY active hold time (vs. CLKOUT↑)	㉒	t_{HKRYH}	10		ns
NMI setup time (vs. CLKOUT↑)	㉓	t_{SNMIK}	10		ns
POLL setup time (vs. CLKOUT↑)	㉔	t_{SPOLK}	20		ns
Data setup time (vs. CLKOUT↓)	㉕	t_{SDK}	7		ns
Data hold time (vs. CLKOUT↓)	㉖	t_{HKD}	5		ns
CLKOUT → address delay time	㉗	t_{DKA}	5	25	ns
CLKOUT → address hold time	㉘	t_{HKA}	10		ns
CLKOUT ↓ → PS delay time	㉙	t_{DKP}	5	30	ns
CLKOUT ↓ → PS float delay time	㉚	t_{FKP}	5	30	ns
Address setup time (vs. ASTB↓)	㉛	t_{SAST}	t_{KKL}−10		ns
CLKOUT ↓ → address float delay time	㉜	t_{FKA}	t_{HKA}	25	ns
CLKOUT ↓ → ASTB ↑ delay time	㉝	t_{DKSTH}		20	ns
CLKOUT ↑ → ASTB ↓ delay time	㉞	t_{DKSTL}		20	ns
ASTB high-level width	㉟	t_{STST}	t_{KKL}−10		ns

Note When reset with the minimum pulse width or when guaranteeing the RESOUT output timing.

★ **(2) μPD70208H, 70216H-20 (T_A = −40 to +85 °C, V_{DD} = 5 V ±5%) (2/3)**

Output Pin Load Capacitance: C_L = 100 pF

Parameter		Symbol		μPD70208H-20 μPD70216H-20 MIN.	μPD70208H-20 μPD70216H-20 MAX.	Unit
ASTB ↓ → address hold time		㊱	t_{HSTA}	t_{KKH}−10		ns
CLKOUT → control 1[Note 1] delay time		㊲	t_{DKCT1}	5	25	ns
CLKOUT → control 2[Note 2] delay time		㊳	t_{DKCT2}	5	30	ns
Address float → $\overline{RD}$ ↓ delay time		㊴	t_{DAFRL}	0		ns
CLKOUT ↓ → $\overline{RD}$ ↓ delay time		㊵	t_{DKRL}	5	25	ns
CLKOUT ↓ → $\overline{RD}$ ↑ delay time		㊶	t_{DKRH}	5	28	ns
$\overline{RD}$ ↑ → address delay time		㊷	t_{DRHA}	t_{CYK}−5		ns
$\overline{RD}$ low-level width		㊸	t_{RR}	2t_{CYK}−15		ns
$\overline{BUFEN}$ ↑ → BUF$\overline{R}$/W delay time (read cycle)		㊹	t_{DBECT}	t_{KKL}−10		ns
CLKOUT ↓ → data output delay time		㊺	t_{DKD}	5	25	ns
CLKOUT ↓ → data float delay time		㊻	t_{FKD}	5	25	ns
$\overline{WR}$ low-level width		㊼	t_{WW}	2t_{CYK}−15		ns
$\overline{WR}$ ↑ → $\overline{BUFEN}$ ↑ or BUF$\overline{R}$/W ↓ (write cycle)		㊽	t_{DWCT}	t_{KKL}−10		ns
CLKOUT ↑ → BS ↓ delay time		㊾	t_{DKBL}	5	30	ns
CLKOUT ↓ → BS ↑ delay time		㊿	t_{DKBH}	5	25	ns
HLDRQ setup time (vs. CLKOUT ↓)		(51)	t_{SHQK}	7		ns
CLKOUT ↓ → HLDAK delay time		(52)	t_{DKHA}	5	25	ns
CLKOUT ↑ → $\overline{DMAAK}$ delay time		(53)	t_{DKHDA}	5	25	ns
CLKOUT ↓ → $\overline{DMAAK}$ delay time (cascade mode)		(54)	t_{DKLDA}	5	45	ns
$\overline{WR}$ low-level width (DMA cycle)	DMA expansion write	(55)	t_{WW1}	2t_{CYK}−15		ns
	DMA normal write	(56)	t_{WW2}	t_{CYK}−15		ns
$\overline{RD}$ ↓, $\overline{WR}$ ↓ delay time (vs. $\overline{DMAAK}$ ↓)		(57)	t_{DDARW}	t_{KKH}−10		ns
$\overline{DMAAK}$ ↑ delay time (vs. $\overline{RD}$ ↑)		(58)	t_{DRHDAH}	t_{KKL}−10		ns
$\overline{RD}$ ↑ delay time (vs. $\overline{WR}$ ↑)		(59)	t_{DWHRH}	3		ns
$\overline{TC}$ output delay time (vs. CLKOUT ↑)		(60)	t_{DKTCL}		25	ns
$\overline{TC}$ OFF delay time (vs. CLKOUT ↑)		(61)	t_{DKTCF}		25	ns
$\overline{TC}$ low-level width		(62)	t_{TCTCL}	t_{CYK}−10		ns
$\overline{TC}$ pull-up delay time (vs. CLKOUT ↑)		(63)	t_{DKTCH}		Note 3	ns
$\overline{END}$ setup time (vs. CLKOUT ↑)		(64)	t_{SEDK}	20		ns
$\overline{END}$ low-level width		(65)	t_{EDEDL}	40		ns
DMARQ setup time (vs. CLKOUT ↑)		(66)	t_{SDQK}	10		ns
INTPn low-level width		(67)	t_{IPIPL}	60		ns
RxD setup time (vs. SCU internal clock ↓)		(68)	t_{SRX}	500		ns
RxD hold time (vs. SCU internal clock ↓)		(69)	t_{HRX}	500		ns
CLKOUT ↓ → $\overline{SRDY}$ delay time		(70)	t_{DKSR}		100	ns

Notes 1. $\overline{MWR}$ and $\overline{IOWR}$ signals in $\overline{DMA}$ cycle

2. $\overline{MWR}$ and $\overline{IOWR}$ signals in $\overline{BUFEN}$, BUF$\overline{R}$/W, $\overline{INTAK}$, $\overline{REFRQ}$, and CPU cycles

3. t_{KKH} + 2t_{CYK} = 5 (reference value when a 1.1-kΩ pull-up resistor is connected)

(2) μPD70208H, 70216H-20 (T_A = −40 to +85 °C, V_{DD} = 5 V ±5%) (3/3) ★

Output Pin Load Capacitance: C_L = 100 pF

Parameter	Symbol		μPD70208H-20 μPD70216H-20		Unit
			MIN.	MAX.	
TOUT1 ↓ → TxD delay time	⑦①	t_{DTX}		200	ns
TCTL2 setup time (vs. CLKOUT ↓)	⑦②	t_{SGK}	40		ns
TCTL2 setup time (vs. TCLK ↑)	⑦③	t_{SGTK}	40		ns
TCTL2 hold time (vs. CLKOUT ↓)	⑦④	t_{HKG}	80		ns
TCTL2 hold time (vs. TCLK ↑)	⑦⑤	t_{HTKG}	40		ns
TCTL2 high-level width	⑦⑥	t_{GGH}	40		ns
TCTL2 low-level width	⑦⑦	t_{GGL}	40		ns
TOUT output delay time (vs. CLKOUT ↓)	⑦⑧	t_{DKTO}		150	ns
TOUT output delay time (vs. TCLK ↓)	⑦⑨	t_{DTKTO}		100	ns
TOUT output delay time (vs. TCTL2 ↓)	⑧⓪	t_{DGTO}		90	ns
TCLK rise time	⑧①	t_{TKR}		25	ns
TCLK fall time	⑧②	t_{TKF}		25	ns
TCLK high-level width	⑧③	t_{TKTKH}	23		ns
TCLK low-level width	⑧④	t_{TKTKL}	23		ns
TCLK cycle	⑧⑤	t_{CYTK}	50	DC	ns
Access interval[Note 1]	⑧⑥	t_{AI}	$2t_{CYK}$−15		ns
$\overline{\text{REFRQ}}$ ↑ delay time (vs. $\overline{\text{MRD}}$ ↑)[Note 2]	⑧⑦	t_{DRQHRH}	t_{KKL}−10		ns
$\overline{\text{RESET}}$ pulse width[Note 3]	⑧⑧	t_{WRESL}	$4t_{CYK}$		ns

Notes 1. This rating is to guarantee the read/write recovery time for the I/O device.

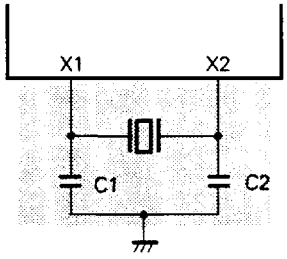
2. This rating is to guarantee that $\overline{\text{REFRQ}}$ ↑ is always behind $\overline{\text{MRD}}$ ↑, and guaranteed only when the EREF bit of the STCL register is 0.

3. The oscillation stabilization time must be added when the power-ON reset or STOP mode has been released. Because the oscillation stabilization time varies depending on the characteristics of the oscillator and oscillation circuit used, evaluate the oscillation stabilization time with the oscillator and oscillation circuit actually used.

★ **RECOMMENDED OSCILLATION CIRCUIT**

The clock input circuits (1) and (2) shown below are recommended.

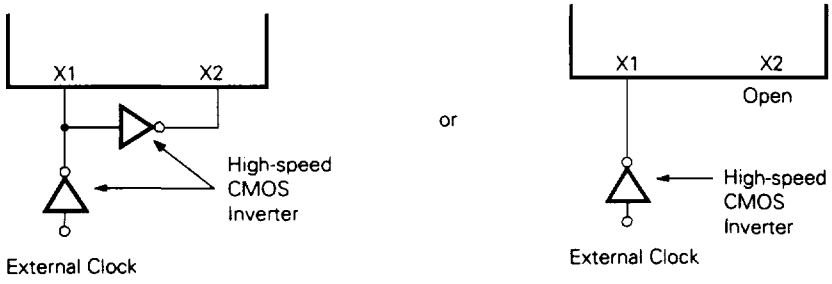
(1) Ceramic resonator connection (T_A = −40 to +85 °C, V_{DD} = 5 V ±10% (μPD70208H, 70216H-10/12/16), V_{DD} = 5 V ±5% (μPD70208H, 70216H-20))



Manufacturer	Frequency (fxx) [MHz]	Product Name	Recommended Constant	
			C1 [pF]	C2 [pF]
Murata Mfg. Co., Ltd.	40	CSA40.00MXZ040	3	3
	32	CSA32.00MXZ040	5	5
	25	CSA25.00MXZ040	5	5
	20	CSA20.00MXZ040	10	10
TDK Corporation	32	FCR32.0M2G	5	5
	25	FCR25.0M2G	5	5
	20	FCR20.0M2G	10	10

Cautions
1. **The oscillation circuit should be as close as possible to the X1 and X2 pins.**
2. ***No other signal lines should pass through the shaded area.***
3. **For matching between V40HL, V50HL and resonator, the efficient evaluation should be carried out.**

(2) External clock input



Caution The high-speed CMOS inverter should be as close as possible to the X1 and X2 pins.

16.2 AT 3 V OPERATION

OPERATING RANGE ★

	E, P, X, M masks	Others
μPD70208H, 70216H-10/12/16	V_{DD} = 3 V ±10%	
μPD70208H, 70216H-20	—	V_{DD} = 3 V ±10%

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

Parameter	Symbol	Test Conditions	Rating	Unit
Supply voltage	V_{DD}		−0.5 to +7.0	V
Input voltage	V_I	V_{DD} = 3 V ±10%	−0.5 to V_{DD}+0.3	V
Clock input voltage	V_K		−0.5 to V_{DD}+1.0	V
Output voltage	V_O		−0.5 to V_{DD}+0.3	V
Operating ambient temperature	T_A		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

Cautions 1. Do not directly connect the output pins of two or more IC products and do not directly connect the output pins to V_{DD} or V_{CC} and GND. However, open-drain pins or open-collector pins may be connected directly. Moreover, an external circuit whose timing is designed to avoid output collision can be connected to pins that go into a high-impedance state.

2. If even one of the above parameters exceeds the absolute maximum rating even momentarily, the quality of the program may be degraded. Absolute maximum ratings, therefore, are the values exceeding which the product may be physically damaged. Use the program keeping all the parameters within these rated values.

The standards and conditions shown in DC and AC Characteristics below specify the range within which the normal operation of the product is guaranteed.

DC CHARACTERISTICS (T_A = −40 to +85 °C, V_{DD} = 3 V ±10%)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH}	Except $\overline{\text{RESET}}$		0.7 V_{DD}		V_{DD}+0.3	V
		$\overline{\text{RESET}}$		0.8 V_{DD}		V_{DD}+0.3	
Input voltage low	V_{IL}	Except $\overline{\text{RESET}}$		−0.5		0.2 V_{DD}	V
		$\overline{\text{RESET}}$					
Clock input voltage high	V_{KH}			0.8 V_{DD}		V_{DD}+0.5	V
Clock input voltage low	V_{KL}			−0.5		0.2 V_{DD}	V
Output voltage high	V_{OH}	I_{OH} = −2.5 mA		0.7 V_{DD}			V
		I_{OH} = −100 μA		V_{DD} − 0.4			
Output voltage low	V_{OL}	Except $\overline{\text{END/TC}}$: I_{OL} = 2.5 mA				0.4	V
		$\overline{\text{END/TC}}$: I_{OL} = 5.0 mA					
Input leak current high	I_{LIH}	V_I = V_{DD}				10	μA
Input leak current low	I_{LIL}	V_I = 0 V : Except INTP				−10	μA
INTP input current low	I_{LIPL}	V_I = 0 V : INTP input				−300	μA
Output leak current high	I_{LOH}	V_O = V_{DD}				10	μA
Output leak current low	I_{LOL}	V_O = 0 V				−10	μA
Latch leak current high	I_{LLH}	V_I = 3.0 V		−50		−300	μA
Latch leak current low	I_{LLL}	V_I = 0.8 V		50		300	μA
Latch inversion current (L → H)	I_{ILH}					400	μA
Latch inversion current (H → L)	I_{ILL}					−400	μA
Supply current[Note]	I_{DD}	E, P, X, M masks	On Operation		3.0 fx	5.5 fx	mA
			On standby (HALT)		0.9 fx	1.5 fx	
			On standby (STOP)			30	μA
★		Others	On Operation		2.5 fx	4.0 fx	mA
★			On standby (HALT)		0.9 fx	1.5 fx	
★			On standby (STOP)			30	μA

Note The unit of constan values 0.9, 1.5, 2.5, 3.0, 4.0 and 5.5 is mA/MHz.

★ **CAPACITANCE (T_A = 25°C, V_{DD} = 0 V)**

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz			10	pF
Input/output capacitance	C_{IO}	0 V other than test pin.			15	pF

AC CHARACTERISTICS

(1) μPD70208H, 70216H-10/12/16 (T_A = −40 to +85 °C, V_{DD} = 3 V ±10%) (1/3)

Output Pin Load Capacitance: C_L = 100 pF

Parameter	Symbol		μPD70208H-10 μPD70216H-10		μPD70208H-12 μPD70216H-12		μPD70208H-16 μPD70216H-16		Unit	
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
External clock input cycle	①	t_{CYX}	100	DC	83	DC	62.5	DC	ns	
External clock input high-level width (V_{KH}=0.8 V_{DD})	②	t_{XXH}	40		30		20		ns	★
External clock input low-level width (V_{KL}=0.2 V_{DD})	③	t_{XXL}	40		30		20		ns	★
External clock input rise time (0.2 V_{DD}→0.8 V_{DD})	④	t_{XR}		10		10		10	ns	★
External clock input fall time (0.8 V_{DD}→0.2 V_{DD})	⑤	t_{XF}		10		10		10	ns	★
Clock output cycle	⑥	t_{CYK}	200	DC	166	DC	125	DC	ns	
Clock output high-level width (V_{OH}=0.7 V_{DD})	⑦	t_{KKH}	0.5t_{CYK}−7		0.5t_{CYK}−7		0.5t_{CYK}−7		ns	★
Clock output low-level width (V_{OL}=0.2 V_{DD})	⑧	t_{KKL}	0.5t_{CYK}−7		0.5t_{CYK}−7		0.5t_{CYK}−7		ns	★
Clock output rise time (0.2 V_{DD}→0.7 V_{DD})	⑨	t_{KR}		7		7		7	ns	★
Clock output fall time (0.7 V_{DD}→0.2 V_{DD})	⑩	t_{KF}		7		7		7	ns	★
CLKOUT delay time (vs. external clock)	⑪	t_{DXK}		75		65		55	ns	
Input rise time (except external clock) (0.2 V_{DD}→0.7 V_{DD})	⑫	t_{IR}		20		20		20	ns	★
Input fall time (except external clock) (0.7 V_{DD}→0.2 V_{DD})	⑬	t_{IF}		12		12		12	ns	★
Output rise time (except CLKOUT) (0.2 V_{DD}→0.7 V_{DD})	⑭	t_{OR}		20		20		20	ns	★
Output fall time (except CLKOUT) (0.7 V_{DD}→0.2 V_{DD})	⑮	t_{OF}		12		12		12	ns	★
$\overline{\text{RESET}}$ setup time (vs. CLKOUT↓)[Note]	⑯	t_{SRESK}	25		25		25		ns	
$\overline{\text{RESET}}$ hold time (vs. CLKOUT↓)[Note]	⑰	t_{HKRES}	35		35		35		ns	
RESOUT output delay time (vs. CLKOUT↓)	⑱	t_{DKRES}	5	80	5	70	5	60	ns	
READY inactive setup time (vs. CLKOUT↑)	⑲	t_{SRYLK}	20		20		15		ns	
READY inactive hold time (vs. CLKOUT↑)	⑳	t_{HKRYL}	30		30		25		ns	
READY active setup time (vs. CLKOUT↑)	㉑	t_{SRYHK}	20		20		15		ns	
READY active hold time (vs. CLKOUT↑)	㉒	t_{HKRYH}	30		30		25		ns	
NMI setup time (vs. CLKOUT↑)	㉓	t_{SNMIK}	15		15		15		ns	
POLL setup time (vs. CLKOUT↑)	㉔	t_{SPOLK}	20		20		20		ns	
Data setup time (vs. CLKOUT↓)	㉕	t_{SDK}	20		20		15		ns	
Data hold time (vs. CLKOUT↓)	㉖	t_{HKD}	5		5		5		ns	
CLKOUT → address delay time	㉗	t_{DKA}	5	75	5	65	5	55	ns	
CLKOUT → address hold time	㉘	t_{HKA}	10		10		10		ns	
CLKOUT↓ → PS delay time	㉙	t_{DKP}	5	80	5	70	5	60	ns	
CLKOUT↓ → PS float delay time	㉚	t_{FKP}	5	80	5	70	5	60	ns	
Address setup time (vs. ASTB↓)	㉛	t_{SAST}	t_{KKL}−30		t_{KKL}−30		t_{KKL}−30		ns	
CLKOUT↓ → address float delay time	㉜	t_{FKA}	5	80	5	70	5	60	ns	
CLKOUT↓ → ASTB↑ delay time	㉝	t_{DKSTH}	5	65	5	55	5	45	ns	
CLKOUT↑ → ASTB↓ delay time	㉞	t_{DKSTL}	5	70	5	60	5	50	ns	
ASTB high-level width	㉟	t_{STST}	t_{KKL}−10		t_{KKL}−10		t_{KKL}−10		ns	

Note When reset with the minimum pulse width or when guaranteeing the RESOUT output timing.

(1) μPD70208H, 70216H-10/12/16 (T_A = −40 to +85 °C, V_{DD} = 3 V ±10%) (2/3)

Output Pin Load Capacitance: C_L = 100 pF

Parameter		Symbol		μPD70208H-10 μPD70216H-10		μPD70208H-12 μPD70216H-12		μPD70208H-16 μPD70216H-16		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
ASTB↓ → address hold time		㊱	t_{HSTA}	t_{KKH}−30		t_{KKH}−30		t_{KKH}−20		ns
CLKOUT → control 1[Note 1] delay time		㊲	t_{DKCT1}	5	90	5	80	5	70	ns
CLKOUT → control 2[Note 2] delay time		㊳	t_{DKCT2}	5	80	5	70	5	60	ns
Address float → $\overline{RD}$↓ delay time		㊴	t_{DAFRL}	0		0		0		ns
CLKOUT↓ → $\overline{RD}$↓ delay time		㊵	t_{DKRL}	5	95	5	85	5	75	ns
CLKOUT↓ → $\overline{RD}$↑ delay time		㊶	t_{DKRH}	5	90	5	80	5	70	ns
$\overline{RD}$↑ → address delay time		㊷	t_{DRHA}	t_{CYK}−70		t_{CYK}−60		t_{CYK}−50		ns
$\overline{RD}$ low-level width		㊸	t_{RR}	2t_{CYK}−70		2t_{CYK}−60		2t_{CYK}−50		ns
$\overline{BUFEN}$↑ → BUFR/W delay time (read cycle)		㊹	t_{DBECT}	t_{KKL}−30		t_{KKL}−30		t_{KKL}−20		ns
CLKOUT↓ → data output delay time		㊺	t_{DKD}	5	80	5	70	5	60	ns
CLKOUT↓ → data float delay time		㊻	t_{FKD}	5	80	5	70	5	60	ns
$\overline{WR}$ low-level width		㊼	t_{WW}	2t_{CYK}−50		2t_{CYK}−50		2t_{CYK}−40		ns
$\overline{WR}$↑ → $\overline{BUFEN}$↑ or BUFR/W↓ (write cycle)		㊽	t_{DWCT}	t_{KKL}−30		t_{KKL}−30		t_{KKL}−20		ns
CLKOUT↑ → BS↓ delay time		㊾	t_{DKBL}	5	80	5	70	5	60	ns
CLKOUT↓ → BS↑ delay time		㊿	t_{DKBH}	5	80	5	70	5	60	ns
HLDRQ setup time (vs. CLKOUT↓)		(51)	t_{SHQK}	25		25		20		ns
CLKOUT↓ → HLDAK delay time		(52)	t_{DKHA}	5	90	5	80	5	70	ns
CLKOUT↑ → $\overline{DMAAK}$ delay time		(53)	t_{DKHDA}	5	80	5	70	5	60	ns
CLKOUT↓ → $\overline{DMAAK}$ delay time (cascade mode)		(54)	t_{DKLDA}	5	110	5	100	5	90	ns
$\overline{WR}$ low-level width (DMA cycle)	DMA expansion write	(55)	t_{WW1}	2t_{CYK}−50		2t_{CYK}−50		2t_{CYK}−40		ns
	DMA normal write	(56)	t_{WW2}	t_{CYK}−50		t_{CYK}−50		t_{CYK}−40		ns
$\overline{RD}$↓ $\overline{WR}$↓ delay time (vs. $\overline{DMAAK}$↓)		(57)	t_{DDARW}	t_{KKH}−40		t_{KKH}−40		t_{KKH}−30		ns
$\overline{DMAAK}$↑ delay time (vs. $\overline{RD}$↑)		(58)	t_{DRHDAH}	t_{KKL}−40		t_{KKL}−40		t_{KKL}−30		ns
$\overline{RD}$↑ delay time (vs. $\overline{WR}$↑)		(59)	t_{DWHRH}	5		5		5		ns
$\overline{TC}$ output delay time (vs. CLKOUT↑)		(60)	t_{DKTCL}	5	80	5	70	5	60	ns
$\overline{TC}$ OFF delay time (vs. CLKOUT↑)		(61)	t_{DKTCF}	5	80	5	70	5	60	ns
$\overline{TC}$ low-level width		(62)	t_{TCTCL}	t_{CYK}−25		t_{CYK}−25		t_{CYK}−15		ns
$\overline{TC}$ pull-up delay time (vs. CLKOUT↑)		(63)	t_{DKTCH}		Note 3		Note 4		Note 4	ns
$\overline{END}$ setup time (vs. CLKOUT↑)		(64)	t_{SEDK}	45		40		35		ns
$\overline{END}$ low-level width		(65)	t_{EDEDL}	140		120		100		ns
DMARQ setup time (vs. CLKOUT↑)		(66)	t_{SDQK}	45		40		35		ns
INTPn low-level width		(67)	t_{IPIPL}	100		100		100		ns
RxD setup time (vs. SCU internal clock↓)		(68)	t_{SRX}	1000		1000		1000		ns
RxD hold time (vs. SCU internal clock↓)		(69)	t_{HRX}	1000		1000		1000		ns
CLKOUT↓ → $\overline{SRDY}$ delay time		(70)	t_{DKSR}		150		150		150	ns

Note 1. $\overline{MWR}$ and $\overline{IOWR}$ signals in DMA cycle

2. $\overline{MWR}$ and $\overline{IOWR}$ signals in $\overline{BUFEN}$, BUFR/W, $\overline{INTAK}$, $\overline{REFRQ}$ and CPU cycles.

3. t_{KKH}+2t_{CYK} − 20 (Reference value when a 1.1-kΩ pull-up resistor is connected)

4. t_{KKH}+2t_{CYK} − 10 (Reference value when a 1.1-kΩ pull-up resistor is connected)

(1) μPD70208H, 70216H-10/12/16 (T_A = −40 to +85 °C, V_{DD} = 3 V ±10%) (3/3)

Output Pin Load Capacitance: C_L = 100 pF

Parameter	Symbol		μPD70208H-10 μPD70216H-10		μPD70208H-12 μPD70216H-12		μPD70208H-16 μPD70216H-16		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
TOUT1↓→ TxD delay time	⑦①	t_{DTX}		500		500		500	ns
TCTL2 setup time (vs. CLKOUT↓)	⑦②	t_{SGK}	50		50		50		ns
TCTL2 setup time (vs. TCLK↑)	⑦③	t_{SGTK}	50		50		50		ns
TCTL2 hold time (vs. CLKOUT↓)	⑦④	t_{HKG}	100		100		100		ns
TCTL2 hold time (vs. TCLK↑)	⑦⑤	t_{HTKG}	50		50		50		ns
TCTL2 high-level width	⑦⑥	t_{GGH}	50		50		50		ns
TCTL2 low-level width	⑦⑦	t_{GGL}	50		50		50		ns
TOUT output delay time (vs. CLKOUT↓)	⑦⑧	t_{DKTO}		200		200		200	ns
TOUT output delay time (vs. TCLK↓)	⑦⑨	t_{DTKTO}		150		150		150	ns
TOUT output delay time (vs. TCTL2↓)	⑧⓪	t_{DGTO}		120		120		120	ns
TCLK rise time	⑧①	t_{TKR}		25		25		25	ns
TCLK fall time	⑧②	t_{TKF}		25		25		25	ns
TCLK high-level width	⑧③	t_{TKTKH}	60		55		50		ns
TCLK low-level width	⑧④	t_{TKTKL}	60		55		50		ns
TCLK cycle	⑧⑤	t_{CYTK}	200	DC	166	DC	125	DC	ns
Access interval[Note 1]	⑧⑥	t_{AI}	$2t_{CYK}$−70		$2t_{CYK}$−60		$2t_{CYK}$−50		ns
$\overline{\text{REFRQ}}$↑ delay time (vs. $\overline{\text{MRD}}$↑)[Note 2]	⑧⑦	t_{DRQHRH}	t_{KKL}−50		t_{KKL}−40		t_{KKL}−30		ns
$\overline{\text{RESET}}$ pulse width[Note 3]	⑧⑧	t_{WRESL}	$4t_{CYK}$		$4t_{CYK}$		$4t_{CYK}$		ns ★

Notes 1. Specification to guarantee read/write recovery time for I/O device.

2. Specification to guarantee that $\overline{\text{REFRQ}}$↑ is always later than $\overline{\text{MRD}}$↑.
Only guaranteed when the EREF bit of the SCTL register is 0.

3. The oscillation stabilization time must be added when the power-ON reset or STOP mode has been released. Because the oscillation stabilization time varies depending on the characteristics of the oscillator and oscillation circuit used, evaluate the oscillation stabilization time with the oscillator and oscillation circuit actually used.

★ **(2) μPD70208H, 70216H-20 (T_A = −40 to +85 °C, V_{DD} = 3 V ±10%) (1/3)**

Output Pin Load Capacitance: C_L = 100 pF

Parameter	Symbol		μPD70208H-20 μPD70216H-20		Unit
			MIN.	MAX.	
External clock input cycle	①	t_{CYX}	50	DC	ns
External clock input high-level width (V_{KH}=0.8 V_{DD})	②	t_{XXH}	19		ns
External clock input low-level width (V_{KL}=0.2 V_{DD})	③	t_{XXL}	19		ns
External clock input rise time (0.2 V_{DD}→0.8 V_{DD})	④	t_{XR}		5	ns
External clock input fall time (0.8 V_{DD}→0.2 V_{DD})	⑤	t_{XF}		5	ns
Clock output cycle	⑥	t_{CYK}	100	DC	ns
Clock output high-level width (V_{OH}=0.7 V_{DD})	⑦	t_{KKH}	0.5t_{CYK}−7		ns
Clock output low-level width (V_{OL}=0.2 V_{DD})	⑧	t_{KKL}	0.5t_{CYK}−7		ns
Clock output rise time (0.2 V_{DD}→0.7 V_{DD})	⑨	t_{KR}		7	ns
Clock output fall time (0.7 V_{DD}→0.2 V_{DD})	⑩	t_{KF}		7	ns
CLKOUT delay time (vs. external clock)	⑪	t_{DXK}		45	ns
Input rise time (except external clock) (0.2 V_{DD}→0.7 V_{DD})	⑫	t_{IR}		15	ns
Input fall time (except external clock) (0.7 V_{DD}→0.2 V_{DD})	⑬	t_{IF}		10	ns
Output rise time (except CLKOUT) (0.2 V_{DD}→0.7 V_{DD})	⑭	t_{OR}		15	ns
Output fall time (except CLKOUT) (0.7 V_{DD}→0.2 V_{DD})	⑮	t_{OF}		10	ns
$\overline{\text{RESET}}$ setup time (vs. CLKOUT↓)[Note]	⑯	t_{SRESK}	25		ns
$\overline{\text{RESET}}$ hold time (vs. CLKOUT↓)[Note]	⑰	t_{HKRES}	25		ns
RESOUT output delay time (vs. CLKOUT↓)	⑱	t_{DKRES}	5	50	ns
READY inactive setup time (vs. CLKOUT↑)	⑲	t_{SRYLK}	15		ns
READY inactive hold time (vs. CLKOUT↑)	⑳	t_{HKRYL}	20		ns
READY active setup time (vs. CLKOUT↑)	㉑	t_{SRYHK}	15		ns
READY active hold time (vs. CLKOUT↑)	㉒	t_{HKRYH}	20		ns
NMI setup time (vs. CLKOUT↑)	㉓	t_{SNMIK}	15		ns
POLL setup time (vs. CLKOUT↑)	㉔	t_{SPOLK}	20		ns
Data setup time (vs. CLKOUT↓)	㉕	t_{SDK}	15		ns
Data hold time (vs. CLKOUT↓)	㉖	t_{HKD}	5		ns
CLKOUT → address delay time	㉗	t_{DKA}	5	50	ns
CLKOUT → address hold time	㉘	t_{HKA}	10		ns
CLKOUT ↓ → PS delay time	㉙	t_{DKP}	5	50	ns
CLKOUT ↓ → PS float delay time	㉚	t_{FKP}	5	50	ns
Address setup time (vs. ASTB↓)	㉛	t_{SAST}	t_{KKL}−20		ns
CLKOUT ↓ → address float delay time	㉜	t_{FKA}	t_{HKA}	50	ns
CLKOUT ↓ → ASTB ↑ delay time	㉝	t_{DKSTH}		40	ns
CLKOUT ↑ → ASTB ↓ delay time	㉞	t_{DKSTL}		45	ns
ASTB high-level width	㉟	t_{STST}	t_{KKL}−10		ns

Note When reset with the minimum pulse width or when guaranteeing the RESOUT output timing.

(2) μPD70208H, 70216H-20 (T_A = −40 to +85 °C, V_{DD} = 3 V ±10%) (2/3) ★

Output Pin Load Capacitance: C_L = 100 pF

Parameter		Symbol		μPD70208H-20 μPD70216H-20 MIN.	μPD70208H-20 μPD70216H-20 MAX.	Unit
ASTB ↓ → address hold time		㊱	t_{HSTA}	t_{KKH}−20		ns
CLKOUT → control 1[Note 1] delay time		㊲	t_{DKCT1}	5	60	ns
CLKOUT → control 2[Note 2] delay time		㊳	t_{DKCT2}	5	55	ns
Address float → $\overline{RD}$ ↓ delay time		㊴	t_{DAFRL}	0		ns
CLKOUT ↓ → $\overline{RD}$ ↓ delay time		㊵	t_{DKRL}	5	65	ns
CLKOUT ↓ → $\overline{RD}$ ↑ delay time		㊶	t_{DKRH}	5	60	ns
$\overline{RD}$ ↑ → address delay time		㊷	t_{DRHA}	t_{CYK}−40		ns
$\overline{RD}$ low-level width		㊸	t_{RR}	2t_{CYK}−40		ns
$\overline{BUFEN}$ ↑ → BUFR/W delay time (read cycle)		㊹	t_{DBECT}	t_{KKL}−20		ns
CLKOUT ↓ → data output delay time		㊺	t_{DKD}	5	55	ns
CLKOUT ↓ → data float delay time		㊻	t_{FKD}	5	55	ns
$\overline{WR}$ low-level width		㊼	t_{WW}	2t_{CYK}−40		ns
$\overline{WR}$ ↑ → $\overline{BUFEN}$ ↑ or BUFR/W ↓ (write cycle)		㊽	t_{DWCT}	t_{KKL}−20		ns
CLKOUT ↑ → BS ↓ delay time		㊾	t_{DKBL}	5	55	ns
CLKOUT ↓ → BS ↑ delay time		㊿	t_{DKBH}	5	55	ns
HLDRQ setup time (vs. CLKOUT ↓)		(51)	t_{SHQK}	15		ns
CLKOUT ↓ → HLDAK delay time		(52)	t_{DKHA}	5	60	ns
CLKOUT ↑ → $\overline{DMAAK}$ delay time		(53)	t_{DKHDA}	5	55	ns
CLKOUT ↓ → $\overline{DMAAK}$ delay time (cascade mode)		(54)	t_{DKLDA}	5	80	ns
$\overline{WR}$ low-level width (DMA cycle)	DMA expansion write	(55)	t_{WW1}	2t_{CYK}−40		ns
	DMA normal write	(56)	t_{WW2}	t_{CYK}−40		ns
$\overline{RD}$ ↓, $\overline{WR}$ ↓ delay time (vs. $\overline{DMAAK}$ ↓)		(57)	t_{DDARW}	t_{KKH}−30		ns
$\overline{DMAAK}$ ↑ delay time (vs. $\overline{RD}$ ↑)		(58)	t_{DRHDAH}	t_{KKL}−30		ns
$\overline{RD}$ ↑ delay time (vs. $\overline{WR}$ ↑)		(59)	t_{DWHRH}	3		ns
$\overline{TC}$ output delay time (vs. CLKOUT ↑)		(60)	t_{DKTCL}		55	ns
$\overline{TC}$ OFF delay time (vs. CLKOUT ↑)		(61)	t_{DKTCF}		55	ns
$\overline{TC}$ low-level width		(62)	t_{TCTCL}	t_{CYK}−15		ns
$\overline{TC}$ pull-up delay time (vs. CLKOUT ↑)		(63)	t_{DKTCH}		Note 3	ns
$\overline{END}$ setup time (vs. CLKOUT ↑)		(64)	t_{SEDK}	30		ns
$\overline{END}$ low-level width		(65)	t_{EDEDL}	80		ns
DMARQ setup time (vs. CLKOUT ↑)		(66)	t_{SDQK}	30		ns
INTPn low-level width		(67)	t_{IPIPL}	80		ns
RxD setup time (vs. SCU internal clock ↓)		(68)	t_{SRX}	500		ns
RxD hold time (vs. SCU internal clock ↓)		(69)	t_{HRX}	500		ns
CLKOUT ↓ → $\overline{SRDY}$ delay time		(70)	t_{DKSR}		100	ns

Notes 1. $\overline{MWR}$ and $\overline{IOWR}$ signals in DMA cycle
2. $\overline{MWR}$ and $\overline{IOWR}$ signals in $\overline{BUFEN}$, BUFR/W, $\overline{INTAK}$, $\overline{REFRQ}$, and CPU cycles
3. t_{KKH} + 2t_{CYK} − 10 (reference value when a 1.1-kΩ pull-up resistor is connected)

★ **(2) μPD70208H, 70216H-20 (T_A = −40 to +85 °C, V_{DD} = 3 V ±10%) (3/3)**

Output Pin Load Capacitance: C_L = 100 pF

Parameter	Symbol		μPD70208H-20 μPD70216H-20		Unit
			MIN.	MAX.	
TOUT1 ↓ → TxD delay time	⑦①	t_{DTX}		200	ns
TCTL2 setup time (vs. CLKOUT ↓)	⑦②	t_{SGK}	40		ns
TCTL2 setup time (vs. TCLK ↑)	⑦③	t_{SGTK}	40		ns
TCTL2 hold time (vs. CLKOUT ↓)	⑦④	t_{HKG}	80		ns
TCTL2 hold time (vs. TCLK ↑)	⑦⑤	t_{HTKG}	40		ns
TCTL2 high-level width	⑦⑥	t_{GGH}	40		ns
TCTL2 low-level width	⑦⑦	t_{GGL}	40		ns
TOUT output delay time (vs. CLKOUT ↓)	⑦⑧	t_{DKTO}		150	ns
TOUT output delay time (vs. TCLK ↓)	⑦⑨	t_{DTKTO}		100	ns
TOUT output delay time (vs. TCTL2 ↓)	⑧⓪	t_{DGTO}		90	ns
TCLK rise time	⑧①	t_{TKR}		25	ns
TCLK fall time	⑧②	t_{TKF}		25	ns
TCLK high-level width	⑧③	t_{TKTKH}	45		ns
TCLK low-level width	⑧④	t_{TKTKL}	45		ns
TCLK cycle	⑧⑤	t_{CYTK}	100	DC	ns
Access interval[Note 1]	⑧⑥	t_{AI}	$2t_{CYK}$−40		ns
$\overline{REFRQ}$ ↑ delay time (vs. $\overline{MRD}$ ↑)[Note 2]	⑧⑦	t_{DRQHRH}	t_{KKL}−30		ns
$\overline{RESET}$ pulse width[Note 3]	⑧⑧	t_{WRESL}	$4t_{CYK}$		ns

Notes 1. This rating is to guarantee the read/write recovery time for the I/O device.

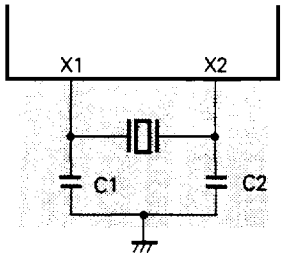
2. This rating is to guarantee that $\overline{REFRQ}$ ↑ is always behind $\overline{MRD}$ ↑, and is guaranteed only when the EREF bit of the STCL register is 0.

3. The oscillation stabilization time must be added when the power-ON reset or STOP mode has been released. Because the oscillation stabilization time varies depending on the characteristics of the oscillator and oscillation circuit used, evaluate the oscillation stabilization time with the oscillator and oscillation circuit actually used.

RECOMMENDED OSCILLATION CIRCUIT ★

The clock input circuits (1) and (2) shown below are recommended.

(1) Ceramic resonator connection (T_A = −40 to +85 °C, V_{DD} = 3 V ±10%[Note])

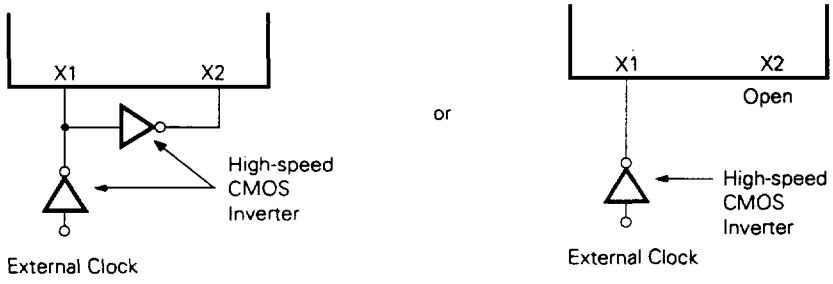


Manufacturer	Frequency (fxx) [MHz]	Product Name	Recommended Constant	
			C1 [pF]	C2 [pF]
Murata Mfg. Co., Ltd.	20	CSA20.00MXZ040[Note]	10	10
	16	CSA16.00MXZ040	15	15
		CSA16.00MXW0C3	–	–
	12.5	CSA12.5MTZ	30	30
		CSA12.5MTW	–	–
	10	CSA10.0MTZ	30	30
		CST10.0MXW	–	–
TDK Corporation	20	FCR20.0M2G	10	10
	16	FCR16.0M2G	15	15
	10	FCR10.0MC	–	–

Note Use the CAS20.00MXZ040 within the range of V_{DD} = 2.9 to 3.3 V.

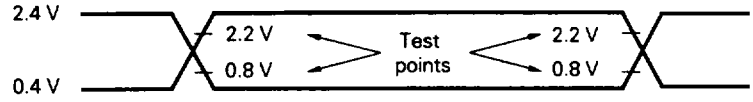
Cautions
1. **The oscillation circuit should be as close as possible to the X1 and X2 pins.**
2. **No other signal lines should pass through the shaded area.**
3. **V40HL, V50HL and resonator matching requires careful evaluation.**

(2) External clock input

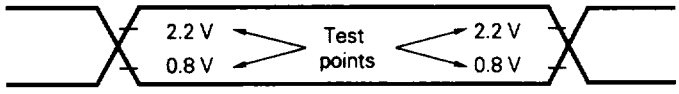


Caution The high-speed CMOS inverter should be as close as possible to the X1 and X2 pins.

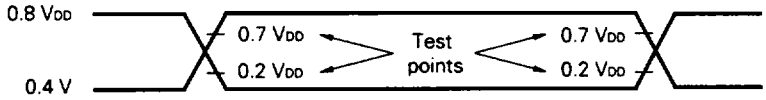
AC Test Input Waveform (Except X1 and X2) (at 5 V operation)



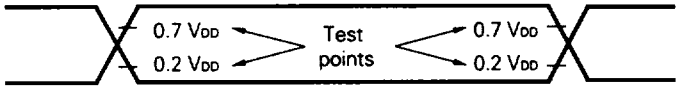
AC Test Output Test Points (at 5 V operation)



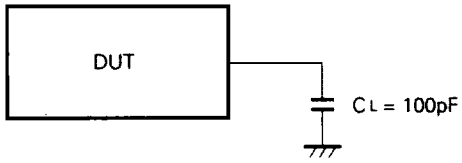
★ **AC Test Input Waveform (Except X1 and X2) (at 3 V operation)**



★ **AC Test Output Waveform (at 3 V operation)**

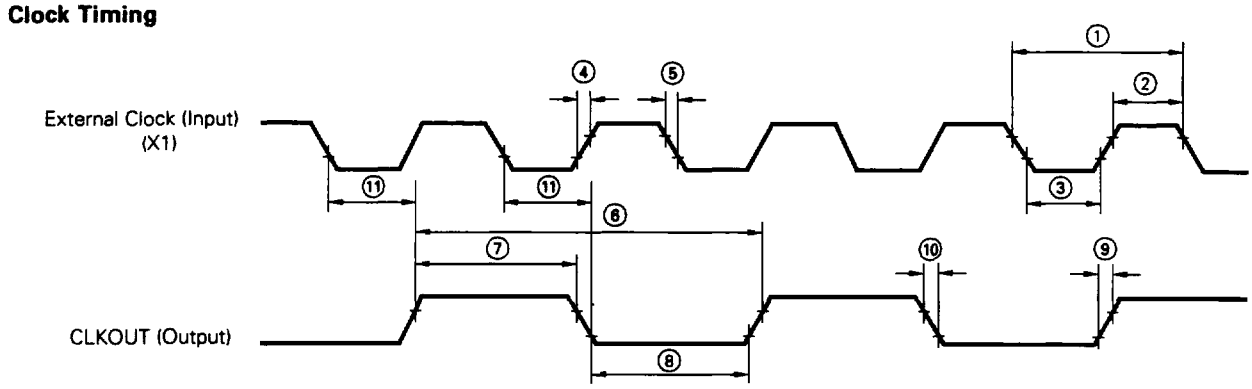


Load Conditions

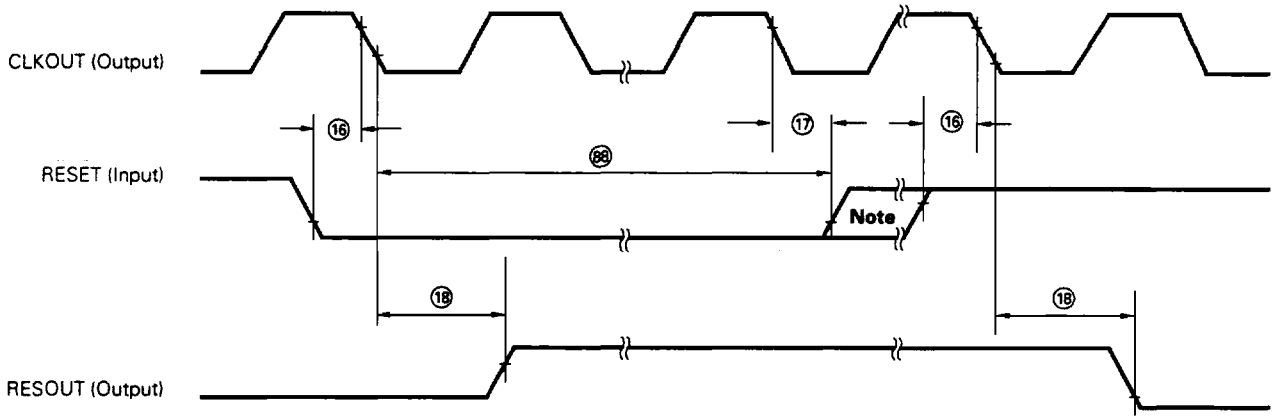


Caution If the load capacitance exceeds 100 pF due to the configuration of the circuit, the load capacitance of this device should be reduced to 100 pF or less by insertion of a buffer, etc.

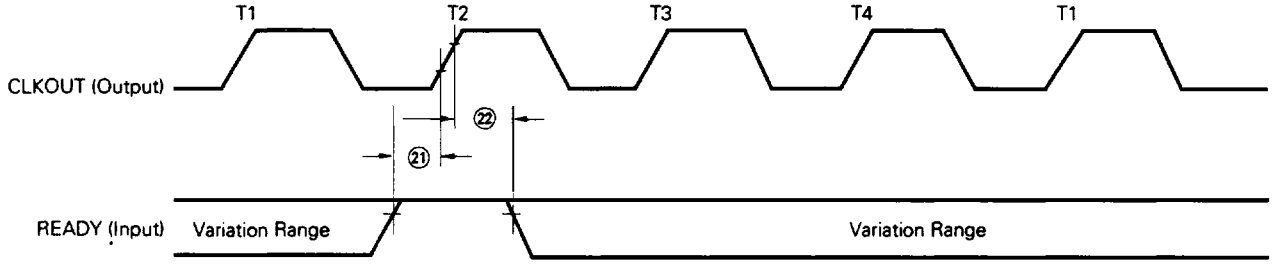
Clock Timing



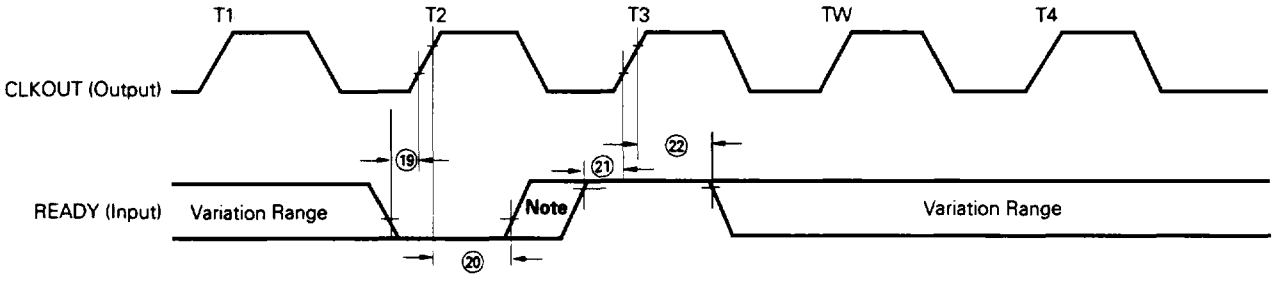
Reset Timing



Ready Timing (1)

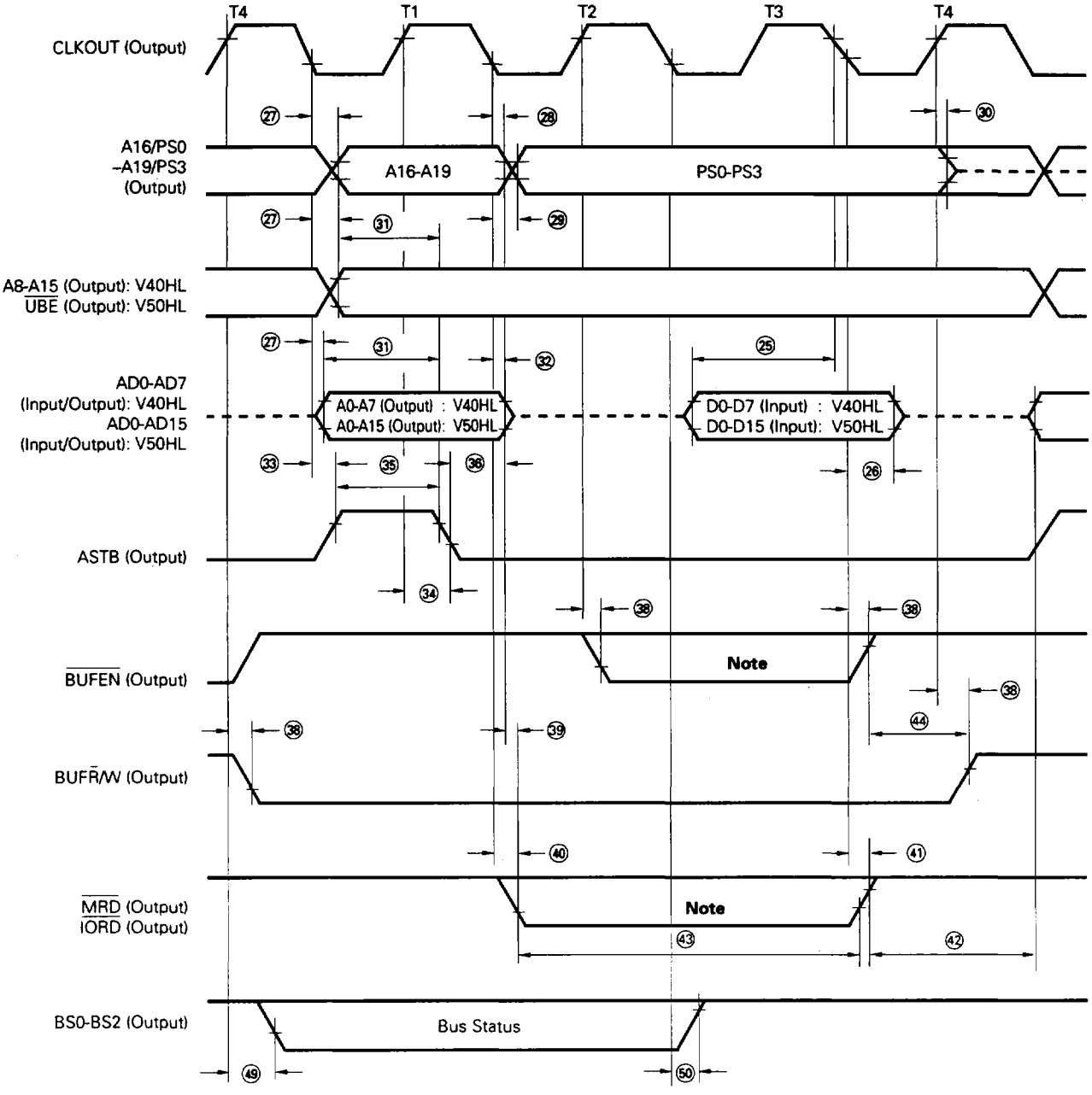


Ready Timing (2)



Note Variation range

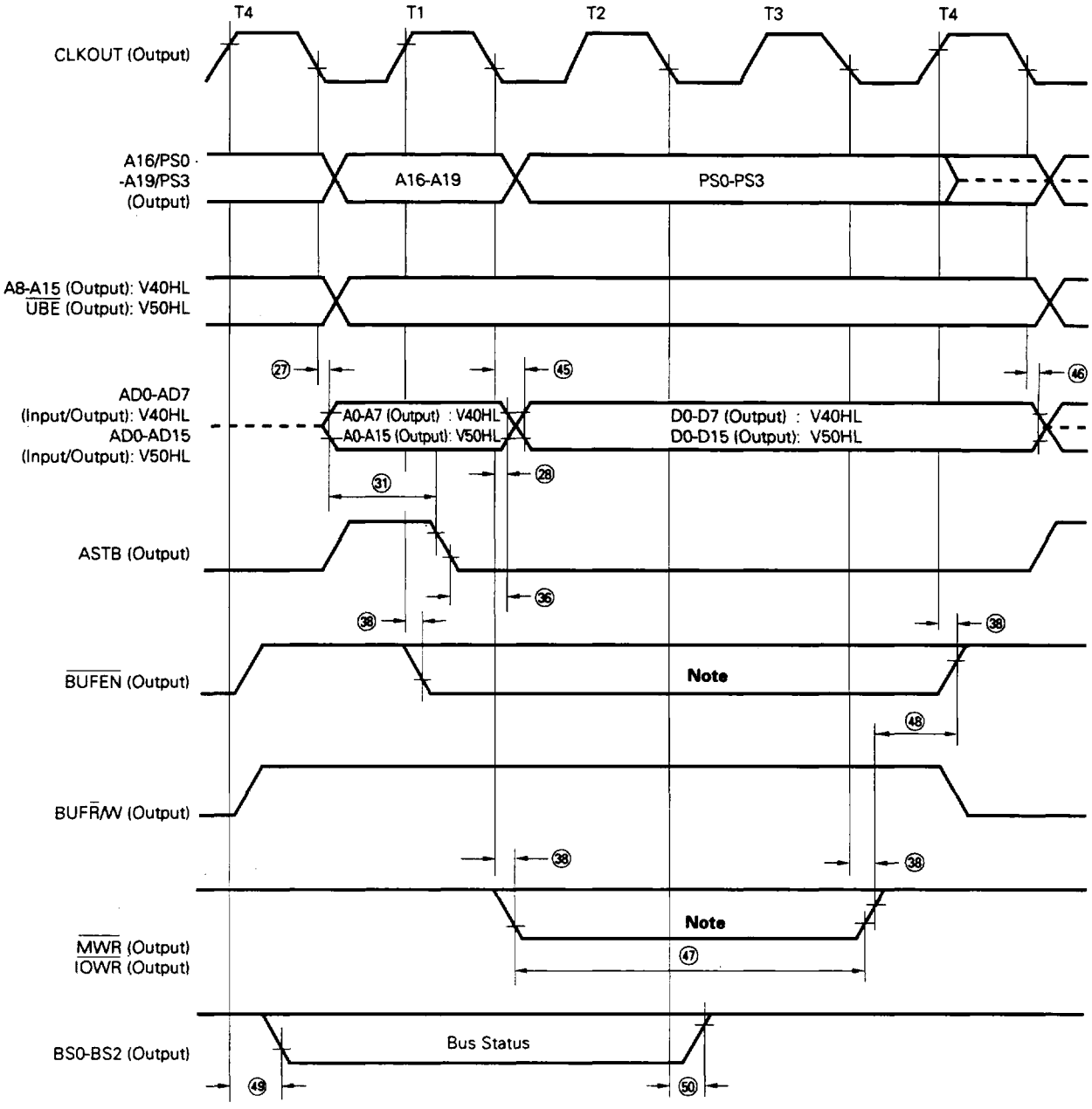
Read Timing



Note High-level signal is output in case of internal access.

Remark A dashed line indicates high impedance.

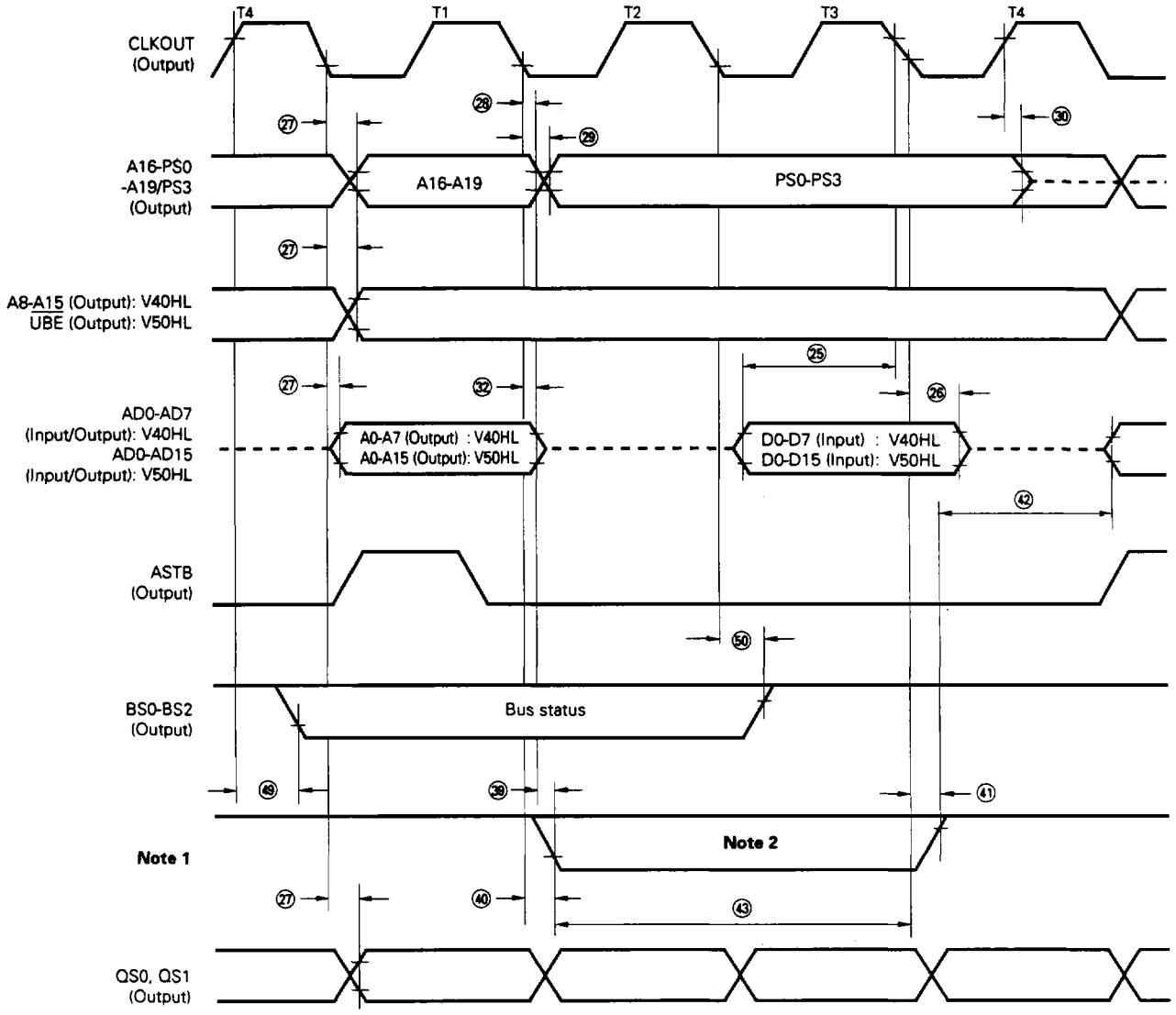
Write Timing



Note High-level signal is output in case of internal access.

Remark A dashed line indicates high impedance.

Status Timing

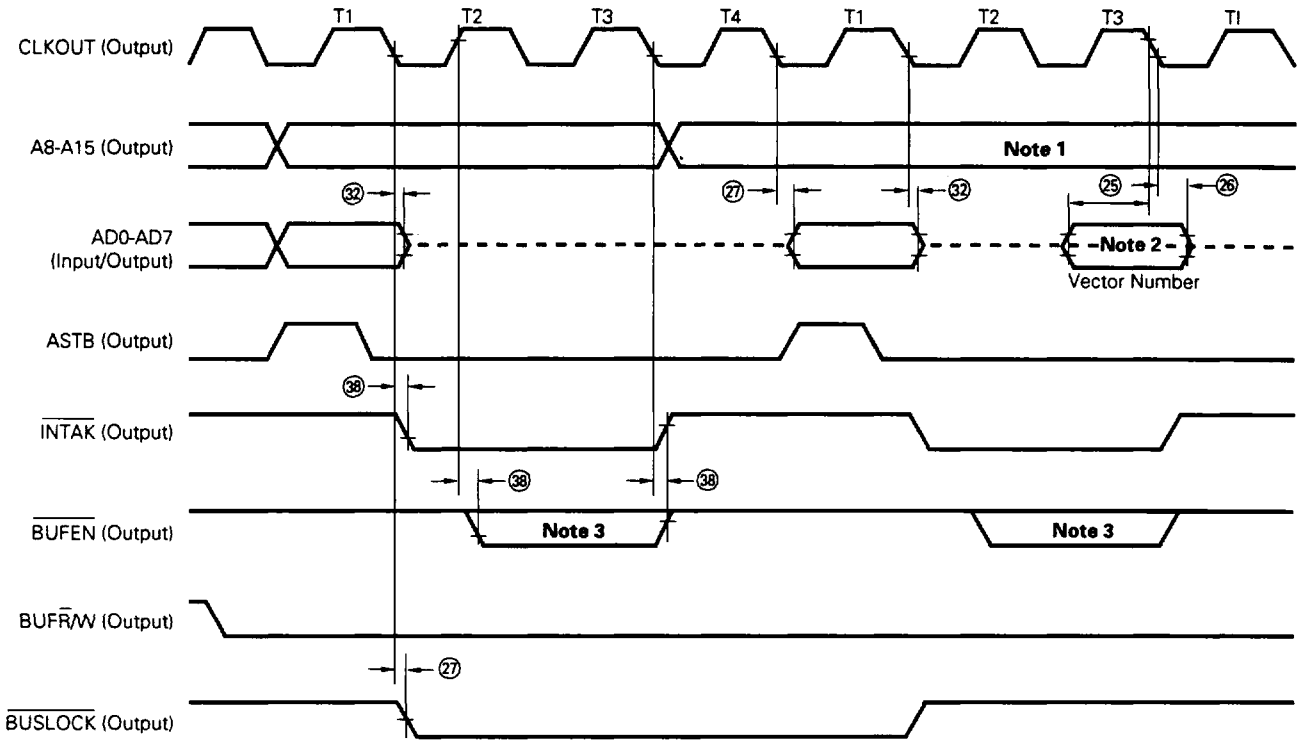


Notes 1. $\overline{MRD}$, $\overline{IORD}$, $\overline{MWR}$, $\overline{IOWR}$ (all output)

2. High-level signal is output in case of internal access.

Remark A dashed line indicates high impedance.

Interrupt Acknowledge Timing (V40HL)

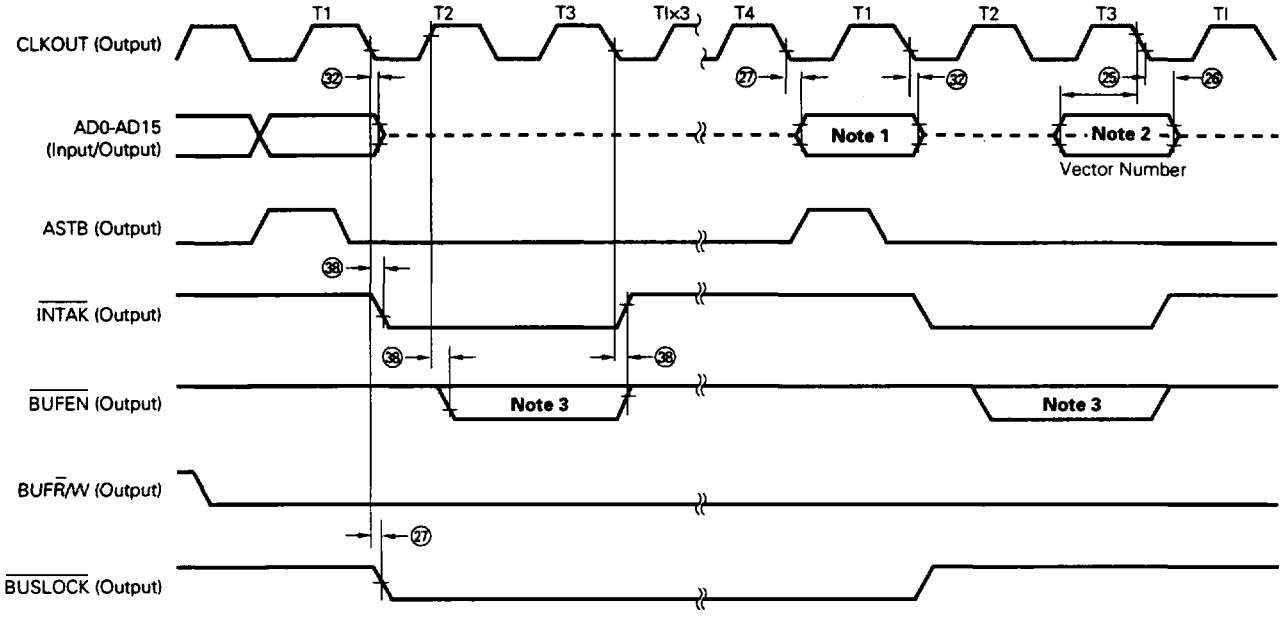


Notes 1. Slave address in case of interrupt from external μPD71059.
Invalid data in case of interrupt from internal ICU.

2. Data read as vector address in case of interrupt from external μPD71059.
High impedance in case of interrupt from internal ICU.
3. Low-level output in case of interrupt from external μPD71059.
High-level output in case of interrupt from internal ICU.

Remark A dashed line indicates high impedance.

Interrupt Acknowledge Timing (V50HL)



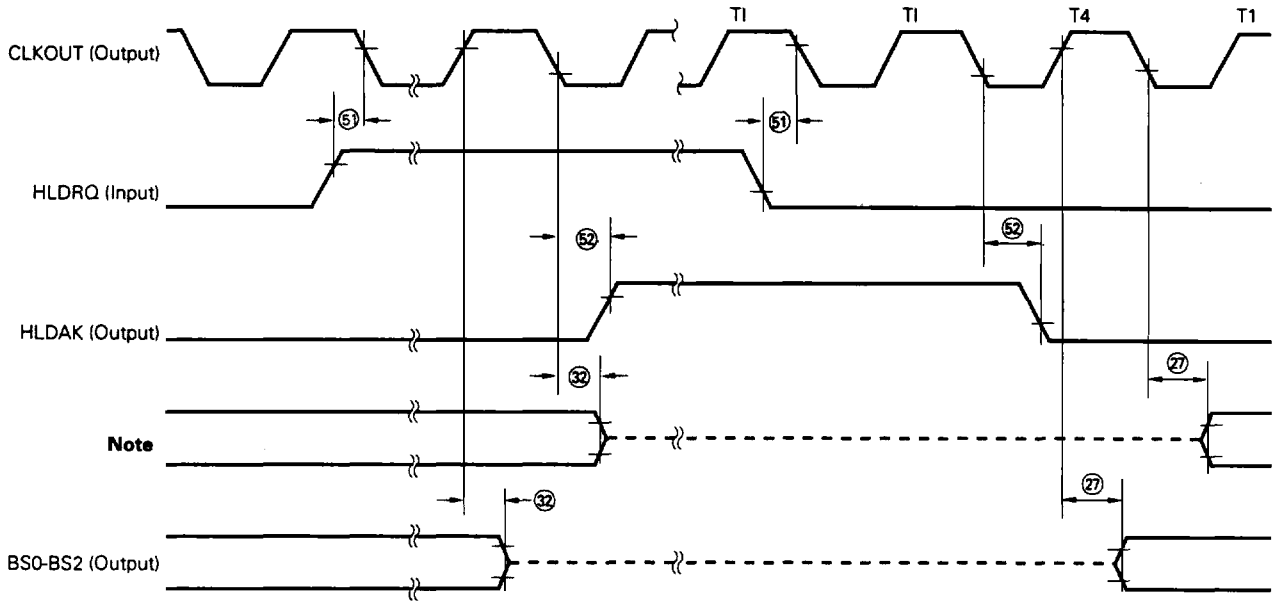
Notes 1. Slave address in case of interrupt from external μPD71059.
Invalid data in case of interrupt from internal ICU.

2. Data read as vector address in case of interrupt from external μPD71059.
High impedance in case of interrupt from internal ICU.

3. Low-level output in case of interrupt from external μPD71059.
High-level output in case of interrupt from internal ICU.

Remark A dashed line indicates high impedance.

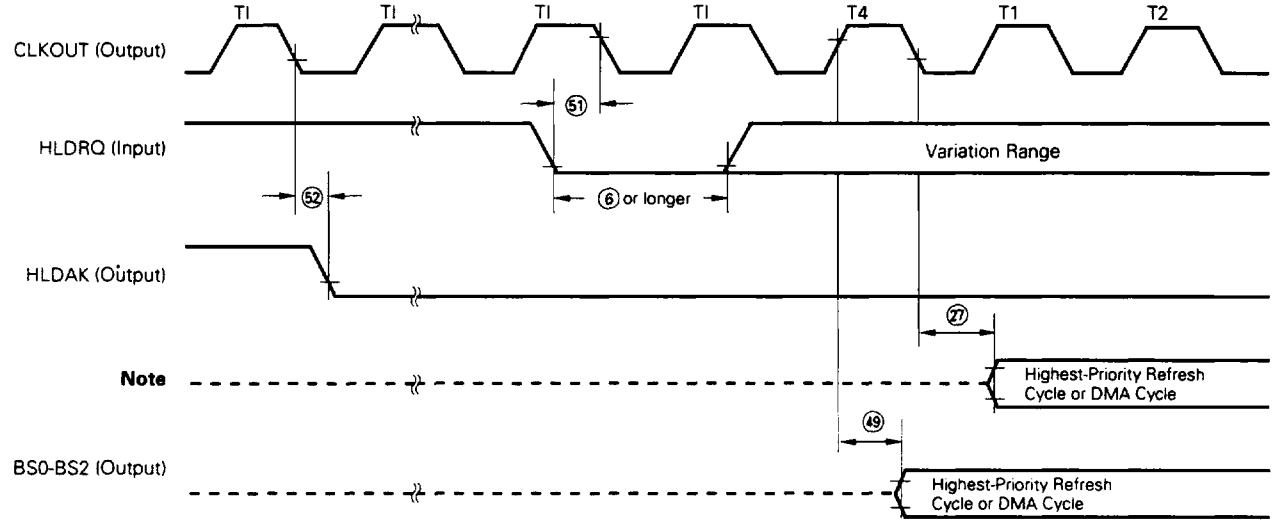
HLDRQ/HLDAK Timing (1)



Note A16/PS0 to A19/PS3, $\overline{UBE}$, $\overline{BUFEN}$, BUFR/W, $\overline{MRD}$, $\overline{IORD}$, $\overline{MWR}$, $\overline{IOWR}$ (all output): V40HL, V50HL
A8-A15 (output): V40HL AD0-AD7 (input/output): V40HL AD0-AD15 (input/output) V50HL

Remark A dashed line indicates high impedance.

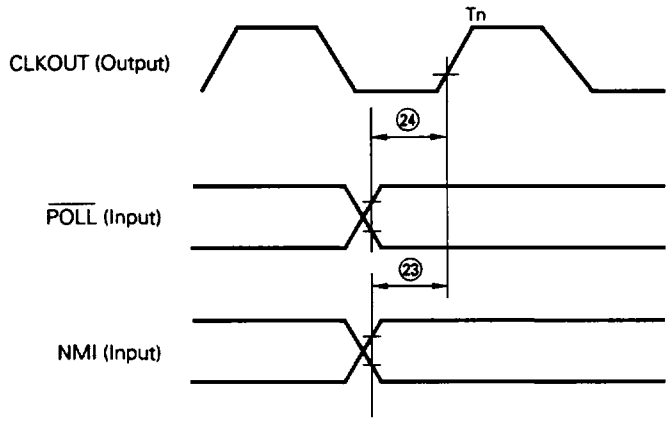
HLDRQ/HLDAK Timing (2)



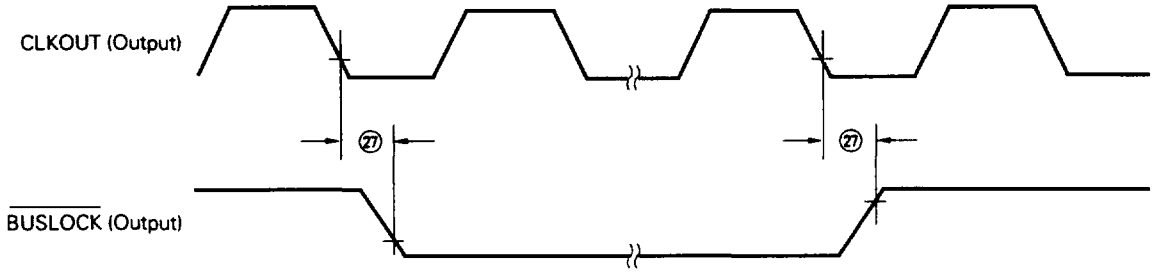
Note A16/PS0 to A19/PS3, $\overline{UBE}$, $\overline{BUFEN}$, BUFR/W, $\overline{MRD}$, $\overline{IORD}$, $\overline{MWR}$, $\overline{IOWR}$ (all output): V40HL, V50HL
A8-A15 (output): V40HL AD0-AD7 (input/output): V40HL AD0-AD15 (input/output) V50HL

Remark A dashed line indicates high impedance.

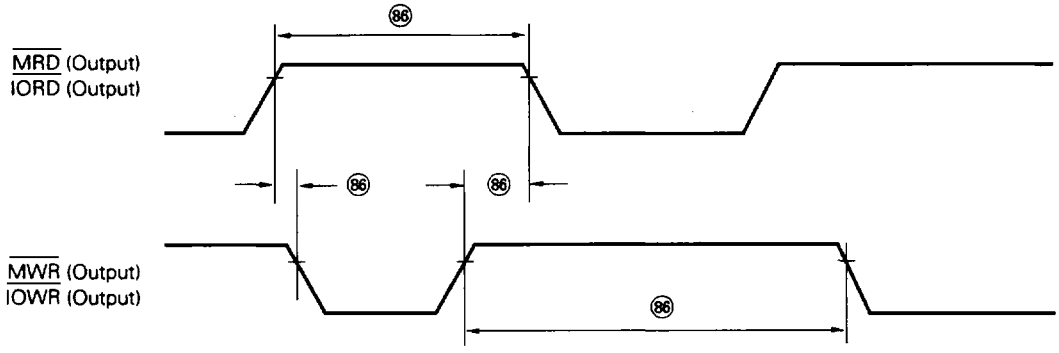
$\overline{\text{POLL}}$, NMI Input Timing



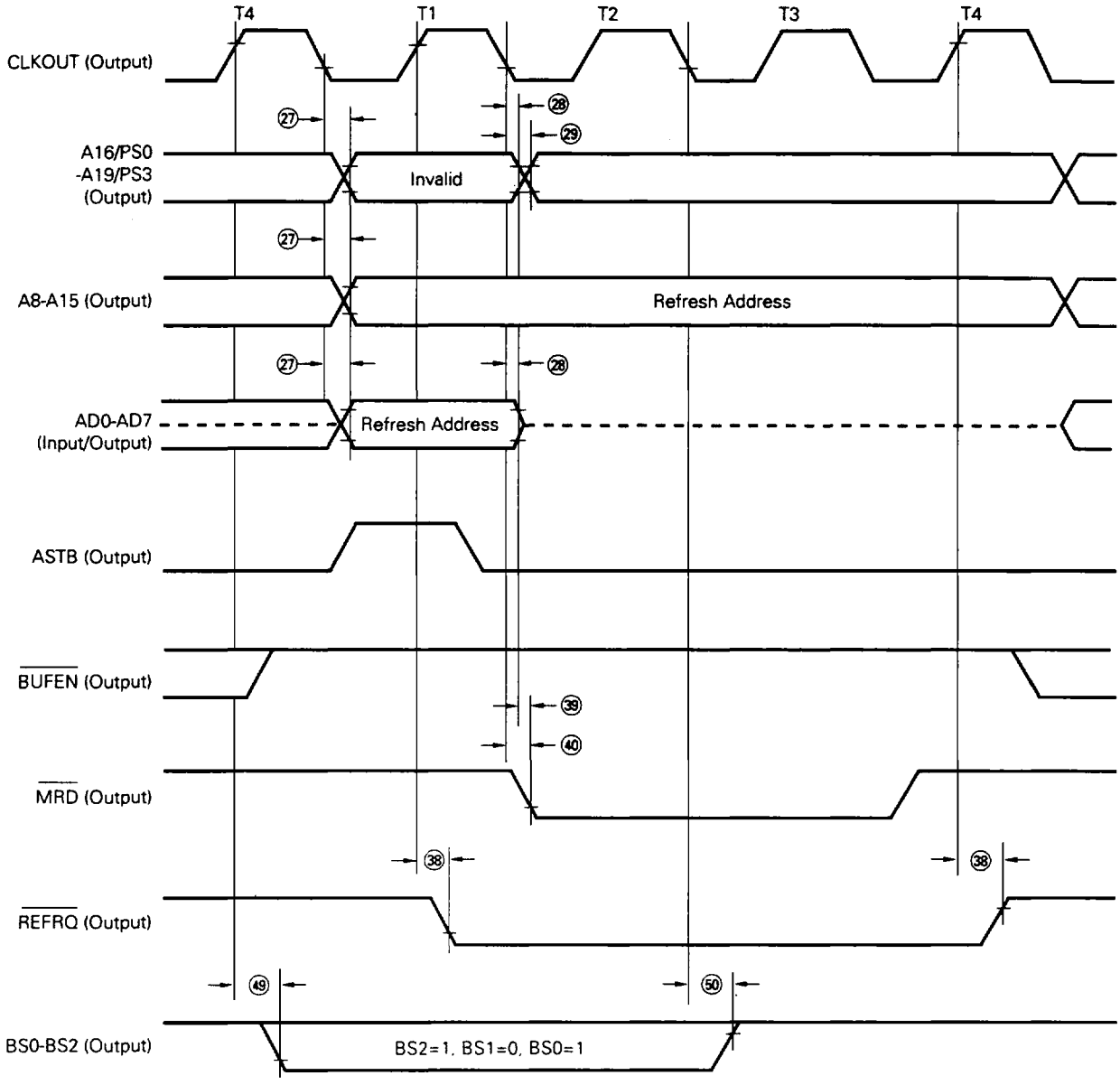
$\overline{\text{BUSLOCK}}$ Output Timing



Access Interval

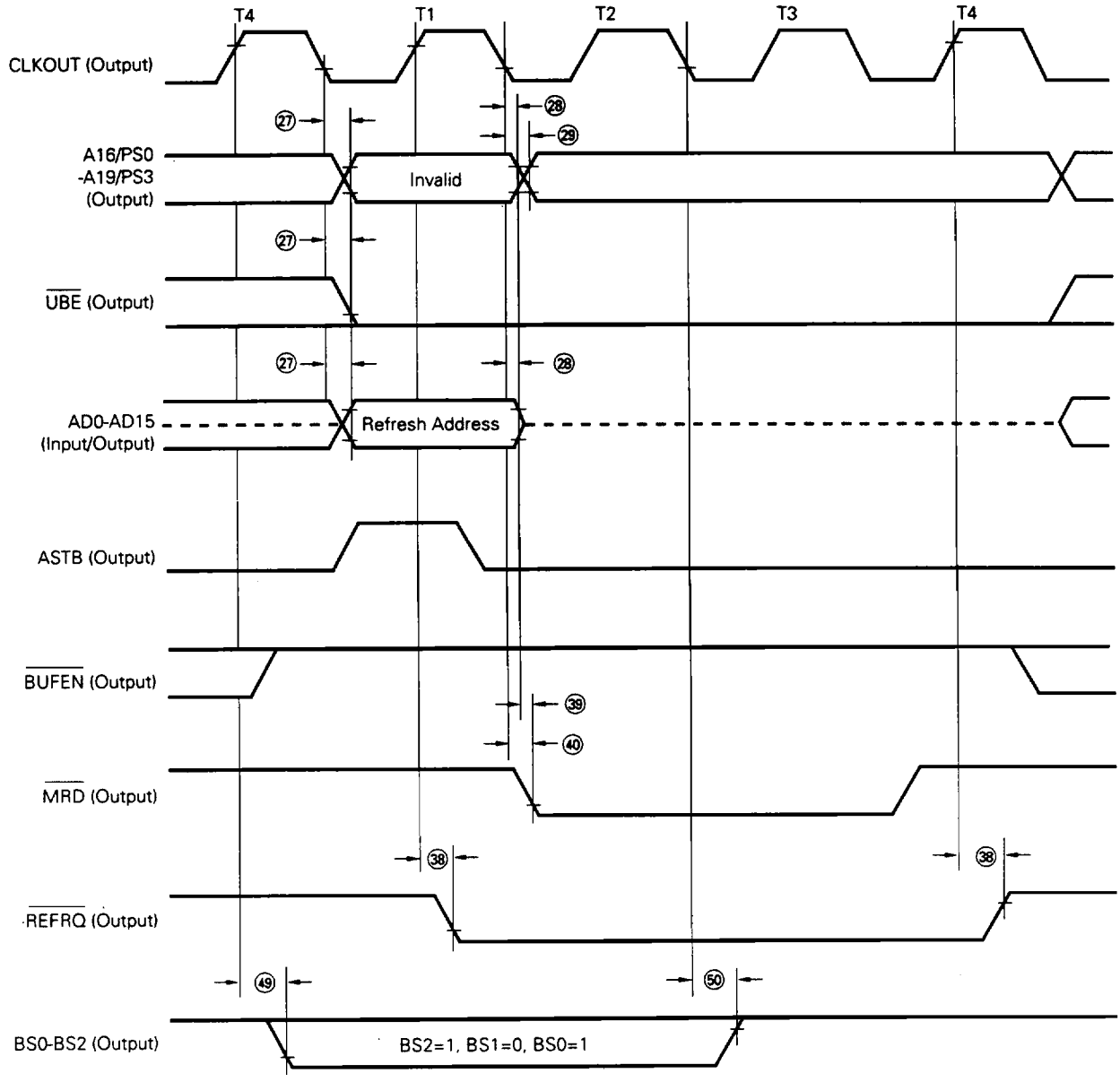


Refresh Timing (V40HL)



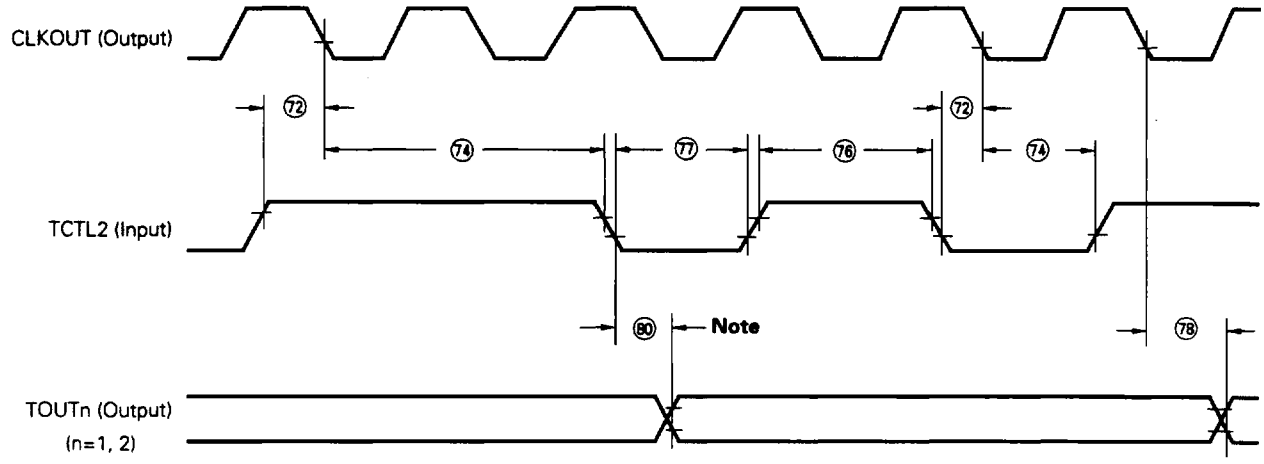
Remark A dashed line indicates high impedance.

Refresh Timing (V50HL)



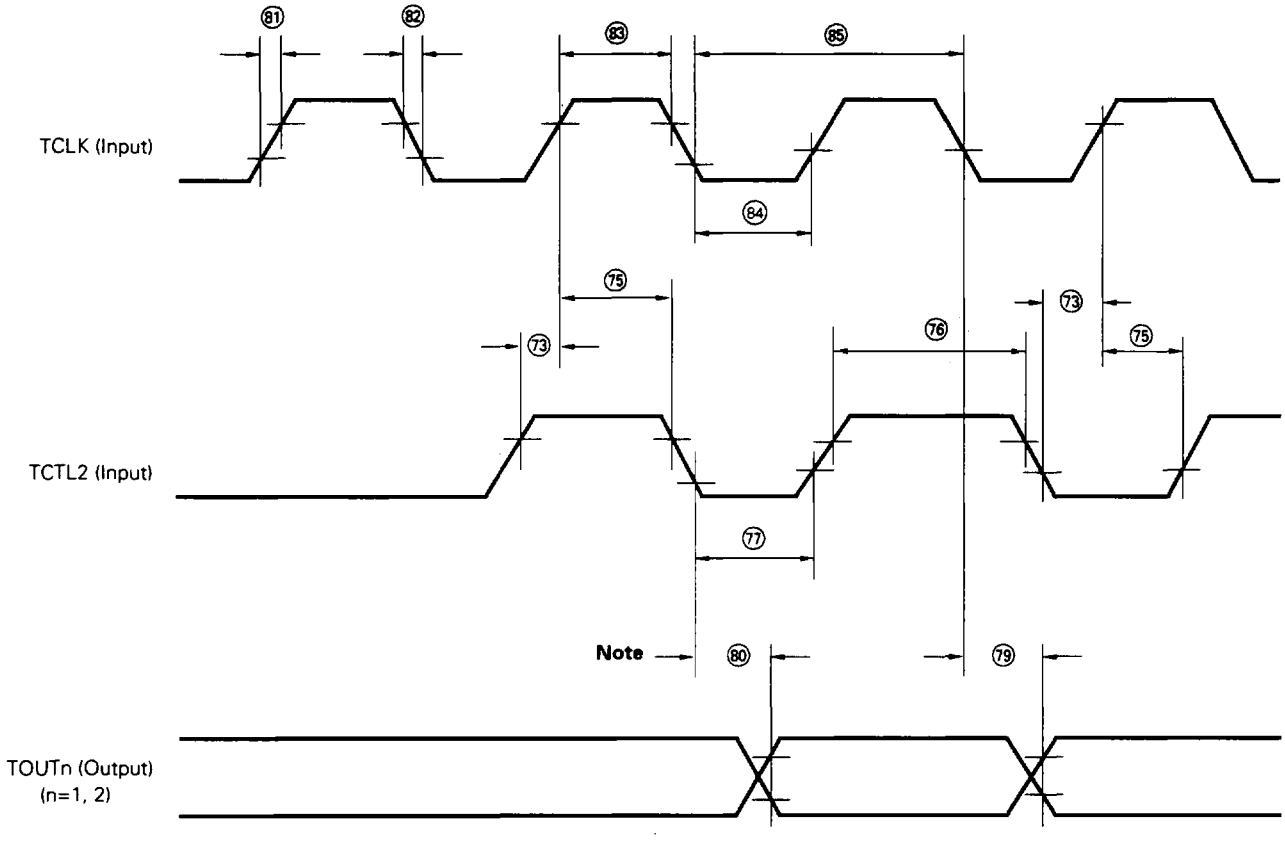
Remark A dashed line indicates high impedance.

TCU Timing (1)



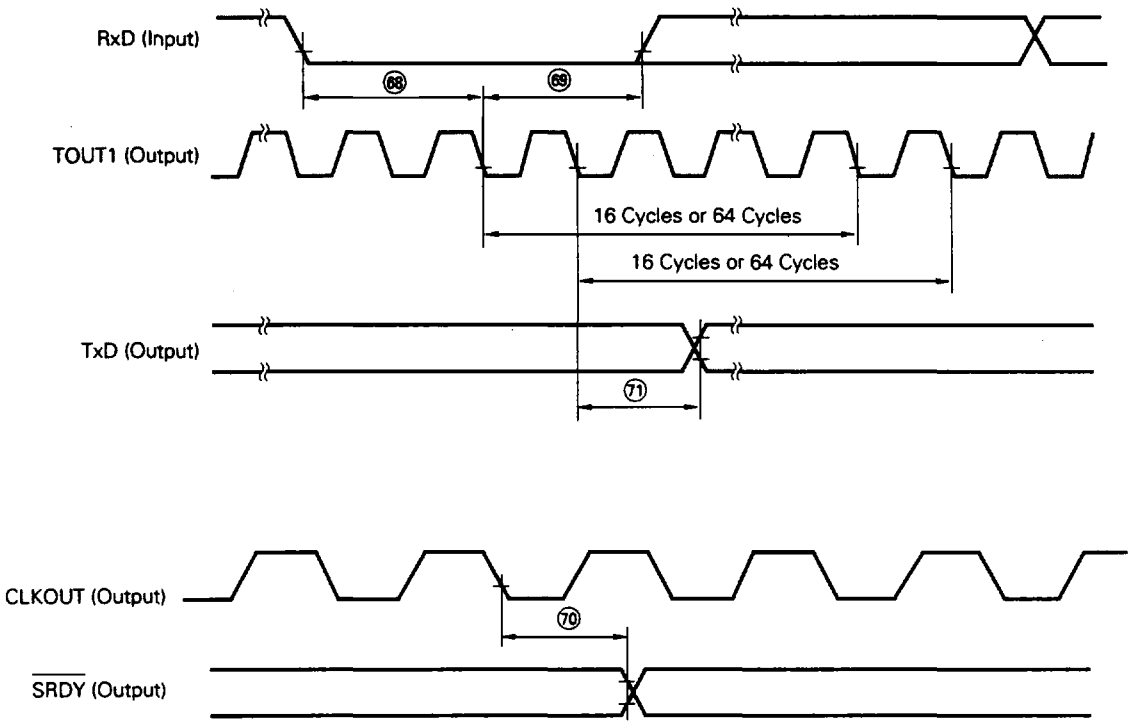
Note Applies to TOUT2 output.

TCU Timing (2)

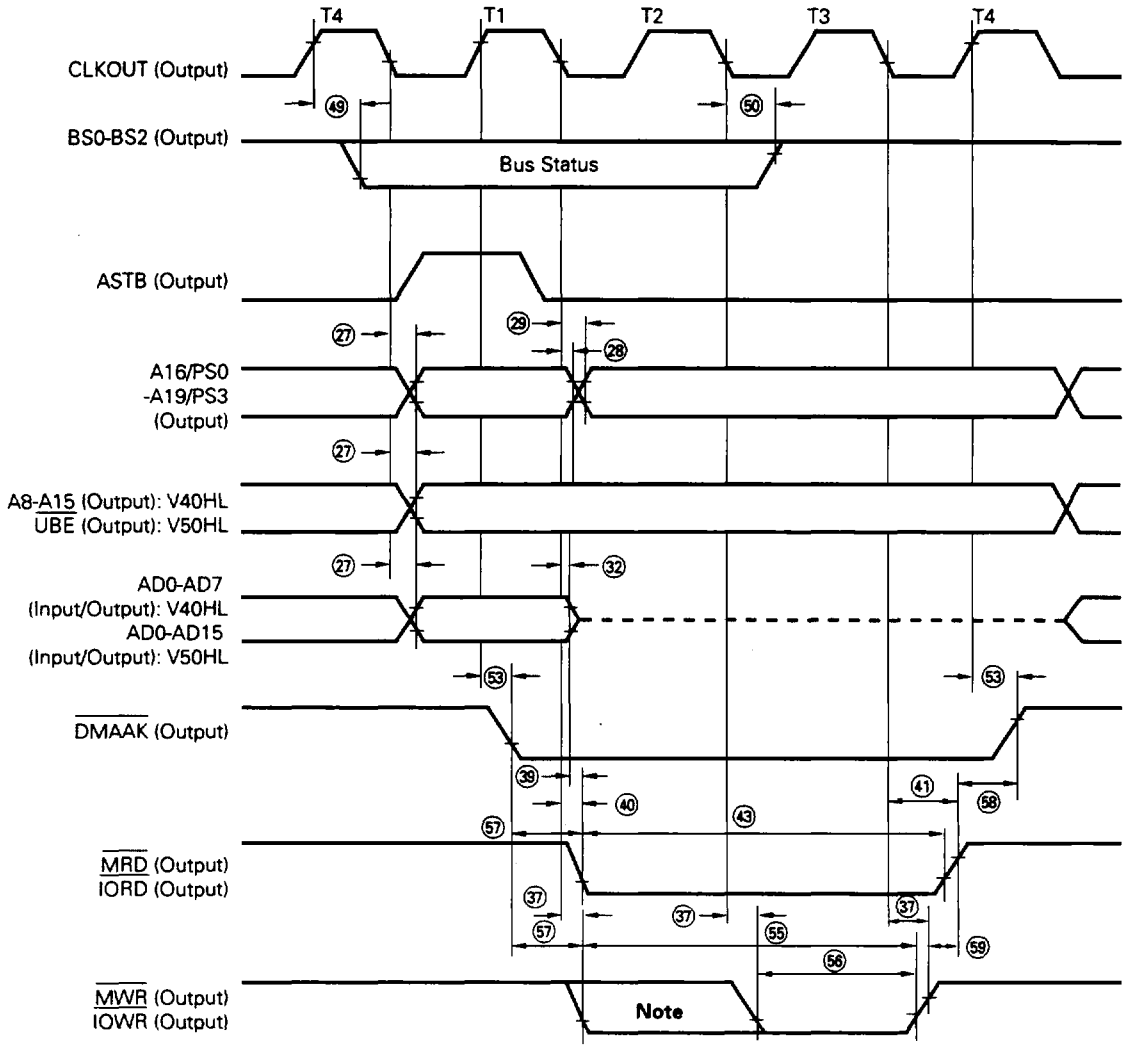


Note Applies to TOUT2 output.

SCU Timing


RxD (Input)
68
69
TOUT1 (Output)
16 Cycles or 64 Cycles
16 Cycles or 64 Cycles
TxD (Output)
71
CLKOUT (Output)
70
SRDY (Output)

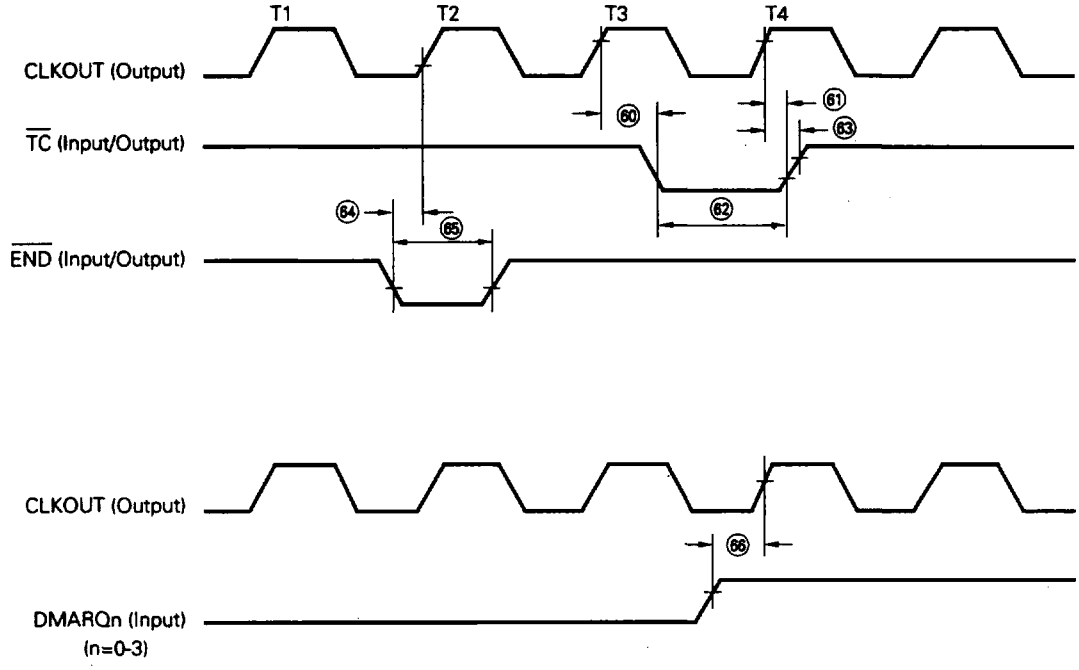
DMAU Timing (1)



Note Low-level signal is output in extended wrote mode.

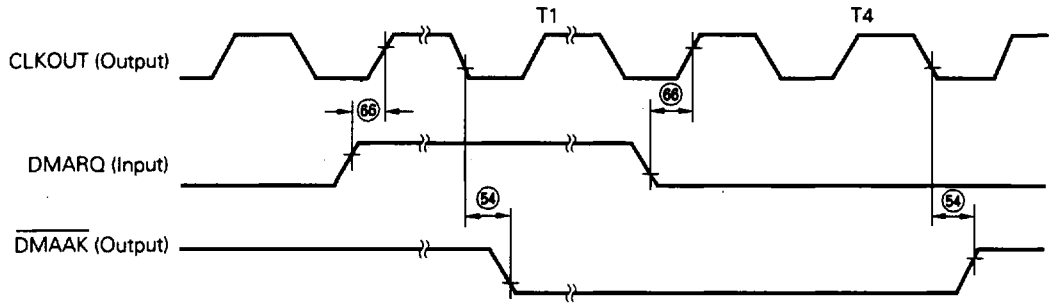
Remark A dashed line indicates high impedance.

DMAU Timing (2)

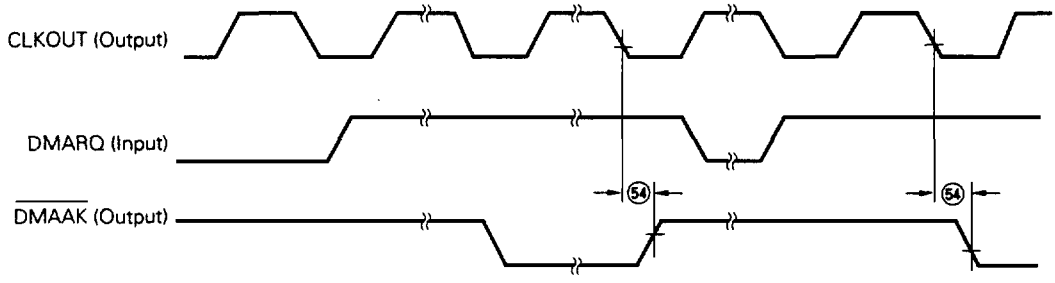


DMAU Timing (3) (Cascade Mode)

In Normal Operation:



When Refresh Cycle is Inserted:



ICU Timing