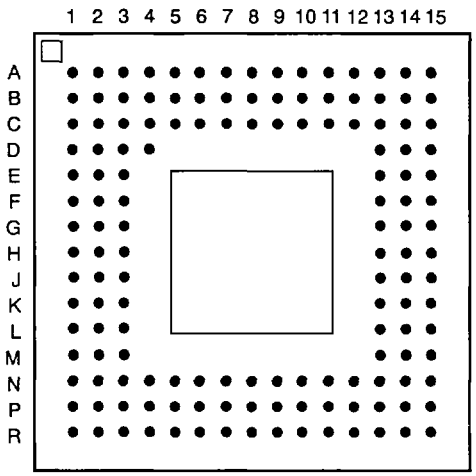
SEPTEMBER 1989

- **Military Temperature Range:**
  −55°C to 125°C
- **Operates as a SMJ34020 Floating Point *Graphics Coprocessor* or as a Standalone Floating Point Processor**
- **Direct Connection to SMJ34020 Coprocessor Interface**
  —Direct SMJ34020 Instruction Extension
  —Multiple SMJ34082 Capability
- **On-Chip Sequencer to Execute Internal or User-Programmed Instructions**
- **Internal Programs for Vector, Matrix, and Graphics Operations**
- **Fast Multiply/Accumulate Cycle Time**
  —40-MHz Version (SMJ34082-40) . . . 50 ns
  —32-MHz Version (SMJ34082-32) . . . 60 ns
- **Twenty-Two 64-Bit Data Registers On-Chip**
- **External Memory Addressing Capability**
  —External Program Storage (Up to 64K Words)
  —External Data Storage (Up to 64K Words)
- **Full ANSI/IEEE STD 754-1985 Compatibility**
  —Addition —Subtraction
  —Multiplication —Division
  —Square Root —Comparison

145-PIN GC PACKAGE
(TOP VIEW)



- **Selectable Data Formats**
  —32-Bit Integer
  —32-Bit Single-Precision Floating Point
  —64-Bit Double-Precision Floating Point

PRODUCT PREVIEW

description

The SMJ34082 is a high-speed floating point processor implemented in TI's advanced one-micron CMOS technology. On a single chip the SMJ34082 combines a 16-bit sequencer and a three-operand FPU (source A, source B, destination) with twenty-two 64-bit data registers. The data registers are organized into two banks of 10 registers each, and two registers are used for internal feedback. In addition, an instruction register to control FPU execution, a status register to retain the most recent FPU status outputs, eight control registers and a two-deep stack are provided.

The SMJ34082 is fully compatible with ANSI/IEEE Std 754-1985 for binary floating point addition, subtraction, multiplication, division, square root, and comparison. Floating point operands can be in either single- or double-precision IEEE format.

In addition to its floating point operations, the SMJ34082 performs 32-bit integer arithmetic, logical comparisons, and shifts. Integer operations may be performed on 32-bit two's-complement or unsigned operands. Integer results are 32 bits long (even for 32 × 32 integer multiplication). Absolute value conversions, floating point to integer conversions, and integer to floating point conversions are available.

The ALU and the multiplier are closely coupled and can be operated in parallel to perform sums of products and products of sums. During multiply/accumulate operations both the ALU and the multiplier are active, and the registers in the FPU core can be used to feed back products and accumulate sums without tying up locations in register banks A and B.

When used with SMJ34020, the SMJ34082 operates in coprocessor mode, and the SMJ34020 can control multiple SMJ34082 coprocessors. When used standalone or with processors other than the SMJ34020, the SMJ34082 operates in host-independent mode. The SMJ34082 is fully programmable by the user and can interface to other processors or floating point subsystems through its two 32-bit bidirectional buses.

data flow

The SMJ34082 has two bidirectional 32-bit buses, LAD31-LAD0 and MSD31-MSD0. Each bus can be used to pass instructions and data operands to the FPU core and to output results. A separate 16-bit bus, MSA15-MSA0, provides memory addressing capability on the MSD bus.

When the SMJ34082 is used as coprocessor for the SMJ34020 Graphics System Processor (GSP), data transfer for the SMJ34082 can be handled through the 32-bit bidirectional data bus (LAD31-LAD0) and may be passed to any internal registers or to external memory on the memory expansion interface (MSD31-MSD0). When the SMJ34082 is used as a standalone FPU, it can use both the LAD bus (LAD31-LAD0) and the MSD bus (MSD31-MSD0) to interface with external data memory or system buses.

Several modes for moving operands and instructions are available. Block transfers up to 255 words long between the LAD and MSD buses can be programmed in either direction. In host-independent mode the SMJ34082 can be operated with the LAD bus as its single data bus and the MSD bus as the instruction source, or with data storage on either port and the program memory on the MSD bus.

A data space/$\overline{\text{code}}$ $\overline{\text{source}}$ (DS/$\overline{\text{CS}}$) output can be used to control access either to data memory or program memory on the MSD port. In SMJ34020 coprocessor mode both instructions and data are transferred on the LAD bus, with the option of accessing external user-generated programs on the MSD port.

One 32-bit operand can be input to the data registers on each clock cycle. A 64-bit double-precision floating point operand is input in two cycles. Transfers to or from the data registers can usually be handled as block moves, loading one or more sets of operands with a single MOVE instruction to minimize I/O overhead.

To permit direct input to or output from the LAD bus, other options for controlling the LAD bus have been implemented. When two 32-bit operands are being selected for input to the FPU core, one operand may be selected from LAD. On output from the FPU, a result may simultaneously be written to a register and to the LAD bus.

During initialization in host-independent mode, a bootstrap loader can bring sixty-five 32-bit words from the LAD bus and write them out to external program memory on the MSD bus, after which the device begins executing from the first memory location. This option facilitates the initial loading of program memory on the MSD port upon power-up.