PACE1750A
SINGLE CHIP, 40MHz, CMOS 16-BIT PROCESSOR

FEATURES

- Implements the MIL-STD-1750A Instruction Set Architecture
- Single Chip PACE Technology™ CMOS 16-Bit Processor with 32 and 48-Bit Floating Point Arithmetic
- DAIS Instruction Mix Execution Performance including Floating Point Arithmetic
  - 1.3 MIPS at 20 MHz
  - 1.9 MIPS at 30 MHz
  - 2.6 MIPS at 40 MHz
- Integer DAIS Mix Performance
  - 3.9 MIPS at 40 MHz
- Conventional Integer Processing Mix Performance
  - 5.0 MIPS at 40 MHz
- Instruction Execution at 40 MHz over the Military Temperature Range
  - 0.10 µsec Integer Add/Sub
  - 0.57 µsec Integer Multiply
  - 0.70 µsec Floating Point Add/Sub
  - 1.07 µsec Floating Point Multiply
- 20, 30 and 40 MHz operation over the Military Temperature Range
- Extensive Error and Fault MAnagement and Interrupt Capability
- 24 User Accessible Registers
- Single 5V ± 10% Power Supply
- Power Dissipation over Military Temperature Range
  - <0.30 watts at 20 MHz
  - <0.35 watts at 30 MHz
  - <0.40 watts at 40 MHz
- TTL Signal Level compatible Inputs and outputs
- Multiprocessor and Co-processor capability
- Built-In Function (BIF) for User Defined Instructions
- Two programmable Timers
- Available In:
  - — 64-Pin DIP or Gull Wing (50 Mil Pin Centers)
  - — 68-Pin Pin Grid Array (PGA)
  - — 68-Lead Quad Pack (Leaded Chip Carrier)

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GENERAL DESCRIPTION

The PACE1750A is a general purpose, single chip, 16-bit CMOS microprocessor designed for high performance floating point and integer arithmetic, with extensive real time environment support. It offers a variety of data types, including bits, bytes, 16-bit and 32-bit integers, and 32-bit and 48-bit floating point numbers. It provides 13 addressing modes, including direct, indirect, indexed, based, based indexed and immediate long and short, and it can access 2 MWords of segmented memory space (64 KWords segments).

The PACE1750A offers a well-rounded instruction set a with 130 instruction types, including a comprehensive integer, floating point, integer-to-floating point and floating point-to-integer set, a variety of stack manipulation instructions, high level language support instructions such as Compare Between Bounds and Loop control instructions. It also offers some unique instructions such as vectored I/O, supports executive and user modes, and provides an escape mechanism which allows user-defined instructions using a coprocessor.

The chip includes 16 general purpose registers, 8 other user-accessible registers, and an array of real time application support resources, such as 2 programmable timers, a complete interrupt controller supporting 16 levels of prioritized internal and external interrupts, and a faults and exceptions handler controlling internally and externally generated faults.

The microprocessor achieves very high throughput of 2.6 MIPS for a standard real time integer/floating point instruction mix at a 40 MHz clock. It executes integer Add in 0.1 uSec, integer Multiply in 0.575 uSec, Floating Point Add in 0.7 uSec, and Floating Point Multiply in 1.075 uSec, for register operands at a 40 MHz clock speed.

The PACE1750A uses a single multiplexed 16-bit parallel bus. Status signals are provided to determine whether the processor is in the memory or I/O bus cycle, reading and writing, and whether the bus cycle is for data or instructions.

The basic bus cycle is 4 clocks long. The PACE1750A will extend the cycle by insertion of wait states in the address and data phases (in response to RDYA and RDYD signals, respectively) and will hold the machine in Hi-Z if this CPU has not acquired the bus. A typical non-bus cycle is three clocks long. However, variable length cycles are used for such repetitive operations as multiply, divide, scale and normalize, reducing significantly the number of CPU CLOCKS per operation step and resulting in very fast integer and floating point execution times.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage Range	–0.5V to +7.0V
Input Voltage Range	–0.5V to V_{CC} + 0.5V
Storage Temperature Range	–65°C to +150°C
Input Current Range	–30mA to +5mA
Voltage applied to Inputs	–0.5V to V_{CC} + 0.5V
Current applied to Output[3]	150mA
Maximum Power Dissipation[2]	1.5W
Operating worst case power dissipation (outputs open): Device type 01 Device type 02 Device type 03 Device type 04	 0.25W at 15MHz 0.30W at 20MHz 0.35W at 30MHz 0.40W at 40MHz
Lead Temperature Range (soldering 10 seconds)	300°C
Thermal resistance, junction-to-case (θ_{JC}): Cases X and T Cases Y and U Case Z	 8°C/W 5°C/W 6°C/W

Notes

1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2. Must withstand the added power dissipation due to short circuit test e.g., I_{OS}.
3. Duration 1 second or less.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range	4.5V to +5.5V
Case Operating Temperature Range	–55°C to +125°C

DC ELECTRICAL SPECIFICATIONS (Over recommended operating conditions)

Symbol	Parameter		Min	Max	Unit	Conditions[1]	
V_{IH}	Input HIGH Level Voltage		2.0	V_{CC} + 0.5	V		
V_{IL}	Input LOW Level Voltage[2]		–0.5	0.8	V		
V_{CD}	Input Clamp Diode Voltage			–1.2	V	V_{CC} = 4.5V, I_{IN} = –18mA	
V_{OH}	Output HIGH Level Voltage		2.4		V	V_{CC} = 4.5V,	I_{OH} = –8.0mA
			V_{CC} – 0.2		V	V_{CC} = 4.5V,	I_{OH} = –300µA
V_{OL}	Output LOW Level Voltage			0.5	V	V_{CC} = 4.5V,	I_{OL} = 8.0mA
				0.2	V	V_{CC} = 4.5V,	I_{OL} = 300µA
I_{IH1}	Input HIGH Level Current, except $IB_0 – IB_{15}$, $\overline{BUS\ BUSY}$, $\overline{BUS\ LOCK}$			10	µA	V_{IN} = V_{CC}, V_{CC} = 5.5V	
I_{IH2}	Input HIGH Level Current, $IB_0 – IB_{15}$, $\overline{BUS\ BUSY}$, $\overline{BUS\ LOCK}$			50	µA	V_{IN} = V_{CC}, V_{CC} = 5.5V	
I_{IL1}	Input LOW Level Current, except $IB_0 – IB_{15}$, $\overline{BUS\ BUSY}$, $\overline{BUS\ LOCK}$			–10	µA	V_{IN} = GND, V_{CC} = 5.5V	
I_{IL2}	Input LOW Level Current, $IB_0 – IB_{15}$, $\overline{BUS\ BUSY}$, $\overline{BUS\ LOCK}$			–50	µA	V_{IN} = GND, V_{CC} = 5.5V	
I_{OZH}	Output Three-State Current			50	µA	V_{OUT} = 2.4V, V_{CC} = 5.5V	
I_{OZL}	Output Three-State Current			–50	µA	V_{OUT} = 0.5V, V_{CC} = 5.5V	
I_{CCQC}	Quiescent Power Supply Current (CMOS Input Levels)			10	mA	V_{IN} < 0.2V or < V_{CC} – 0.2V, f = 0MHz, Outputs Open, V_{CC} = 5.5V	
I_{CCQT}	Quiescent Power Supply Current (TTL Input Levels)			50	mA	V_{IN} < 3.4V, f = 0MHz, Outputs Open, V_{CC} = 5.5V	
I_{CCD}	Dynamic Power Supply Current	15 MHz		40	mA	V_{CC} = 0V to V_{CC}, tr = tf = 2.5 ns, Outputs Open, V_{CC} = 5.5V	
		20 MHz		50	mA		
		30 MHz		60	mA		
		40 MHz		70	mA		
I_{OS}	Output Short Circuit Current[3]		–25		mA	V_{OUT} = GND, V_{CC} = 5.5V	
C_{IN}	Input Capacitance			10	pF		
C_{OUT}	Output Capacitance			15	pF		
$C_{I/O}$	Bi-directional Capacitance			15	pF		

Notes

1. 4.5V ≤ V_{CC} ≤ 5.5V, –55°C ≤ T_C ≤ +125°C. Unless otherwise specified, testing shall be conducted at worst-case conditions.
2. V_{IL} = –3.0V for pulse widths less than or equal to 20ns.
3. Duration of the short should not exceed one second; only one output may be shorted at a time.

SIGNAL PROPAGATION DELAYS[1, 2]

		15 MHz		20 MHz		30 MHz		40 MHz		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Unit
$t_{C(BR)L}$	$\overline{\text{BUS REQ}}$		45		33		25		22	ns
$t_{C(BR)H}$	$\overline{\text{BUS REQ}}$		45		33		25		22	ns
$t_{BGV(C)}$	$\overline{\text{BUS GNT}}$ setup	5		5		5		5		ns
$t_{C(BG)X}$	$\overline{\text{BUS GNT}}$ hold	5		5		5		5		ns
$t_{C(BB)L}$	$\overline{\text{BUS BUSY}}$ LOW		35		25		24		20	ns
$t_{C(BB)H}$	$\overline{\text{BUS BUSY}}$ HIGH		35		25		20		15	ns
$t_{BBV(C)}$	$\overline{\text{BUS BUSY}}$ setup	5		5		5		5		ns
$t_{C(BB)X}$	$\overline{\text{BUS BUSY}}$ hold	5		5		5		5		ns
$t_{C(BL)L}$	$\overline{\text{BUS LOCK}}$ LOW		50		30		25		21	ns
$t_{C(BL)H}$	$\overline{\text{BUS LOCK}}$ HIGH		50		30		25		17	ns
$t_{BLV(C)}$	$\overline{\text{BUS LOCK}}$ setup	5		5		5		5		ns
$t_{C(BL)X\ (IN)}$	$\overline{\text{BUS LOCK}}$ hold	5		5		5		5		ns
$t_{C(ST)V}$	M/$\overline{\text{IO}}$, R/$\overline{\text{W}}$ Status		45		30		25		20	ns
$t_{C(ST)V}$	AS_0-AS_3, AK_0-AK_3, D/I Status		40		25		20		20	ns
$t_{C(ST)X}$	AS_0-AS_3, AK_0-AK_3, D/I Status ,M/$\overline{\text{IO}}$, R/$\overline{\text{W}}$		0		0		0		0	ns
$t_{C(SA)H}$	STRBA HIGH		25		22		17		16	ns
$t_{C(SA)L}$	STRBA LOW		25		22		17		16	ns
$t_{SAL(IBA)X}$	Address hold from STRBA LOW	5		5		5		5		ns
$t_{RAV(C)}$	RDYA setup	5		5		5		5		ns
$t_{C(RA)X}$	RDYA hold	5		5		5		5		ns
$t_{C(SDW)L}$	$\overline{\text{STRBD}}$ LOW write		25		22		17		14	ns
$t_{C(SD)H}$	$\overline{\text{STRBD}}$ HIGH		25		22		17		14	ns
$t_{C(SDR)L}$	$\overline{\text{STRBD}}$ LOW read		25		22		17		14	ns
$t_{(SDR)HIBDX}$	$\overline{\text{STRBD}}$ HIGH	0		0		0		0		ns
$t_{SDWH(IBD)X}$	$\overline{\text{STRBD}}$ HIGH	45		30		25		17		ns
$t_{SDL(SD)H}$	$\overline{\text{STRBD}}$ write	50		40		36		20		ns
$t_{RDV(C)}$	RDYD setup	5		5		5		5		ns
$t_{C(RD)X}$	RDYD hold	5		5		5		5		ns
$t_{C(IBA)V}$	IB_0-IB_{15}		45		30		25		20	ns
$t_{FC(IBA)V}$	IB_0-IB_{15}	0		0		0		0		ns
$t_{IBDRV(C)}$	IB_0-IB_{15} setup	5		5		5		5		ns
$t_{C(IBD)X}$	IB_0-IB_{15} hold (read)	8		7		6		5		ns
$t_{C(IBD)X}$	Data valid out (write)	0		0		0		0		ns

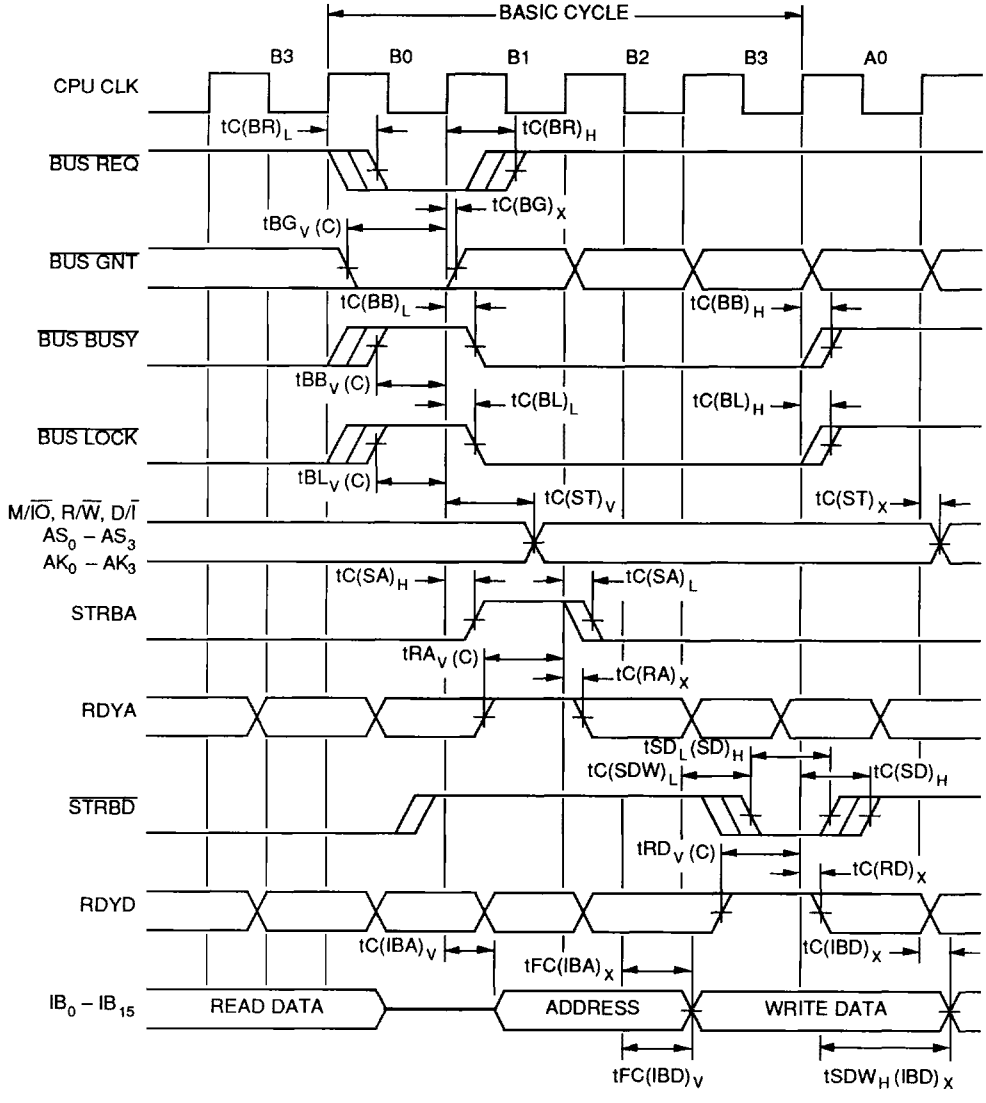
SIGNAL PROPAGATION DELAYS[1, 2] (continued)

Symbol	Parameter	15 MHz		20 MHz		30 MHz		40 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$t_{FC(IBD)V}$	IB_0-IB_{15}		45		30		25		20	ns
$t_{C(SNW)}$	SNEW		45		30		26		22	ns
$t_{FC(TGO)}$	TRIGO RST		45		30		26		22	ns
$t_{RSTL(DMA\ ENL)}$	DMA enable		45		40		35		30	ns
$t_{C(DME)}$	DMA enable		45		40		35		30	ns
$t_{FC(NPU)}$	Normal power up		45		40		35		30	ns
$t_{C(ER)}$	Clock to major error unrecoverable		75		60		50		45	ns
$t_{RSTL(NPU)}$	$\overline{RESET}$		65		50		40		30	ns
$t_{REQV(C)}$	Console request	0		0		0		0		ns
$t_{C(REQ)X}$	Console request	10		10		10		10		ns
$t_{FV(BB)H}$	Level sensitive faults	5		5		5		5		ns
$t_{BBH(F)X}$	Level sensitive faults	5		5		5		5		ns
$t_{IRV(C)}$	IOL_{1-2}INT setup user interrupt (0-5)	0		0		0		0		ns
$t_{C(IR)X}$	Power down interrupt level sensitive hold	10		10		10		10		ns
t_{RSTL} (t_{RSTH})	Reset pulse width	30		25		20		15		ns
$t_{C(XX)Z}$	Clock to three-state		30		22		17		13	ns
$t_{f(F)}$, $t_{1(1)}$	Edge sensitive pulse width	5		5		5		5		ns
t_r, t_f	Clock rise and fall		5		5		5		5	ns

Notes

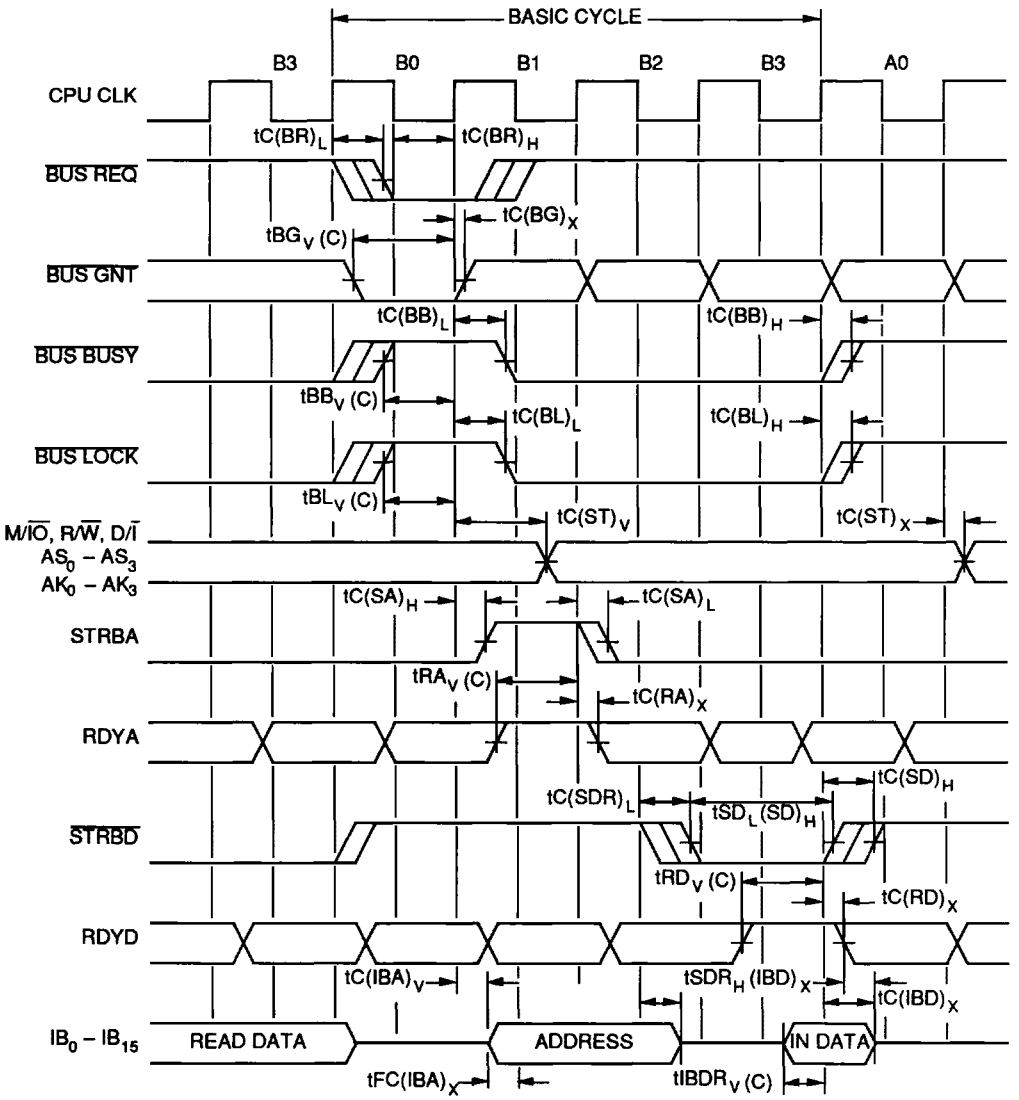
1. $4.5V \le V_{CC} \le 5.5V$, $-55°C \le T_C \le +125°C$. Unless otherwise specified, testing shall be conducted at worst-case conditions.
2. All timing parameters are composed of Three elements. The first "t" stands for timing. The second represents the "from" signal. The third in parentheses indicates "to" signal. When the CPU clock is one of the signal elements, either the rising edge "C" or the falling edge "FC" is referenced. When other elements are used, an additional suffix indicates the final logic level of the signal. "L" - low level, "H" - high level, "V" - valid, "Z" - high impedance, "X" - don't care, "LH" - low to high, "ZH" - high impedance to high, "R" - read cycle, and "W" - write cycle.

MINIMUM WRITE BUS CYCLE TIMING DIAGRAM



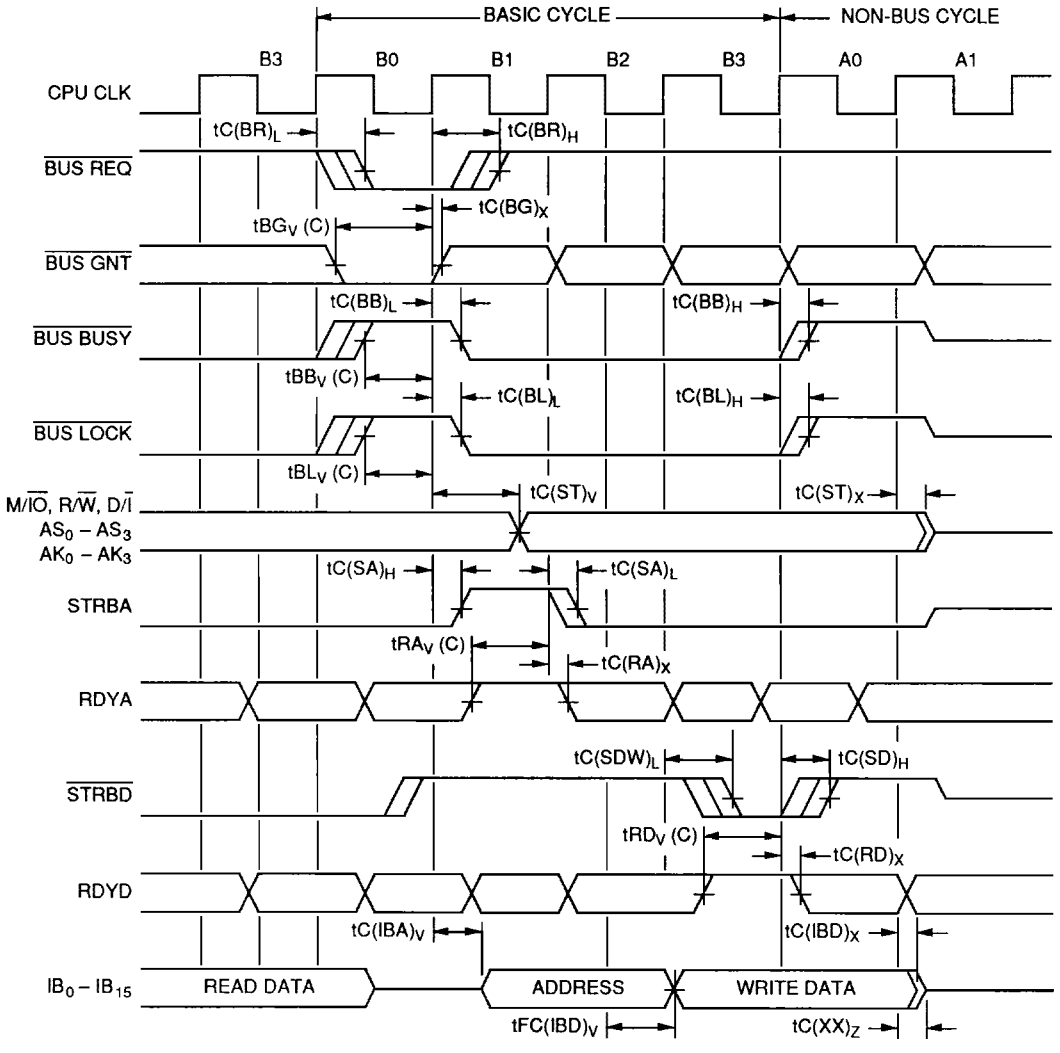
Note:
All time measurements on active signals relate to the 1.5 volt level.

MINIMUM READ BUS CYCLE TIMING DIAGRAM



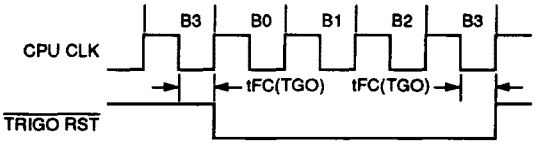
Note:
All time measurements on active signals relate to the 1.5 volt level.

MINIMUM WRITE BUS CYCLE, FOLLOWED BY A NON-BUS CYCLE, TIMING DIAGRAM

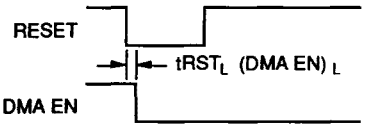


Note:
All time measurements on active signals relate to the 1.5 volt level.

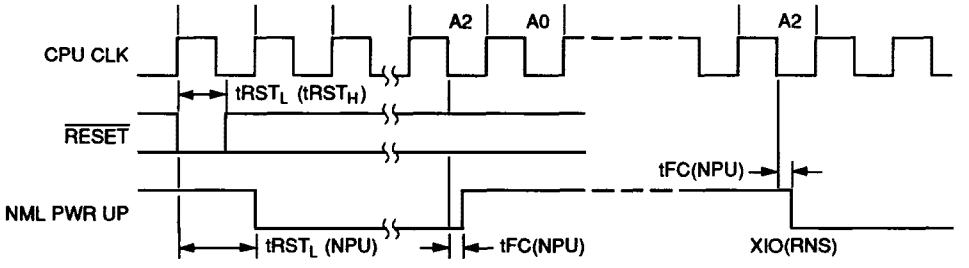
$\overline{\text{TRIGO RST}}$ Discrete Timing



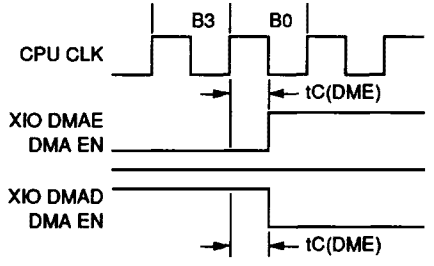
DMA EN Discrete Timing



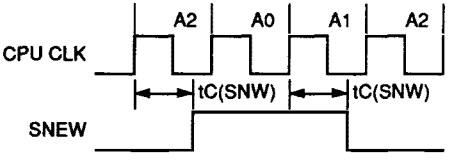
Normal Power Up Discrete Timing



XIO Operations



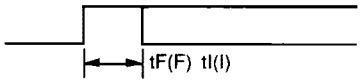
SNEW Discrete Timing



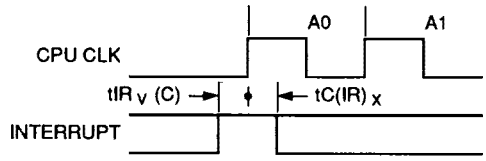
Note:
All time measurements on active signals relate to the 1.5 volt level.

EXTERNAL FAULTS AND INTERRUPTS TIMING DIAGRAM

Edge-sensitive interrupts and faults ($SYSFLT_0$, $SYSFLT_1$) min. pulse width

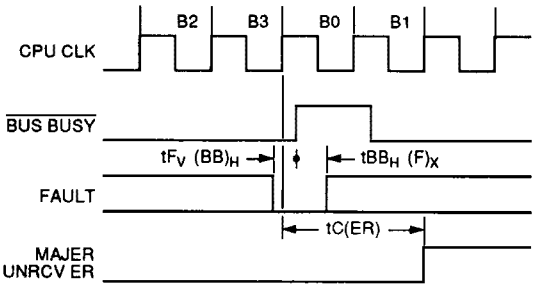


Level-sensitive interrupts

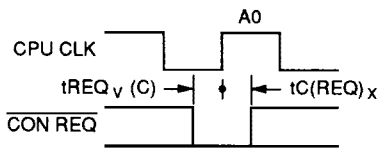


Note: $tC(IR)_X$ max = 35 clocks

Level-sensitive faults

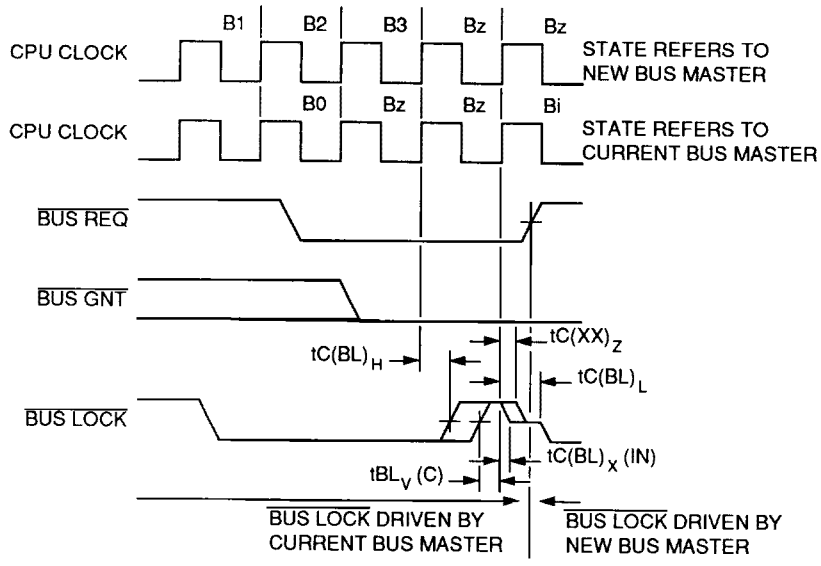


$\overline{\text{CON REQ}}$



Note: All time measurements on active signals relate to the 1.5 volt level.

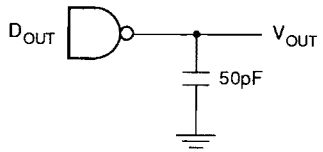
BUS ACQUISITION



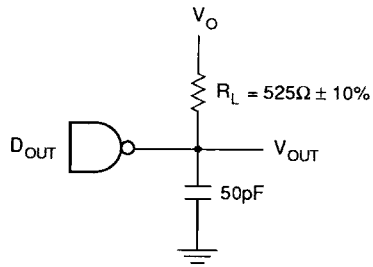
Note: A CPU contending for the BUS, will assert the $\overline{\text{BUS REQ}}$ line, and will acquire it when $\overline{\text{BUS GNT}}$ is assserted and the BUS is not locked ($\overline{\text{BUS LOCK}}$ is high).

SWITCHING TIME TEST CIRCUITS

Standard Output (Non-Three-State)



Three-State



Note: All time measurements on active signals relate to the 1.5 volt level.

Parameter	V0	VMEA
t_{PLZ}	≥ 3V	0.5V
t_{PHZ}	0V	V_{CC} – 0.5V
t_{PXL}	$V_{CC}/2$	1.5V
t_{PXH}	$V_{CC}/2$	1.5V

SIGNAL DESCRIPTIONS

CLOCKS AND EXTERNAL REQUESTS

Mnemonic	Name	Description
CPU CLK	CPU clock	A single phase input clock signal (0–40 MHz, 40 percent to 60 percent duty cycle).
TIMER CLK	Timer clock	A 100 kHz input that, after synchronization with CPU CLK, provides the clock for timer A and timer B. If timers are used, the CPU CLK signal frequency must be > 300 kHz.
$\overline{\text{RESET}}$	Reset	An active low input that initializes the device.
$\overline{\text{CON REQ}}$	Console request	An active low input that initiates console operations after completion of the current instruction.

INTERRUPT INPUTS

Mnemonic	Name	Description
PWRDN INT	Power down interrupt	An interrupt request input that cannot be masked or disabled. This signal is active on the positive going edge or the high level, according to the interrupt mode bit in the configuration register.
USR_0INT - USR_5INT	User interrupt	Interrupt request input signals that are active on the positive going edge or the high level, according to the interrupt mode bit in the configuration register
IOL_1INT IOL_2INT	I/O level interrupts	Active high interrupt request inputs that can be used to expand the number of user interrupts.

FAULTS

Mnemonic	Name	Description
$\overline{\text{MEM PRT ER}}$	Memory protect error	An active low input generated by the MMU or BPU, or both and sampled by the $\overline{\text{BUS BUSY}}$ signal into the fault register (bit 0 CPU bus cycle, bit 1 if non-CPU bus cycle).
$\overline{\text{MEM PAR ER}}$	Memory parity error	An active low input sampled by the $\overline{\text{BUS BUSY}}$ signal into bit 2 of the fault register.
$\overline{\text{EXT ADR ER}}$	External address	An active low input sampled by the $\overline{\text{BUS BUSY}}$ signal into error the fault register (bit 5 or 8), depending on the cycle (memory or I/O).
$SYSFLT_0$ $SYSFLT_1$	System fault $_0$, System fault $_1$,	Asynchronous, positive edge-sensitive inputs that set bit 7 ($SYSFLT_0$) or bits 13 and 15 ($SYSFLT_1$) in thefault register.

ERROR CONTROL

Mnemonic	Name	Description
UNRCV ER	Unrecoverable error	An active high output that indicates the occurrence of an error classified as unrecoverable.
MAJ ER	Major error	An active high output that indicates the occurrence of an error classified as major.

SIGNAL DESCRIPTIONS (Continued)

BUS CONTROL

Mnemonic	Name	Description
D/$\overline{I}$	Data or instruction	An output signal that indicates whether the current bus cycle access is for Data (high) or Instruction (low). It is three-state during bus cycles not assigned to this CPU. This line can be used as an additional memory address bit for systems that require separate data and program memory.
R/$\overline{W}$	Read or write	An output signal that indicates direction of data flow with respect to the current bus master. A high indicates a read or input operation and a low indicates a write or output operation. The signal is three-state during bus cycles not assigned to this CPU.
M/$\overline{IO}$	Memory or I/O	An output signal that indicates whether the current bus cycle is memory (high) or I/O (low). This signal is three-state during bus cycles not assigned to this CPU.
STRBA	Address strobe	An active high output that can be used to externally latch the memory or I/O address at the high-to-low transition of the strobe. The signal is three-state during bus cycles not assigned to this CPU.
RDYA	Address ready	An active high input that can be used to extend the address phase of a bus cycle. When RDYA is not active wait states are inserted by the device to accommodate slower memory or I/O devices.
$\overline{STRBD}$	Data strobe	An active low output that can be used to strobe data in memory and XIO cycles. This signal is three-state during bus cycles not assigned to this CPU.
RDYD	Data ready	An active high input that extends the data phase of a bus cycle. When RDYD is not active, wait states are inserted by the device to accommodate slower memory or I/O devices.

INFORMATION BUS

Mnemonic	Name	Description
IB_0 - IB_{15}	Information bus	A bidirectional time-multiplexed address/data bus that is three-state during bus cycles not assigned to this CPU. IB0 is the most significant bit.

STATUS BUS

Mnemonic	Name	Description
AK_0 - AK_3	Access key	Outputs used to match the access lock in the MMU for memory accesses (a mismatch will cause the MMU to pull the $\overline{MEM\ PRT\ ER}$ signal low), and also indicates processor state (PS). Privileged instructions can be executed with PS = 0 only. These signals are three-state during bus cycles not assigned to this CPU.
AS_0 - AS_3	Address state	Outputs that select the page register group in the MMU. It is three-state during bus cycles not assigned to this CPU. [These outputs together with D/$\overline{I}$ can be used to expand the device direct addressing space to 4 MBytes, in a nonprotected mode (no MMU)]. However, using this addressing mode may produce situations not specified in MIL-STD-1750.

SIGNAL DESCRIPTIONS (Continued)

BUS ARBITRATION

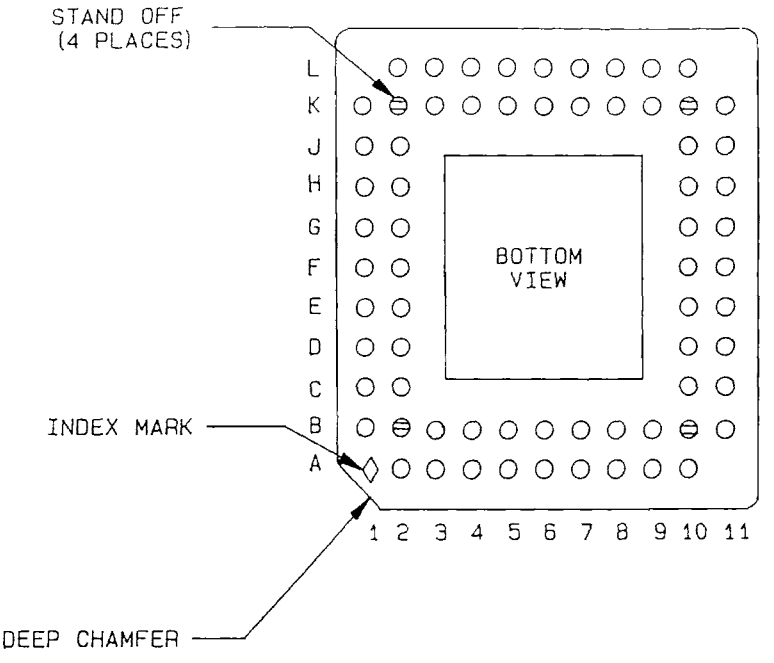
Mnemonic	Name	Description
$\overline{\text{BUS REQ}}$	Bus request	An active low output that indicates the CPU requires the bus. It becomes inactive when the CPU has acquired the bus and started the bus cycle.
$\overline{\text{BUS GNT}}$	Bus grant	An active low input from an external arbiter that indicates the CPU currently has the highest priority bus request. If the bus is not used and not locked, the CPU may begin a bus cycle, commencing with the next CPU clock. A high level will hold the CPU in Hi-Z state (Bz), three-stating the IB bus status lines (D/$\overline{\text{I}}$, R/$\overline{\text{W}}$, M/$\overline{\text{IO}}$), strobes (STRBA, $\overline{\text{STRBD}}$), and all the other lines that go three-state when this CPU does not have the bus.
$\overline{\text{BUS BUSY}}$	Bus busy	An active low, bidirectional signal used to establish the beginning and end of a bus cycle. The trailing edge (low-to-high transition) is used for sampling bits into the fault register. It is three-state in bus cycles not assigned to this CPU. However, the CPU monitors the $\overline{\text{BUS BUSY}}$ line for latching non-CPU bus cycle faults into the fault register.
$\overline{\text{BUS LOCK}}$	Bus lock	An active low, bi-directional signal used to lock the bus for successive bus cycles. During non-locked bus cycles, the $\overline{\text{BUS LOCK}}$ signal mimics the $\overline{\text{BUS BUSY}}$ signal. It is three-state during bus cycles not assigned to this CPU. The following instructions will lock the bus: INCM, DECM, SB, RB, TSB, SRM, STUB and STLB.

DISCRETE CONTROL

Mnemonic	Name	Description
DMA EN	Direct memory Access enable	An active high output that indicates the DMA is enabled. It is disabled when the CPU is initialized (reset) and can be enabled or disabled under program control (I/O commands DMAE, DMAD).
NML PWRUP	Normal power up	An active high output that is set when the CPU has successfully completed the built-in self test in the initialization sequence. It can be reset by the I/O command RNS.
SNEW	Start new	An active high output that indicates a new instruction is about to start executing in the next cycle.
$\overline{\text{TRIGO RST}}$	Trigger-go reset	An active low discrete output. This signal can be pulsed low under program control I/O address 400B (Hex) and is automatically pulsed during processor initialization.

TERMINAL CONNECTIONS

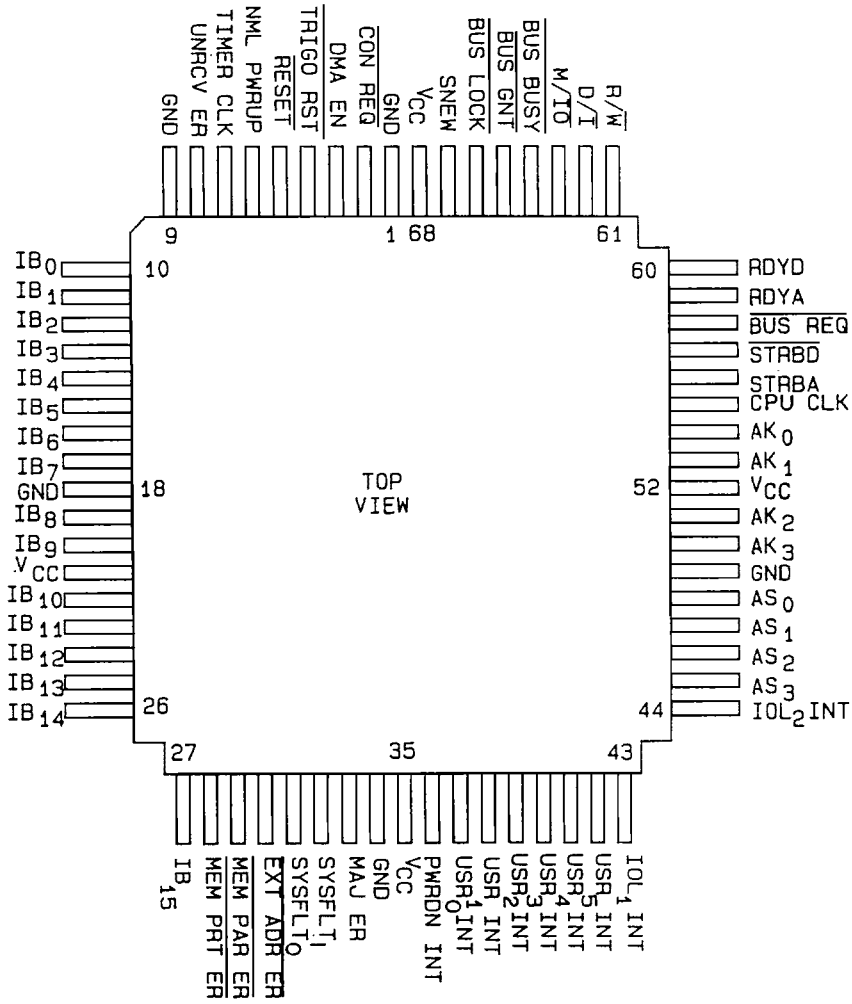
Case Outline Z



Pin	Pin name	Pin	Pin name	Pin	Pin name	Pin	Pin name
B1	V_{CC}	L2	GND	K11	RDYD	A10	GND
B2	IB_{14}	K2	UNRCV ER	K10	RDYA	B10	IOL_1 INT
C1	IB_{13}	L3	TIMER CLK	J11	BUS REQ	A9	USR_5 INT
C2	IB_{12}	K3	NML PWRUP	J10	STRBD	B9	USR_4 INT
D1	IB_{11}	L4	RESET	H11	STRBA	A8	USR_3 INT
D2	IB_{10}	K4	TRIGO RST	H10	CPU CLK	B8	USR_2 INT
E1	IB_9	L5	DMA EN	G11	AK_0	A7	USR_1 INT
E2	IB_8	K5	CON REQ	G10	AK_1	B7	USR_0 INT
F1	GND	L6	V_{CC}	F11	AK_2	A6	PWRON INT
F2	IB_7	K6	SNEW	F10	AK_3	B6	GND
G1	IB_6	L7	BUS LOCK	E11	GND	A5	MAJ ER
G2	IB_5	K7	BUS GNT	E10	AS_0	B5	$SYSFLT_1$
H1	IB_4	L8	BUS BUSY	D11	AS_1	A4	$SYSFLT_0$
H2	IB_3	K8	M/IO	D10	AS_2	B4	EXT ADR ER
J1	IB_2	L9	D/I	C11	AS_3	A3	MEM PAR ER
J2	IB_1	K9	R/W	C10	IOL_2 INT	B3	MEM PRT ER
K1	IB_0	L10	GND	B11	V_{CC}	A2	IB_{15}

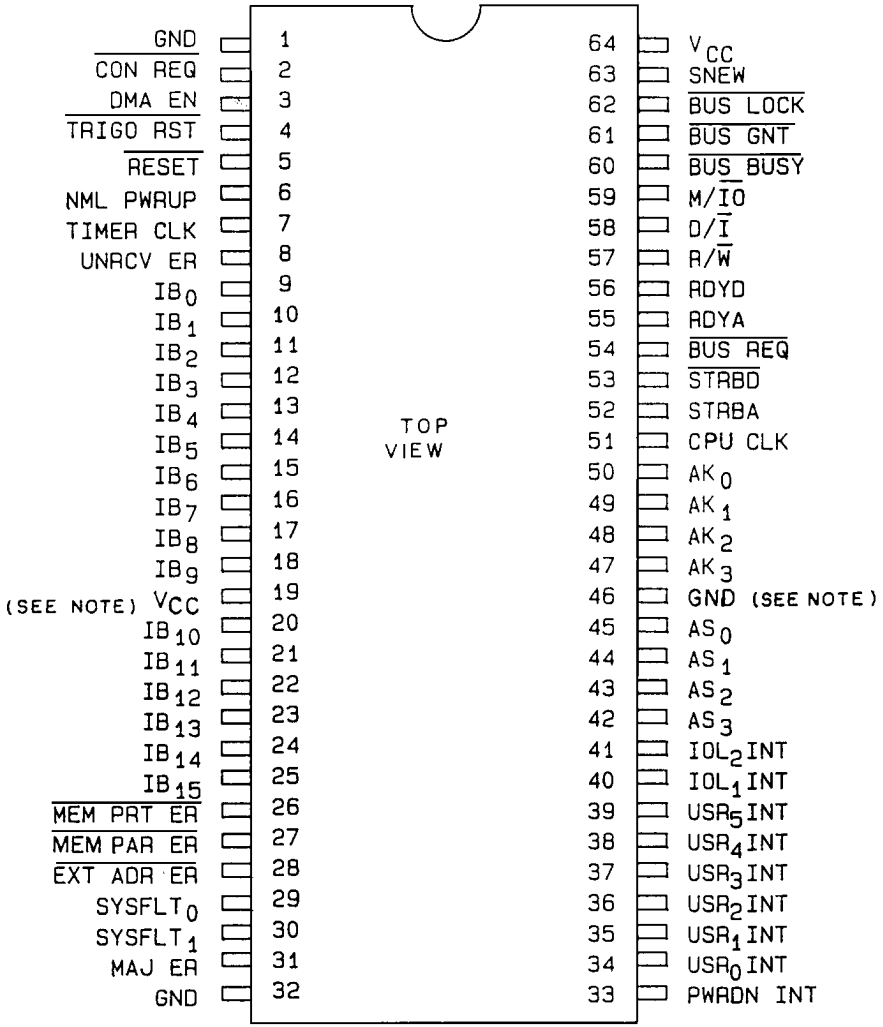
TERMINAL CONNECTIONS

Cases U and Y



TERMINAL CONNECTIONS

Cases X and T



Note: For 15 and 20MHz processors, pins 19 and 46 are not connected

Standardized Military Drawing PIN	Vendor CAGE Number	Vendor similar PIN[1]
5962-8766501TX	75569	P1750A-15GMB
5962-8766501UX	75569	P1750A-15QLMB
5962-8766501XX	75569	P1750A-15CMB
5962-8766501YX	75569	P1750A-15QGMB
5962-8766501ZX	75569	P1750A-15PGMB
5962-8766502TX	75569	P1750A-20GMB
5962-8766502UX	75569	P1750A-20QLMB
5962-8766502XX	75569	P1750A-20CMB
5962-8766502YX	75569	P1750A-20QGMB
5962-8766502ZX	75569	P1750A-20PGMB
5962-8766503TX	75569	P1750A-30GMB
5962-8766503UX	75569	P1750A-30QLMB
5962-8766503XX	75569	P1750A-30CMB
5962-8766503YX	75569	P1750A-30QGMB
5962-8766503ZX	75569	P1750A-30PGMB
5962-8766504TX	75569	P1750A-40GMB
5962-8766504UX	75569	P1750A-40QLMB
5962-8766504XX	75569	P1750A-40CMB
5962-8766504YX	75569	P1750A-40QGMB
5962-8766504ZX	75569	P1750A-40PGMB

ORDERING INFORMATION