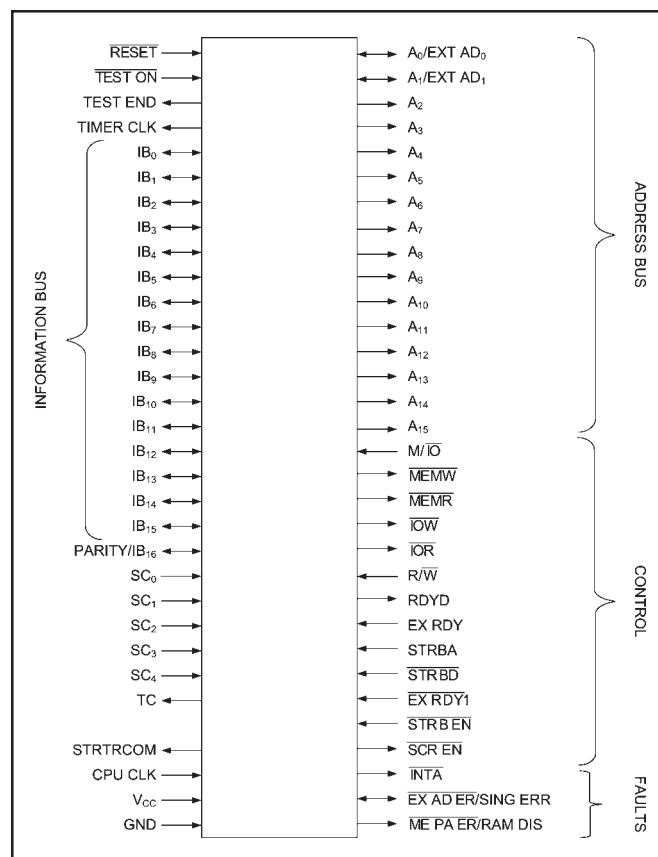# PACE1754/SOS
PROCESSOR INTERFACE CIRCUIT (PIC)
CMOS/SOS SPACE PROCESSOR
MICROPERIPHERAL

FEATURES

■ **The PACE1754 (PIC) is a support chip for the PACE1750A/AE Processors. It eliminates the SSI/MSI Logic and external system functions required in typical 1750A implementations.**

■ **Provides a significant savings in part-count and power dissipation enhancing reliability and overall system speed performance.**

■ **Provides an optimal interface when used with the PACE1753 MMU/COMBO in a full 1750A implementation.**

■ **Provides the following additional important system functions:**
  — **Programmable READY for memory and I/O**
  — **Automatic READY during self-test and internal I/O instructions**
  — **100KHz timer clock output provided**
  — **Programmable system watchdog—ranges from 1 μs to 1 minute**
  — **Programmable Bus time-out function**
  — **Memory Parity generation/detection**
  — **Error detection of unimplemented memory and/or I/O space addressing**
  — **First failing memory address register for diagnostics**
  — **High drive three-state address latches**
  — **Built-in system test program—automatically tests the PACE1750A/AE CPUs, PACE1753 MMU/COMBO, PACE1754 PIC and system address lines as well as memory and I/O strobes**
  — **System configuration decoding and buffering**
  — **Interrupt acknowledge decoder and strobe**
  — **Start up ROM support per MIL-STD-1750A**
  — **Memory or I/O READ/WRITE three-state strobes with external three-state control for DMA applications**

■ **Available with Class S manufacturing, screening, and testing.**

■ **SOS insulated substrate technology provides absolute latch-up immunity and excellent SEU tolerance.**

■ **SOS devices are fully interchangeable with application-proven SMD CMOS P1754 devices.**

■ **20, 25 and 30 MHz operation over full Military Temperature Range**

■ **Single 5V ± 10% Power Supply**

■ **Available in:**
  — **68-Lead Quad Pack with optional Gull Wing Surface Mount**

PACE1754 PROCESSOR INTERFACE CIRCUIT DESCRIPTION

The PACE1754 Processor Interface Circuit (PIC) is a single chip implementation of many special system functions that are often required when using the PACE1750A/AE, a single chip microprocessor. The PIC allows a system designer to design a higher performance, more effecient microprocessor system which uses less power and takes up less board space.

The PIC provides many important system functions. These functions are governed by respective bit positions in a programmable Control Register which is incorporated in the PIC. The individual bits of the control register are set to select the various features and are set to a specified default value upon Reset.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage Range	0.5V to +7.0V
Input Voltage Range	0.5V to V_{CC} + 0.5V
Storage Temperature Range	−65°C to +150°C
Input Current Range	−30mA to +5mA
Current applied to any output[3]	150mA
Maximum Power Dissipation[2]	1.5W
Lead Temperature Range (soldering 10 seconds)	300°C
Thermal resistance (θ_{JC}): Packages QL and QG	8°C/W

Notes:

1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2. Must withstand the added power dissipation due to short circuit test e.g., I_{OS}.
3. Duration 1 second or less.

RECOMMENDED OPERATING CONDITIONS

Case Temperature	**GND**	**V_{CC}**
−55°C to +125°C	0	4.5V to +5.5V

DC ELECTRICAL SPECIFICATIONS (Over recommended operating conditions)

Symbol	Parameter	Min	Max	Unit	Conditions[1]	
V_{IH}	Input HIGH Voltage	2.0	$V_{CC} + 0.5$	V		
V_{IL}	Input LOW Voltage	−0.5	0.8	V		
V_{CD}	Input Clamp Diode Voltage		−1.2	V	$V_{CC} = 4.5V$, $I_{IN} = -18mA$	
V_{OH}	Output HIGH Voltage	2.4		V	$V_{CC} = 4.5V$,	$I_{OH} = -8.0mA$
		$V_{CC} - 0.2$		V	$V_{IN} = 0.8V, 2.0V$	$I_{OH} = -300\mu A$
V_{OL}	Output LOW Voltage, except $A_0 - A_{15}$		0.5	V	$V_{CC} = 4.5V$,	$I_{OL} = 8.0mA$
			0.2	V	$V_{IN} = 0.8V, 2.0V$	$I_{OL} = 300\mu A$
V_{OL}	Output LOW Voltage, $A_0 - A_{15}$		0.5	V	$V_{CC} = 4.5V$,	$I_{OL} = 20.0mA$
			0.2	V	$V_{IN} = 0.8V, 2.0V$	$I_{OL} = 300\mu A$
I_{IH}	Input HIGH Current, except $IB_0 - IB_{15}$, parity/IB_{16}, SING ERR, A_0/EXT AD_0, A_1/EXT AD_1, STRBA		300	µA	$V_{IN} = V_{CC}$, $V_{CC} = 5.5V$	
I_{IH}	Input HIGH Current, $IB_0 - IB_{15}$, parity/IB_{16}, A_0/EXT AD_0, A_1/EXT AD_1		100	µA	$V_{IN} = V_{CC}$, $V_{CC} = 5.5V$	
I_{IH}	Input HIGH Current, STRBA, SING ERR		300	µA	$V_{IN} = V_{CC}$, $V_{CC} = 5.5V$	
I_{IL}	Input LOW Current, except $IB_0 - IB_{15}$, parity/IB_{16}, SING ERR, A_0/EXT AD_0, A_1/EXT AD_1, $\overline{STRBD}$, $\overline{TEST\ ON}$		−50	µA	$V_{IN} = GND$, $V_{CC} = 5.5V$	
I_{IL}	Input LOW Current, $IB_0 - IB_{15}$, parity/IB_{16}, SING ERR, A_0/EXT AD_0, A_1/EXT AD_1		−50	µA	$V_{IN} = GND$, $V_{CC} = 5.5V$	
I_{IL}	Input LOW Current, $\overline{STRBD}$, $\overline{TEST\ ON}$		300	µA	$V_{IN} = GND$, $V_{CC} = 5.5V$	
I_{OZH}	Output Three-State Current		50	µA	$V_{OUT} = 2.4V, V_{CC} = 5.5V$	
I_{OZL}	Output Three-State Current		−50	µA	$V_{OUT} = 0.5V, V_{CC} = 5.5V$	
I_{CCQC}	Quiescent Power Supply Current (CMOS Input Levels)		25	mA	$V_{IN} < 0.2V$ or $> V_{CC} - 0.2V$ $f = 0MHz$, Outputs Open, $V_{CC} = 5.5V$	
I_{CCQT}	Quiescent Power Supply Current (TTL Input Levels)		100	mA	$V_{IN} = 3.4V, f = 0MHz$, All Inputs, Outputs Open, $V_{CC} = 5.5V$	
I_{CCD}	Dynamic Power Supply Current — $f = 20MHz$		90	mA	$V_{IN} = 0V$ to V_{CC},	
	$f = 25MHz$		100	mA	$tr = tf = 2.5$ ns typ.,	
	$f = 30MHz$		125	mA	Outputs Open, $V_{CC} = 5.5V$	
I_{OS}	Output Short Circuit Current[2]	−25		mA	$V_{OUT} = GND, V_{CC} = 5.5V$	
C_{IN}	Input Capacitance		10	pF	Inputs Only	
C_{OUT}	Output/Bi-directional Capacitance		15	pF	Outputs Only (Including I/O Buffers)	

Notes:

1. $4.5V \leq V_{CC} \leq 5.5V$, $-55°C \leq T_C \leq +125°C$. Unless otherwise specified, testing shall be conducted at worst-case conditions.
2. Duration of the short should not exceed one second; only one output may be shorted at a time.

AC ELECTRICAL CHARACTERISTICS[1,2]
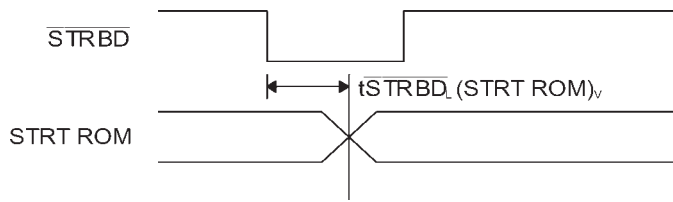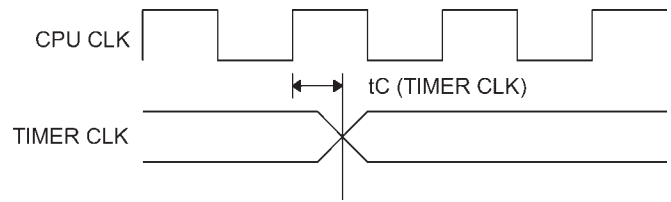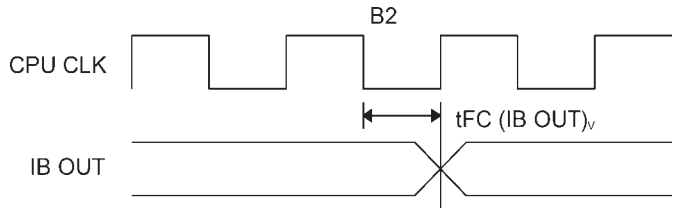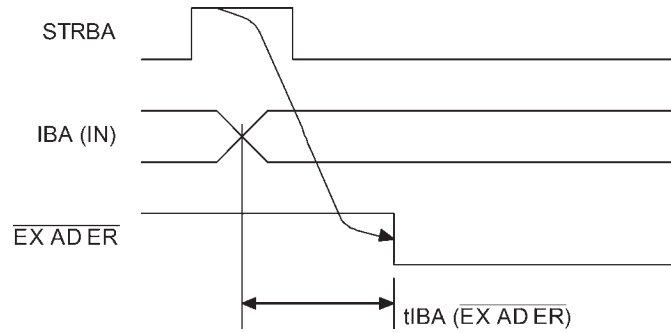(V_{CC} = 5V ± 10% Over Recommended Operating Conditions)

| Symbol	Parameter	20 MHz		25MHz		30 MHz		Unit
		Min	Max	Min	Max	Min	Max	
tEX RDY (RDYD)$_V$	Time from External Ready to Ready Data Valid		19		15		14	ns
tC (RDYD)$_V$	Time from Clock Read to Ready Data Valid		29		25		23	ns
tSTRBA$_H$ (A)$_V$	Time from Strobe Address HIGH to Address Bus Valid		29		25		23	ns
tIBA$_V$ (A)$_V$	Time from Information Bus Address to Address Bus Valid		31		27		25	ns
tFC (R)$_L$	Time from Falling Clock to Read LOW		25		21		19	ns
$\overline{STR\,BD}_H$ (R)$_H$	Time from Strobe Data HIGH to Read HIGH		25		21		19	ns
$\overline{STR\,BD}_L$ (W)$_L$	Time from Strobe Data LOW to Write LOW		27		23		21	ns
$\overline{STR\,BD}_H$ (W)$_H$	Time from Strobe Data HIGH to Write HIGH		27		23		21	ns
tIBD$_{IN}$ ($\overline{ME\,PA\,ER}$)$_L$	Time from Information Bus Data into Memory Parity Error LOW		24		20		18	ns
tIBA$_{IN}$ ($\overline{EX\,AD\,ER}$)	Time from Information Bus Address into External Address Error		32		28		26	ns
$\overline{STR\,BD}_L$ – (STRT ROM)$_V$	Time from Strobe Data LOW to Start-up ROM Valid		27		23		21	ns
tFC (IB OUT)$_V$	Time from Falling Clock to Information Bus Valid		32		28		26	ns
tC (TIMER CLK)	Time from Rising Edge of Clock to Timer Clock		32		28		26	ns
tIB IN$_V$ (IB16)	Time from Information Bus Data to Parity Valid		26		23		21	ns
tEXT AD (CLKB3)	Extended Address Setup Time	10		10		10		ns
t$\overline{EX\,RDY}$1 (RDYD)$_V$	Time from External Ready Data to Ready Data Valid		30		26		24	ns
$\overline{STR\,BD}_H$ ($\overline{SCR\,EN}$)	Time from STRBD HIGH to SCR Enable;		32		28		26	ns

Notes:

1. 4.5V ≤ V_{CC} ≤ 5.5V, –55°C ≤ T_C ≤ +125°C. Unless otherwise specified, testing shall be conducted at worst-case conditions.

2. All measurements of delay times on active signals are related to the 1.5V levels.
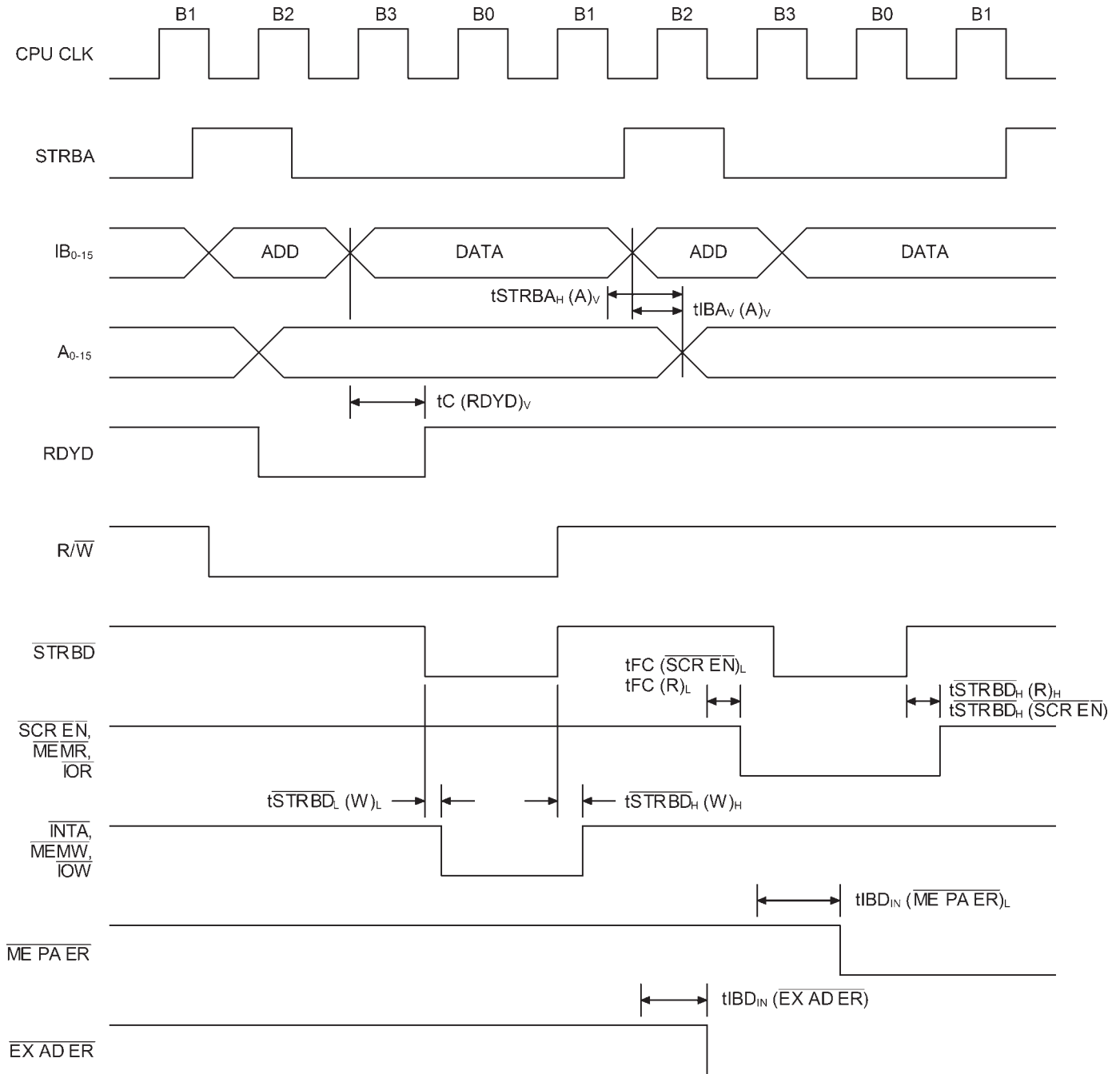
TERMINAL CONNECTIONS - PACKAGES QL AND QG

Case Outlines		U and Y			
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	GND	24	IB_{12}	47	A_3
2	SC_0	25	IB_{13}	48	GND
3	SC_1	26	IB_{14}	49	A_2
4	$\overline{TEST\ ON}$	27	IB_{15}	50	$A_1/EXT\ AD_1$
5	$\overline{RESET}$	28	$\overline{PARITY}/IB_{16}$	51	$A_0/EXT\ AD_0$
6	TEST END	29	$\overline{ME\ PA\ ER}/RAM\ DIS$	52	SC_4
7	TIMER CLK	30	$\overline{EX\ AD\ ER}/SING\ ERR$	53	SC_3
8	SC_2	31	$\overline{INTA}$	54	TC
9	V_{CC}	32	STRT ROM	55	CPU CLK
10	IB_0	33	V_{CC}	56	STRBA
11	IB_1	34	GND	57	$\overline{STRBD}$
12	IB_2	35	A_{15}	58	$\overline{STRBEN}$
13	IB_3	36	A_{14}	59	EX RDY
14	IB_4	37	A_{13}	60	RDYD
15	IB_5	38	A_{12}	61	$R/\overline{W}$
16	IB_6	39	A_{11}	62	GND
17	IB_7	40	A_{10}	63	$M/\overline{IO}$
18	$\overline{EX\ RDY_1}$	41	A_9	64	$\overline{MEMW}$
19	IB_8	42	A_8	65	$\overline{MEMR}$
20	IB_9	43	A_7	66	$\overline{IOW}$
21	GND	44	A_6	67	$\overline{IOR}$
22	IB_{10}	45	A_5	68	V_{CC}
23	IB_{11}	46	A_4		

STRT ROM

$\overline{STRBD}$

$t\overline{STRBD}_L$ (STRT ROM)$_V$

STRT ROM

Timer Clk

CPU CLK

tC (TIMER CLK)

TIMER CLK

IB Bus Output (0:15)

B2

CPU CLK

tFC (IB OUT)$_V$

IB OUT

$\overline{EX\ AD\ ER}$

STRBA

IBA (IN)

$\overline{EX\ AD\ ER}$

tIBA ($\overline{EX\ AD\ ER}$)

Extended Addresses (0:1)

B1   B2   B3

CPU CLK

tEXT AD (CLKB3)

EXT AD (0:1)

IB 16

IB IN (0:15)

tIB IN$_V$ (IB16)

IB 16
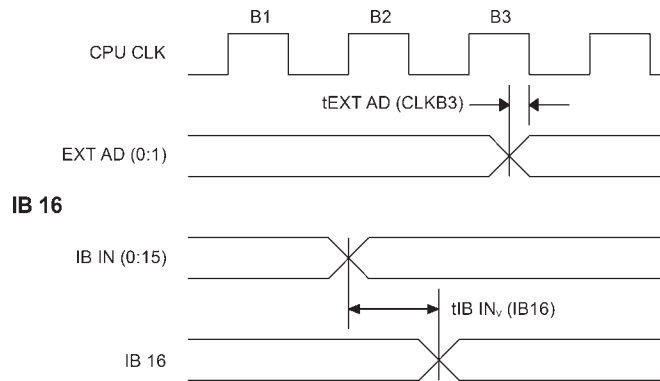
Note: All time measurements on active signals relate to 1.5V levels.

RDYD Timing
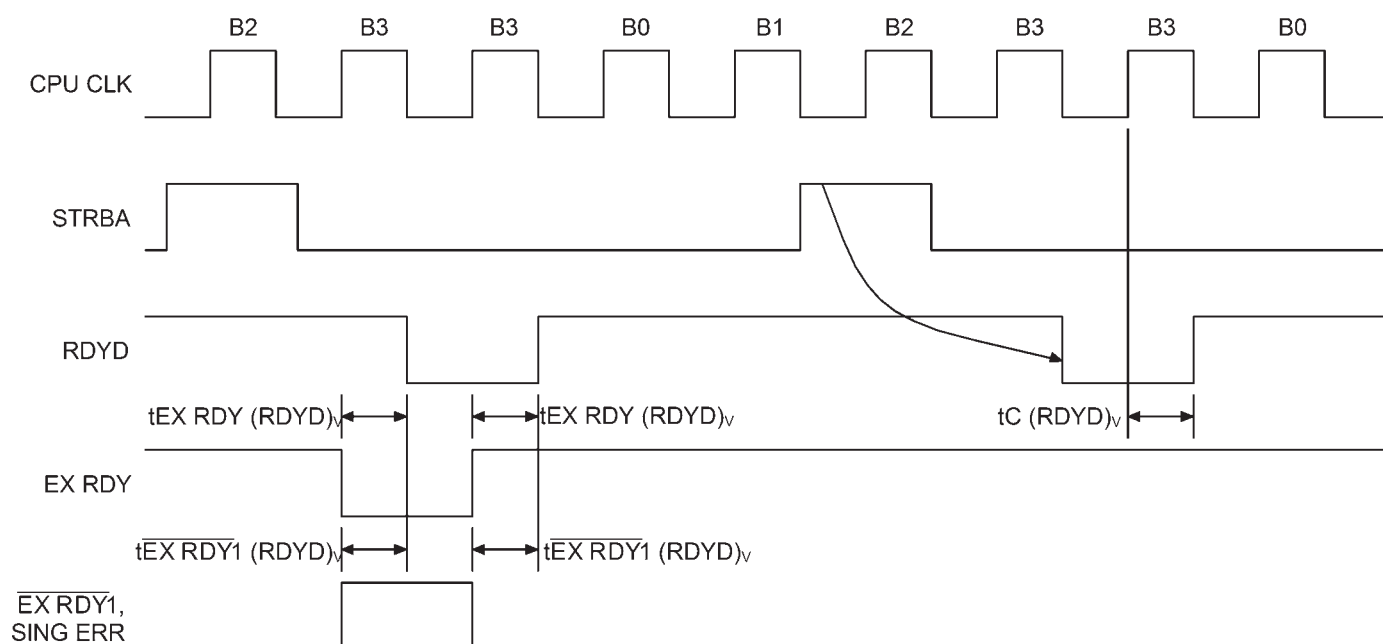
TEST END Timing[1]
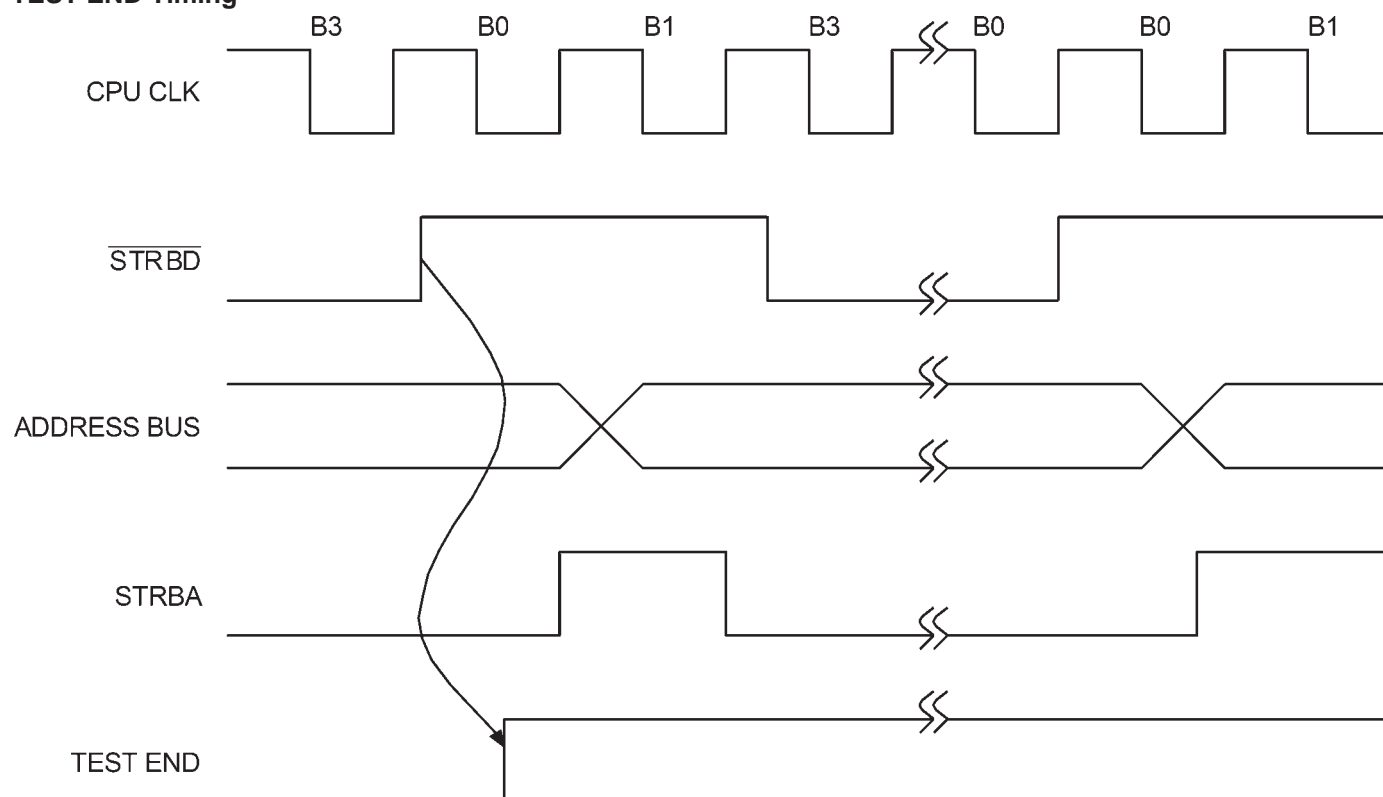
Notes:

1. The last two instructions executed during system test are: XIO RA, 1F44, 0 and JC 7, 0000 hex, 0. After execution of the <u>IOW</u> bus cycle, the XIO proceeds by filling the instruction pipe with two memory read bus cycles where the opcode 7070 hex and 0000 hex are entered to the processor. As from the end of <u>STRBD</u> in the second cycle, TEST END is asserted. At this point, the execution of IC starts by first issuing two fetch cycles from the "old PC" (from addresses XXXX & XXXX+1). The data will be taken from system memory (because TEST END is asserted) but both the address and data are irrelevent. Following that, IC will start filling the pipe from address 0000 hex and 0001 hex, now from the system memory to start user's program execution.

2. All time measurements on active signals relate to 1.5V levels.

Address Bus and Strobes

CPU CLK — B1 B2 B3 B0 B1 B2 B3 B0 B1

STRBA

IB_{0-15} — ADD DATA ADD DATA

$tSTRBA_H (A)_V$ $tIBA_V (A)_V$

A_{0-15}

$tC (RDYD)_V$

RDYD

$R/\overline{W}$

$\overline{STRBD}$

$tFC (\overline{SCR\ EN})_L$
$tFC (R)_L$
$t\overline{STRBD}_H (R)_H$
$t\overline{STRBD}_H (\overline{SCR\ EN})$

$\overline{SCR\ EN}, \overline{MEMR}, \overline{IOR}$

$t\overline{STRBD}_L (W)_L$ $t\overline{STRBD}_H (W)_H$

$\overline{INTA}, \overline{MEMW}, \overline{IOW}$

$tIBD_{IN} (\overline{ME\ PA\ ER})_L$

$\overline{ME\ PA\ ER}$

$tIBD_{IN} (\overline{EX\ AD\ ER})$

$\overline{EX\ AD\ ER}$

Note: All time measurements on active signals relate to 1.5V levels.

TEST CIRCUITS

Standard Output (Non Three-State)
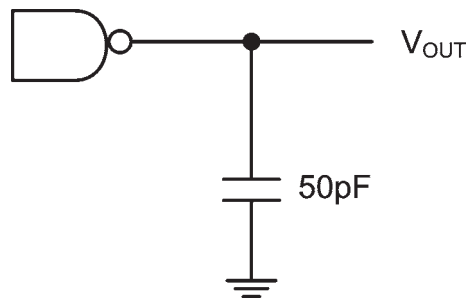
V_{OUT}

50pF

Note: All time measurements on active signals relate to 1.5V levels.

Three-State

V_O

$R_L = 525\Omega \pm 10\%$

V_{OUT}

50pF
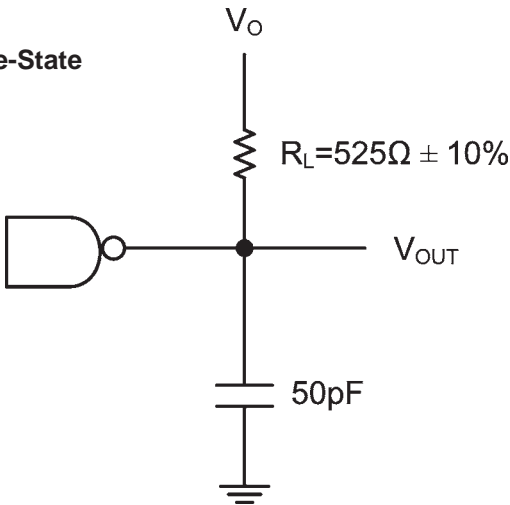
Parameter	V_O	V_{MEA}
TPLZ	$\geq 3V$	0.5V
TPHZ	0V	$V_{CC} - 0.5V$
TPXL	$V_{CC}/2$	1.5V
TPXH	$V_{CC}/2$	1.5V

PIN FUNCTIONS

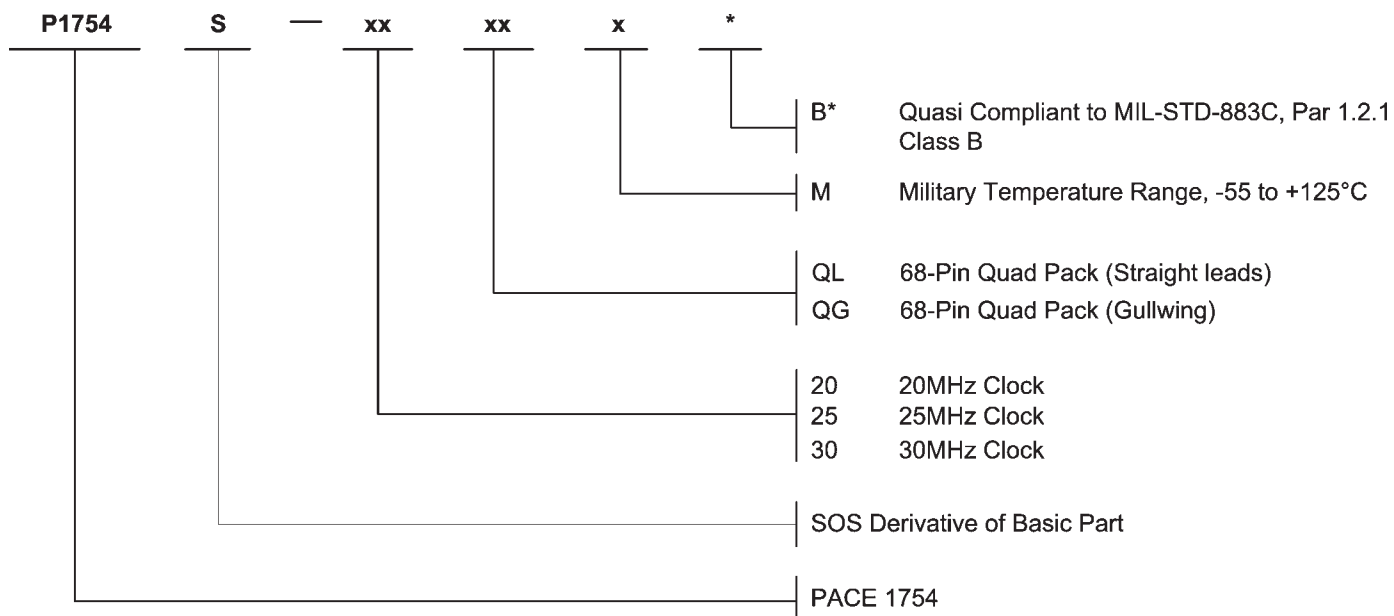| Symbol	Name	Description
CPU CLK	CPU Clock	A single-phase input clock signal (0-40MHz, 40% to 60% duty cycle.)
STRBA	Strobe Address	An active HIGH input which latches the contents of IB(0:15) into the address latches.
$\overline{STRBD}$	Strobe Data	An active LOW input which is used for writing or reading data to or from the device and also to produce the external memory and I/O strobes.
TIMER CLK	Timer Clock	A 100KHz output (fixed frequency) based on the programmed operating frequency of the CPU clock.
$\overline{MEMW}$	Memory Write Strobe	An active LOW output produced in memory write cycles.
$\overline{MEMR}$	Memory Read Strobe	An active LOW output produced in memory read cycles.
$\overline{IOW}$	I/O Write Strobe	An active LOW output produced in output write cycles.
$\overline{IOR}$	I/O Read Strobe	An active LOW output produced in input read cycles.
$\overline{INTA}$	Interrupt Acknowledge Strobe	An active LOW output produced after any interrupt, corresponding to an output write to address 1000 (hex).
$\overline{SCR\ EN}$	System Configuration	An active LOW output (in 64 pin only) produced any time an input read from address 8410 (hex), read system configuration is executed.
$\overline{STRB\ EN}$	Strobe Enable	An active LOW input, enabling the active state of the address outputs and the $\overline{MEMR}$, $\overline{MEMQ}$, $\overline{IOR}$, and $\overline{IOW}$ outputs. When at a logic "1" (if enabled by bits EST, EAD of the control register) it will correspondingly enable the three-state state of the above signals.
IB_0 - IB_{15}	Information Bus (0:15)	A bi-directional time multiplexed bus. It is an input during the address phase of any bus cycle and also during the data phase when writing. It is an output during the data phase when reading from the device.
IB_{16}	Information Bus (16)	A bi-directional line. It is an output during write cycles and an input during read cycles. It is used to implement the parity function at the system level.
A(0:1)/ EX AD(0:1), A(2:15)	Address Bus (0:15)	An active HIGH output bus. Contains the address of the current bus cycle as latched by the end of STRBA. In system configurations including the MMU function, the only active lines during memory are A(4:15). In this case, A(2:3) are high impedance (don't care) and A(0:1) turn into inputs called Extended Addresses, EXT ADR (0:1). In this case, these two lines supplied by the MMU, will be used to operate the programmable ready generation during bus cycles.
M/$\overline{IO}$	Memory I/O	An input qualifier indicating the nature of the current bus cycle.

PIN FUNCTIONS (Continued)

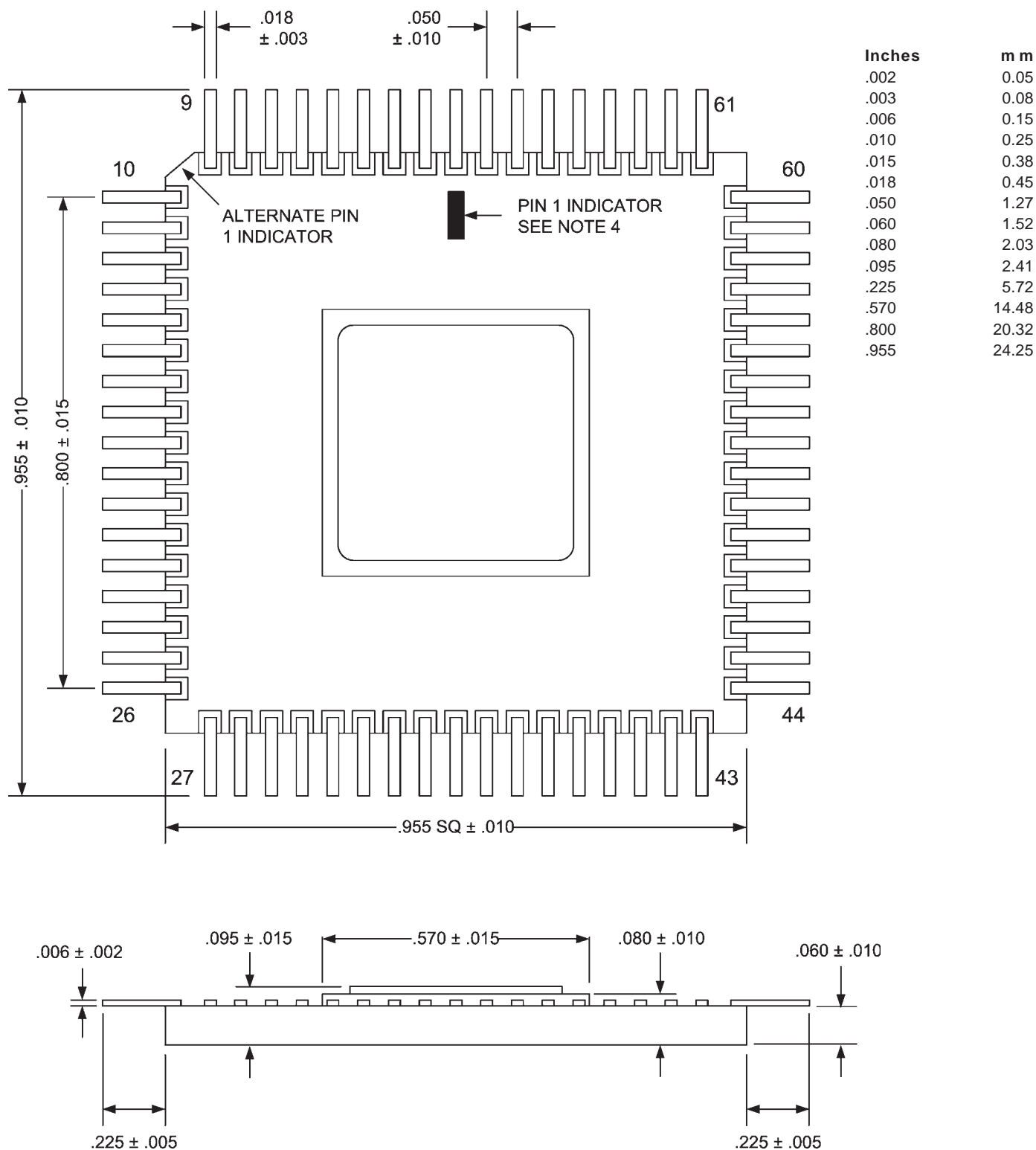| Symbol	Name	Description
R/$\overline{\text{W}}$	Read or Write	An input qualifier indicating the nature of the current bus cycle, either Read (1) or Write (0).
$\overline{\text{RESET}}$	External Reset	An active LOW input used to initialize the device's hardware.
$\overline{\text{TEST ON}}$	System Test Enable	An active LOW input used to enable the execution of the System Test built into the device, immediately after completion of the P1750A/AE initialization and before fetching any instruction from the user program.
TEST END	System Test End	An active HIGH output indicating whether the system test in the device has been completed. Whenever the system test is disabled by the $\overline{\text{TEST ON}}$ signal, the TEST END output will be at a logical "1" immediately after RESET is removed.
STRT ROM	Start Up ROM	An output following the execution of the ESUR and DSUR, I/O commands as defined in MIL-STD-1750A. It will be at the logical "1" level after executing ESUR and at the logical "0" level after executing DSUR. Initially, it defaults to a logical "1".
RDYD	Ready Data	An active HIGH output to be connected to the P1750A/AE input to control the bus cycle termination.
EX RDY	External Ready Data	An active HIGH input which at logical "0" overrides the internal RDYD generation and forces it to a logical "0".
$\overline{\text{EX RDY}}_1$	External Ready Data	An active LOW input which at logical "1" overrides the internal RDYD generation and forces it to a logical "0".
$\overline{\text{ME PA ER}}$/ RAM DIS	Memory Parity Error	An active LOW output indicating a parity error when reading from memory. It becomes an active HIGH output called RAM DISABLE for handshaking with the P1753 MMU when the device is programmed to support EDAC.
$\overline{\text{EX AD ER}}$/ SING ERR	Illegal Address Error	An active LOW output indicating an illegal address error when referencing memory or I/O. It becomes an active HIGH output called SINGLE ERROR for handshaking with the P1753 MMU when the device is programmed to support EDAC.
TC	Terminal Count	An active HIGH output indicating a Bus time out or a watchdog trigger.
SC_0–SC_4	System Configuration	Inputs which are buffered onto IB_0–IB_4 when executing an I/O read from I/O address 8410 (hex), system configuration.
GND	Ground	0 volts system ground.
V_{CC}	Power Supply	5 volts ± 10% power supply.

Standardized Military Drawing Part Number	Pyramid Semiconductor CAGE Number	Pyramid Semiconductor Part Number
5962-8864201UX	3DTT2	P1754-20QLMB
5962-8864201YX	3DTT2	P1754-20QGMB
5962-8864201ZX	3DTT2	P1754-20PGMB
5962-8864202UX	3DTT2	P1754-30QLMB
5962-8864202YX	3DTT2	P1754-30QGMB
5962-8864202ZX	3DTT2	P1754-30PGMB
5962-8864203UX	3DTT2	P1754-40QLMB
5962-8864203YX	3DTT2	P1754-40QGMB
5962-8864203ZX	3DTT2	P1754-40PGMB
5962-8864204TX	3DTT2	P1754-20GMB
5962-8864204XX	3DTT2	P1754-20CMB
5962-8864205TX	3DTT2	P1754-30GMB
5962-8864205XX	3DTT2	P1754-30CMB
5962-8864206TX	3DTT2	P1754-40GMB
5962-8864206XX	3DTT2	P1754-40CMB

ORDERING INFORMATION

P1754   S — xx   xx   x   *

B*   Quasi Compliant to MIL-STD-883C, Par 1.2.1 Class B

M   Military Temperature Range, -55 to +125°C

QL   68-Pin Quad Pack (Straight leads)
QG   68-Pin Quad Pack (Gullwing)

20   20MHz Clock
25   25MHz Clock
30   30MHz Clock

SOS Derivative of Basic Part

PACE 1754

CASE OUTLINE 1:

68 Lead Quad Pack with Straight Leads (Ordering Code QL)

Inches	m m
.002	0.05
.003	0.08
.006	0.15
.010	0.25
.015	0.38
.018	0.45
.050	1.27
.060	1.52
.080	2.03
.095	2.41
.225	5.72
.570	14.48
.800	20.32
.955	24.25

NOTES:

1) Dimensions are in inches.

2) Metric equivalents are given for general information only.

3) Unless otherwise specified, tolerances are .02 (0.5 mm) for two place decimals and .005 (0.13 mm) for three place decimals.

4) Pin 1 indicator can be either rectangle, dot, or triangle at specified location or referenced to the uniquely beveled corner.

5) Corners indicated as notched may be either notched or square.

CASE OUTLINE 2:

68 Lead Quad Pack with Gullwing Leads (Ordering Code QG)
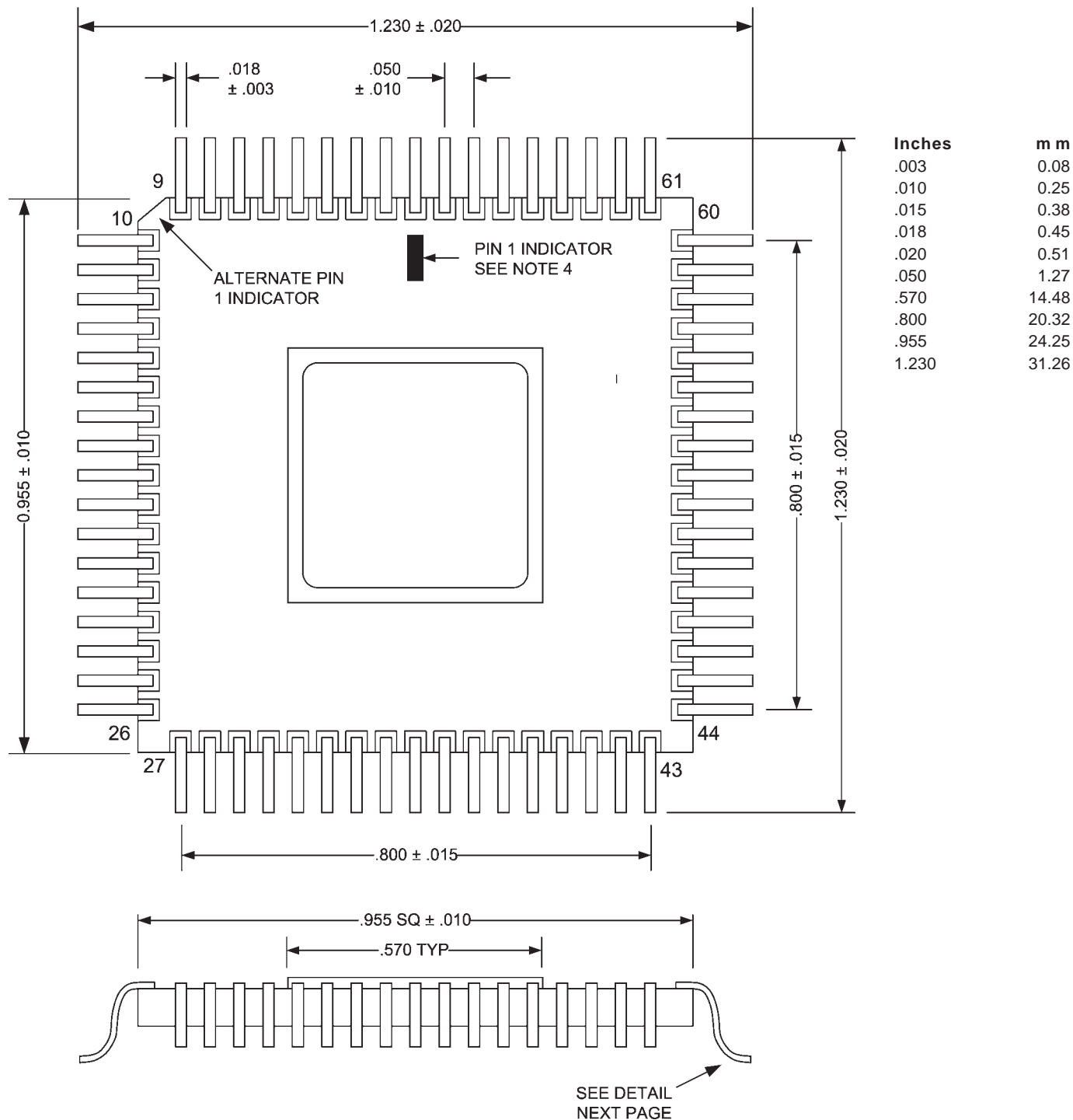
Inches	m m
.003	0.08
.010	0.25
.015	0.38
.018	0.45
.020	0.51
.050	1.27
.570	14.48
.800	20.32
.955	24.25
1.230	31.26

NOTES:

1) Dimensions are in inches.

2) Metric equivalents are given for general information only.

3) Unless otherwise specified, tolerances are .02 (0.5 mm) for two place decimals and .005 (0.13 mm) for three place decimals.

4) Pin 1 indicator can either be rectangle, dot, or triangle at specified location or referenced to the uniquely beveled corner.

5) Corners indicated as notched my be either notched or square (with radius).

6) Case 2 is derived from Case 1 by forming the leads to the shown gullwing configuration.

LEAD FORM DETAIL

Symbol	INCHES	
	Min	Max
A	0.048	0.090
A1	0.011	0.031
B	0.016	0.021
C	0.004	0.008
e1	0.050 BSC	
D	1.210	1.250
D1	0.945	0.965
D2	0.800 BSC	
E	1.210	1.250
E1	0.945	0.965
E2	0.800 BSC	
L*	0.270 Nominal	
L0	0.120	0.210
L3	0.040	0.050
L4	0.086	0.109
R1	0.018	0.020
R2	0.018	0.020
Φ_1	4°	8°
Φ_2	-1°	7°
A0**		0.141

* Lead length in the straight lead configuration, prior to leadforming (used for all test and in-process WIP operations).

** Measured from the highest of the top of the leads or the top of the lid.

REVISIONS

DOCUMENT NUMBER:		MICRO-9	
DOCUMENT TITLE:		PACE1754/SOS MMU/COMBO	
REV.	ISSUE DATE	ORIG. OF CHANGE	DESCRIPTION OF CHANGE
ORIG	May-89	RKK	New Data Sheet
A	Jul-04	JDB	Added Pyramid logo
B	Aug-05	JDB	Re-created electronic version