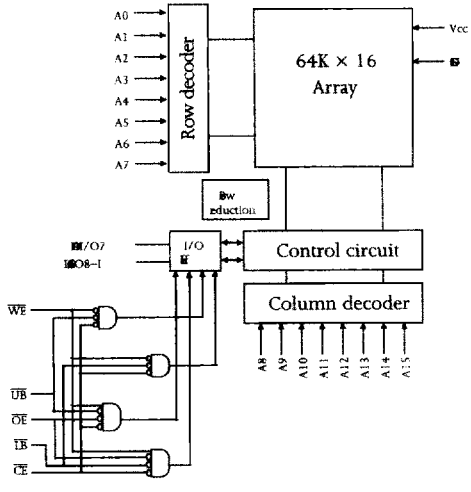
Advance information

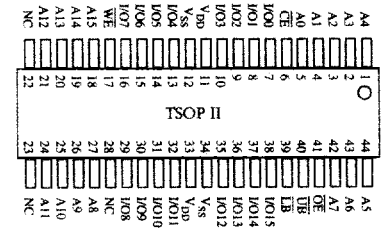
Features

- Optimized design for battery operated portable systems
- Intelliwatt™ active power reduction circuitry
- Organization: 65,536 words × 16 bits
- 1.65V to 1.95V operating range (JESD 8-7)
- High speed
  - 35/55/75/100 ns address access time
- Low power consumption
  - Active: 36 mW max (100 ns cycle)
  - Typical: <10 mW (100 ns cycle)
  - Standby: 3.6 µW max
  - Very low DC component in active power
- 1.25V data retention
- Equal access and cycle times
- Easy memory expansion with $\overline{CE}$, $\overline{OE}$ inputs
- LVTTL/LVCMOS-compatible, three-state I/O
- JEDEC registered packaging
  - 44-pin TSOP II package
  - 48-ball csp 8mm × 6mm BGA
- Center power and ground pins for low noise
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA
- Industrial temperature range available (-40 to +85 °C)
- Other voltage versions available
  - 2.3V to 3.0V (AS7C251026LL)
  - 3.3V version available (AS7C31026LL)

Logic block diagram



Pin arrangement



48-CSP Ball-Grid-Array Package (shading indicates no ball)

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A_0	A_1	A_2	NC
B	I/O_8	$\overline{UB}$	A_3	A_4	$\overline{CE}$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2
D	V_{SS}	I/O_{11}	NC	A_7	I/O_3	V_{DD}
E	V_{DD}	I/O_{12}	NC	NC	I/O_4	V_{SS}
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	no ball	A_8	A_9	A_{10}	A_{11}	no ball

Selection guide

	7C181026LL-35	7C181026LL-55	7C181026LL-70	7C181026LL-100	Unit
Maximum address access time	35	55	70	100	ns
Maximum output enable access time	15	25	35	50	ns
Maximum operating current	25	19	15	10	mA
Maximumstandby current	1	1	1	1	µA

Functional description

The AS7C181026LL is a high performance CMOS 1,048,576-bit Static Random Access Memory (SRAM) organized as 65,536 words × 16 bits. It is designed for portable applications where fast data access, long battery life, low heat dissipation, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 35/55/75/100 ns are ideal for high performance applications. The chip enable input $\overline{CE}$ permits easy memory expansion with multiple-bank memory systems.

When $\overline{CE}$ is High, or when $\overline{UB}$ and $\overline{LB}$ are simultaneously pulled Low, the device enters standby mode. The AS7C181026LL is guaranteed not to exceed 3.6 µW power consumption in CMOS standby mode. This device also offers data retention down to 1.5V.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and chip enable ($\overline{CE}$). Data on the input pins I/O0-I/O15 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and chip enable ($\overline{CE}$), with write enable ($\overline{WE}$) High. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

The devices provide multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read. $\overline{LB}$ controls the lower bits, I/O0–I/O7, and $\overline{UB}$ controls the higher bits, I/O8–I/O15.

The device is packaged in common industry standard packages. Chip scale BGA packaging, easy to use in manufacturing, provides the smallest possible footprint. This 48-ball JEDEC registered package has a ball pitch of 0.75 mm and external dimensions of 8 mm × 6 mm.

Low power design

In the AS7C181026LL design, priority was placed on low power, while maintaining moderately high performance. To reduce standby and data retention current, a 6-transistor memory cell was utilized. Active power was reduced considerably over traditional designs by using Intelliwatt™ power reduction circuitry. With Intelliwatt, SRAM powers down unused circuits between access operations, providing incremental power savings. During periods of inactivity, Intelliwatt SRAM power consumption approaches fully deactivated standby power, even though the chip is enabled. This power savings, both in active and inactive modes, results in longer battery life, and better system marketability. All chip inputs and outputs are TTL-compatible, and operation is from a single power supply. The supply voltage range for the AS7C181026LL conforms to JEDEC standard JESD 8-7.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Voltage on any input pin relative to GND	V_t	−1	+5.5	V
Voltabe on any I/O pin	V_t	−1	V_{DD} + 0.5	V
Power dissipation	P_D	–	1.0	W
Storage temperature (plastic)	T_{stg}	−55	+150	°C
DC output current	I_{out}	–	50	mA

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O0–I/O7	I/O8–I/O15	Mode
H	X	X	X	X	High Z	High Z	Standby, power down
L	H	L	L	H	D_{OUT}	High Z	Read I/O0–I/O7
L	H	L	H	L	High Z	D_{OUT}	Read I/O8–I/O15
L	H	L	L	L	D_{OUT}	D_{OUT}	Read I/O0–I/O15
L	L	X	L	L	D_{IN}	D_{IN}	Write I/O0–I/O15
L	L	X	L	H	D_{IN}	High Z	Write I/O0–I/O7
L	L	X	H	L	High Z	D_{IN}	Write I/O8–I/O15
L	X	H	X	X	High Z	High Z	Output disable
X	X	X	H	H	High Z	High Z	Disable, power down

Key: X = don't care, L = Low, H = High

Recommended operating conditions

Parameter		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{DD}	1.65	1.8	1.95	V
		V_{SS}	0.0	0.0	0.0	V
Input voltage		V_{IH}	2.0	–	V_{DD} + 0.5	V
		V_{IL}	−0.5†	–	0.8	V
Ambient operating temperature	Commercial	T_A	0	–	70	°C
	Industrial	T_A	-40	–	85	°C

† V_{IL} min = −3.0V for pulse width less than $t_{RC}/2$.

DC operating characteristics

			-35		-55		-70		-100		
Parameter	Symbol	Test conditions	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Input leakage current	$\lvert I_{LI} \rvert$	$0V \le V_{in} \le V_{DD}$	–	1	–	1	–	1	–	1	µA
Output leakage current	$\lvert I_{LO} \rvert$	Outputs disabled, $0V \le V_{out} \le V_{DD}$	–	1	–	1	–	1	–	1	µA
Operating power supply current	I_{CC}	$\overline{CE} \le V_{IL}$, V_{DD} = Max, $f = f_{Max} = 1/t_{RC}$	–	25	–	19	–	15	–	10	mA
	I_{CC1}	$\overline{CE} = V_{SS}$, V_{DD} = Max, f = 0		0.1		0.1		0.1		0.1	mA
Standby power supply current	I_{SB}	$\overline{CE} \ge V_{IH}$, V_{DD} = Max, $f = f_{Max} = 1/t_{RC}$	–	0.1	–	0.1	–	0.1	–	0.1	mA
	I_{SB1}	$\overline{CE} \ge V_{DD}-0.2V$, V_{DD} = Max, $V_{in} \le V_{SS} + 0.2V$ or $V_{in} \ge V_{DD} - 0.2V$, f = 0	–	1	–	1	–	1	–	1	µA
Output voltage	V_{OL}	I_{OL} = 4 mA, V_{DD} = Min	–	0.4	–	0.4	–	0.4	–	0.4	V
		I_{OL} = 100 µA, V_{DD} = Min	–	0.1	–	0.1	–	0.1	–	0.1	
	V_{OH}	I_{OH} = −4 mA, V_{DD} = Min	2.4	–	2.4	–	2.4	–	2.4	–	V
		I_{OH} = −100 µA, V_{DD} = Min	V_{DD} - 0.1	–	V_{DD} - 0.1	–	V_{DD} - 0.1	–	V_{DD} - 0.1	–	

Capacitance

(f = 1 MHz, T_A = 25°C, V_{DD} = 3.3V)

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$, $\overline{LB}$, $\overline{UB}$	V_{in} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O	V_{in} = V_{out} = 0V	7	pF

Outputs disabled in all cases.

I_{CC} = worst case power consumption.

I_{SB1} = current for the disabled, bus-active condition.

I_{CC1} = enabled, bus-inactive condition.

I_{SB} = "full standby" or the disabled, bus-inactive condition.

I_{CCDR} = current in data retention (reduced VDD) mode.

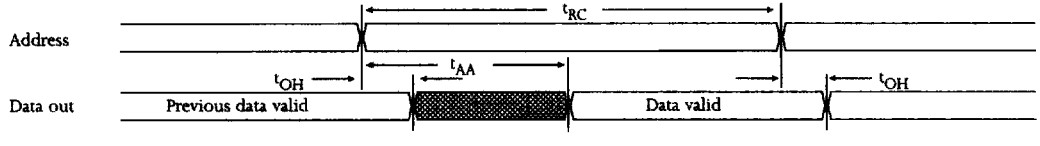
Read cycle [3]

		35		55		70		100			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}	35	–	55	–	70	–	100	–	ns	
Address access time	t_{AA}	–	35	–	55	–	70	–	100	ns	3
Chip enable access time	t_{ACE}	–	35	–	55	–	70	–	100	ns	3, 12
Output enable (OE) access time	t_{OE}	–	10	–	20	–	20	–	25	ns	
Output hold from address change	t_{OH}	3	–	3	–	3	–	3	–	ns	5
Chip enable Low to output in Low Z	t_{CLZ}	3	–	3	–	3	–	3	–	ns	4, 5, 12
Chip enable High to output in High Z	t_{CHZ}	–	10	–	10	–	10	–	15	ns	4, 5, 12
OE Low to output in Low Z	t_{OLZ}	0	–	0	–	0	–	0	–	ns	4, 5
OE High to output in High Z	t_{OHZ}	–	10	–	10	–	10	–	15	ns	4, 5
Power up time	t_{PU}	0	–	0	–	0	–	0	–	ns	4, 5, 12
Power down time	t_{PD}	–	35	–	55	–	70	–	70	ns	4, 5, 12

Key to switching waveforms

Rising input Falling input Undefined output/don't care

Read waveform 1 [6,7,9]



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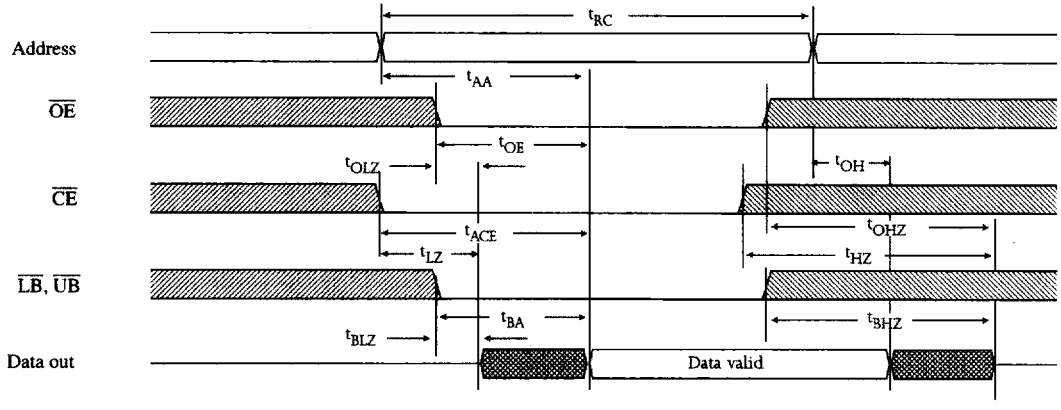
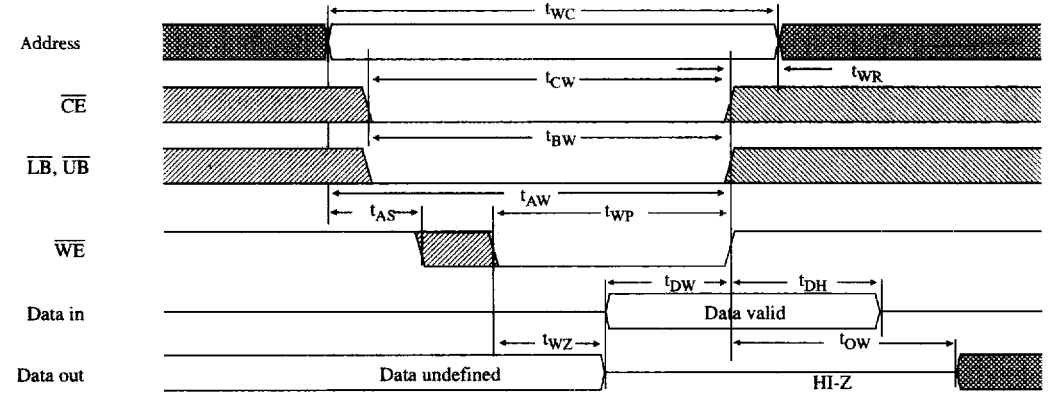
Read waveform 2 [6,8,9]



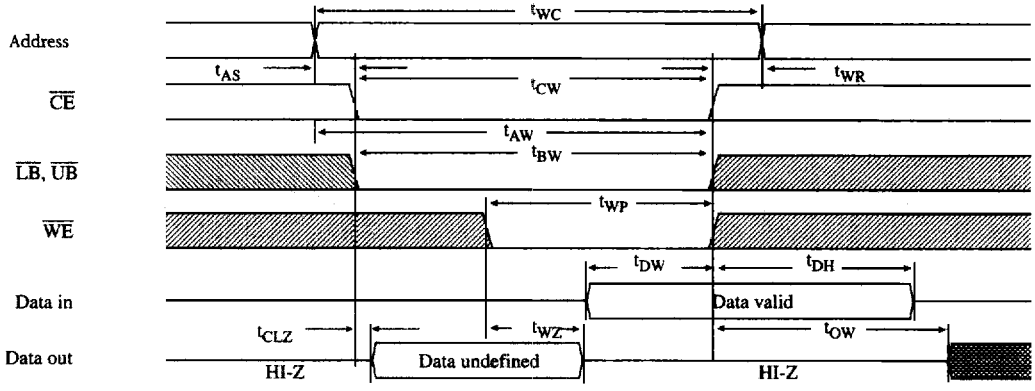
Write cycle

		35		55		70		100			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Write cycle time	t_{WC}	35	–	55	–	70	–	100	–	ns	
Chip enable to write end	t_{CW}	30	–	40	–	40	–	80	–	ns	12
Address setup to write end	t_{AW}	30	–	40	–	50	–	80	–	ns	
Address setup time	t_{AS}	0	–	0	–	0	–	0	–	ns	12
Write pulse width	t_{WP}	30	–	40	–	50	–	80	–	ns	
Address hold from end of write	t_{AH}	0	–	0	–	0	–	0	–	ns	
Data valid to write end	t_{DW}	25	–	25	–	25	–	35	–	ns	
Data hold time	t_{DH}	0	–	0	–	0	–	0	–	ns	4, 5
Write enable to output in High Z	t_{WZ}	–	10	–	10	–	10	–	10	ns	4, 5
Output active from write end	t_{OW}	5	–	5	–	5	–	5	–	ns	4, 5

Write waveform 1 [10,11]



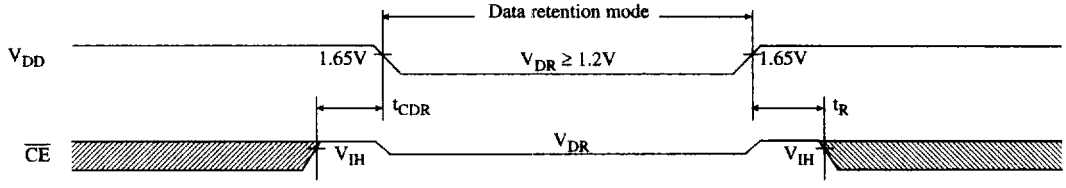
Write waveform 2 [10,11]



Data retention characteristics

Parameter	Symbol	Test conditions	Min	Max	Unit	Notes
V_{DD} for data retention	V_{DR}	V_{DD} = 1.2V	1.2	–	V	
Data retention current	I_{CCDR}	$\overline{CE} \geq V_{DD}-0.2V$	–	0.4	µA	5
Chip deselect to data retention time	t_{CDR}	$V_{in} \geq V_{DD}-0.2V$ or $V_{in} \leq 0.2V$	0	–	ns	5
Operation recovery time	t_R		t_{RC}	–	ns	5

Data retention waveform



AC test conditions

- Output load: see Figure B, except as noted.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

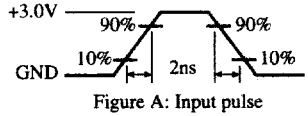


Figure A: Input pulse

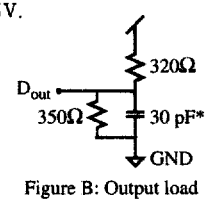


Figure B: Output load

Thevenin Equivalent:

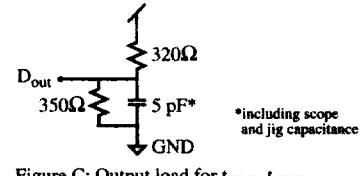


Figure C: Output load for t_{CLZ}, t_{CHZ}, t_{OLZ}, t_{OHZ}, t_{OW}, t_{WZ}, t_{BLZ}, t_{BHZ}

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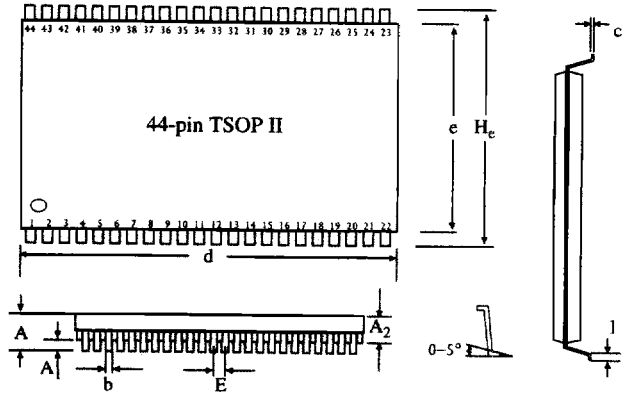
Notes

1 During V_{DD} power-up, a pull-up resistor to V_{DD} on $\overline{CE}$ is required to meet I_{SB} specification.
2 This parameter is sampled and not 100% tested.
3 For test conditions, see *AC Test Conditions*, Figures A, B, C.
4 These parameters are specified with C_L = 5pF as in Figure C. Transition is measured ±500mV from steady-state voltage.
5 This parameter is guaranteed but not tested.
6 $\overline{WE}$ is High for read cycle.
7 $\overline{CE}$ and $\overline{OE}$ are Low for read cycle.
8 Address valid prior to or coincident with $\overline{CE}$ transition Low.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 $\overline{CE}$ or $\overline{WE}$ must be High during address transitions.
11 All write cycle timings are referenced from the last valid address to the first transitioning address.

Package dimensions



	44-pin TSOP II	
	Min (mm)	Max (mm)
A		1.2
A_1	0.05	
A_2	0.95	1.05
b	0.25	0.45
c	0.15 (typical)	
d	20.85	21.05
e	10.06	10.26
H_e	11.56	11.96
E	0.80 (typical)	
l	0.40	0.60

AS7C181026LL ordering codes

Package \ Access time		35 ns	55 ns	70 ns	100 ns
TSOP II, 18.4×10.2 mm	Commercial	AS7C181026LL-35TC	AS7C181026LL-55TC	AS7C181026LL-70TC	AS7C181026LL-100TC
	Industrial	AS7C181026LL-35TI	AS7C181026LL-55TI	AS7C181026LL-70TI	AS7C181026LL-100TI
CSP BGA	Commercial	AS7C181026LL-35BC	AS7C181026LL-55BC	AS7C181026LL-70BC	AS7C181026LL-100BC
	Industrial	AS7C181026LL-35BI	AS7C181026LL-55BI	AS7C181026LL-70BI	AS7C181026LL-100BI

AS7C181026LL part numbering system

AS7C	18	1026LL	–XX	X	C
SRAM prefix	3=3.3V CMOS 25=2.5V CMOS 18=1.8V CMOS	Device number	Access time	Package:T=TSOP type 2 B=CSP BGA	Temperature range, C =Commercial:0°C to 70°C I =Industrial:-40°C to 85°C

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