GAL6001

High Performance E²CMOS®
Generic Array Logic™

2

FEATURES

- **ELECTRICALLY ERASABLE CELL TECHNOLOGY**
  - — Instantly Reconfigurable Logic
  - — Instantly Reprogrammable Cells
  - — Guaranteed 100% Yields
- **HIGH PERFORMANCE E²CMOS™ TECHNOLOGY**
  - — Low Power: 90mA Typical
  - — High Speed: 12ns Max. Clock to Output Delay
    25ns Max. Setup Time
    30ns Max. Propagation Delay
- **UNPRECENTED FUNCTIONAL DENSITY**
  - — 78 x 64 x 36 FPLA Architecture
  - — 10 Output Logic Macrocells
  - — 8 Buried Logic Macrocells
  - — 20 Input and I/O Logic Macrocells
- **HIGH-LEVEL DESIGN FLEXIBILITY**
  - — Asynchronous or Synchronous Clocking
  - — Separate State Register and Input Clock Pins
  - — Functionally Supersets Existing 24-pin PAL® and IFL™ Devices
- **TTL COMPATIBLE INPUTS AND OUTPUTS**
- **SPACE SAVING 24-PIN, 300-MIL DIP**
- **HIGH SPEED PROGRAMMING ALGORITHM**
- **20-YEAR DATA RETENTION**

DESCRIPTION

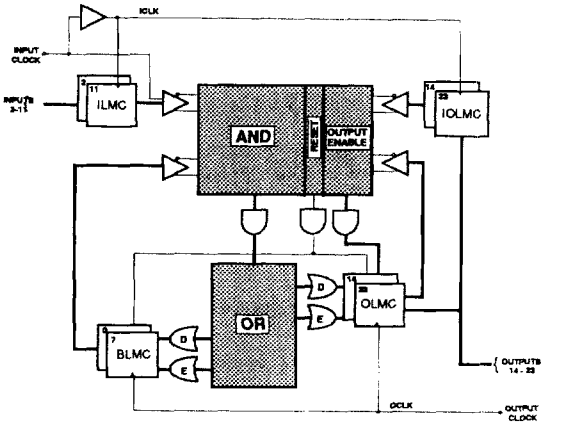
Using a high performance E²CMOS technology, Lattice Semiconductor has produced a next-generation programmable logic device, the GAL6001. Having an FPLA architecture, known for its superior flexibility in state-machine design, the GAL6001 offers the highest degree of functional integration, flexibility, and speed currently available in a 24-pin, 300-mil package.

The GAL6001 has 10 programmable Output Logic Macrocells (OLMC) and 8 programmable Buried Logic Macrocells (BLMC). In addition, there are 10 Input Logic Macrocells (ILMC) and 10 I/O Logic Macrocells (IOLMC). Two clock inputs are provided for independent control of the input and output macrocells.

Advanced features that simplify programming and reduce test time, coupled with E²CMOS reprogrammable cells, enable 100% AC, DC, programmability, and functionality testing of each GAL6001 during manufacture. This allows Lattice to guarantee 100% performance to specifications. In addition, data retention of 20 years and a minimum of 100 erase/write cycles are guaranteed.

Programming is accomplished using standard hardware and software tools. In addition, an Electronic Signature is available for storage of user specified data, and a security cell is provided to protect proprietary designs.

FUNCTIONAL BLOCK DIAGRAM



MACROCELL NAMES

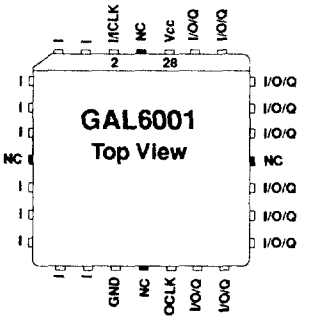
ILMC	INPUT LOGIC MACROCELL
IOLMC	I/O LOGIC MACROCELL
BLMC	BURIED LOGIC MACROCELL
OLMC	OUTPUT LOGIC MACROCELL

PIN NAMES

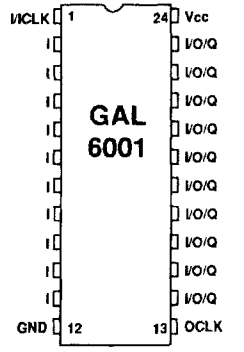
I_0 - I_{10}	INPUT	I/O/Q	BIDIRECTIONAL
ICLK	INPUT CLOCK	V_{CC}	POWER (+5)
OCLK	OUTPUT CLOCK	GND	GROUND

PIN DIAGRAM

Chip Carrier



DIP



LATTICE SEMICONDUCTOR CORP., 5555 N.E. Moore Ct., Hillsboro, Oregon U.S.A.
Tel. (503) 681-0118 or 1-800-FAST GAL; FAX (503) 681-3037

March 1990

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V_{CC} ..... –.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

Tri-state levels are measured 0.5V from steady-state active level.

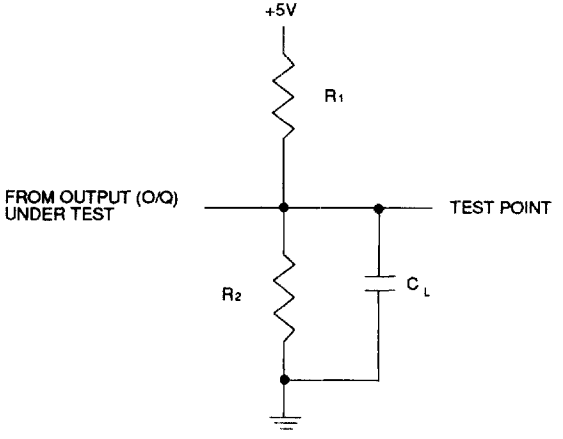
COMMERCIAL		INDUSTRIAL		MILITARY	
R_1	R_2	R_1	R_2	R_1	R_2
300	390	300	390	390	750

AC Test Conditions:

Cond. 1) R_1 per table; C_L = 50pF; R_2 per above table

Cond. 2) Active High R_1 = ∞; Active Low R_1 per table; C_L = 50pF; R_2 per above table

Cond. 3) Active High R_1 = ∞; Active Low R_1 per table; C_L = 5pF; R_2 per above table



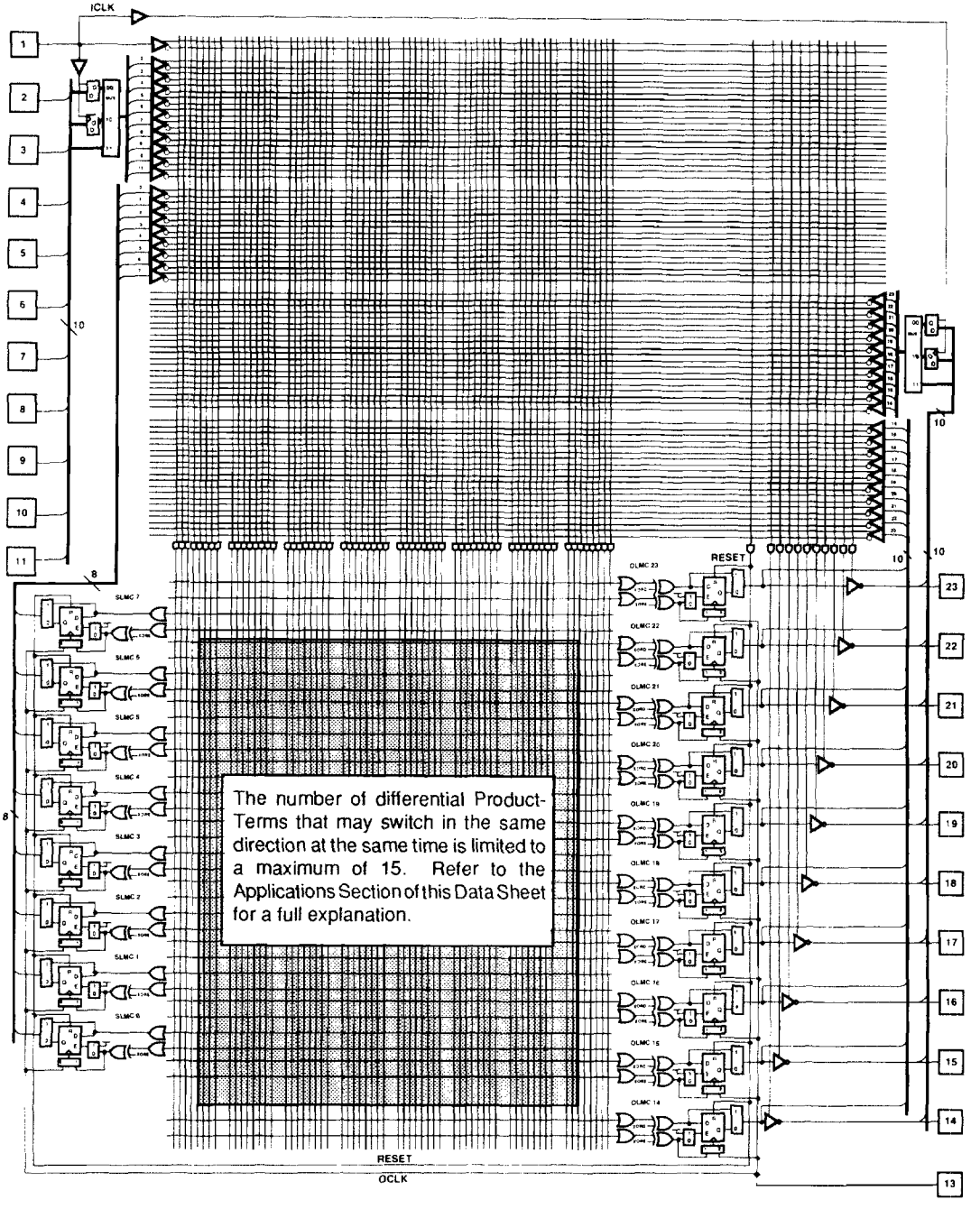
CL INCLUDES JIG AND PROBE TOTAL CAPACITANCE

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	8	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O/Q}$	I/O/Q Capacitance	10	pF	V_{CC} = 5.0V, $V_{I/O/Q}$ = 2.0V

*Guaranteed but not 100% tested.

GAL6001 LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS — GAL6001-30 Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

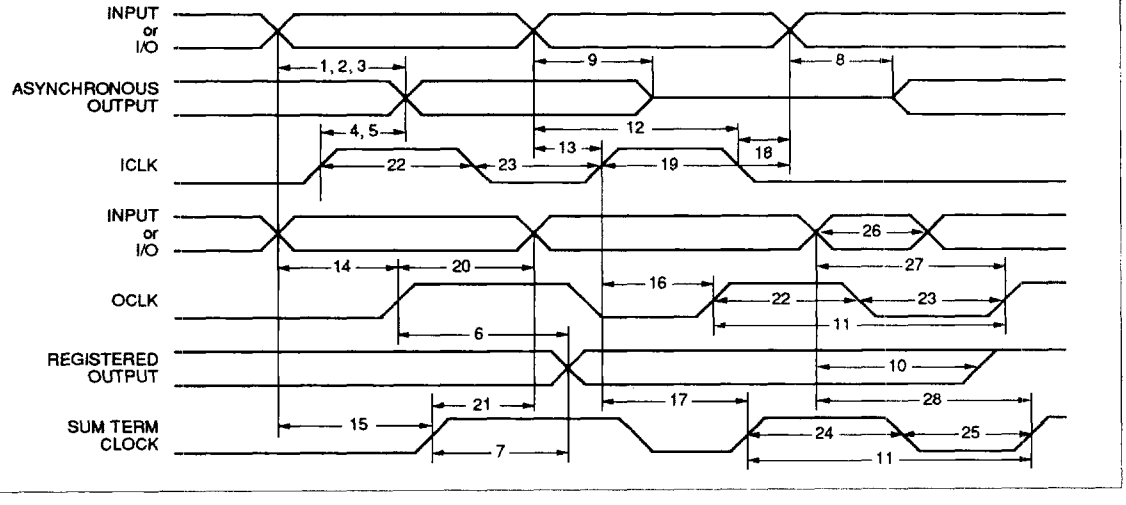
SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = Gnd	–30	—	–130	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	90	150	mA

1) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — GAL6001-30 Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	16	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING WAVEFORMS



SWITCHING CHARACTERISTICS — GAL6001-30 Commercial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I	O	ILMC = Async, OLMC = Combinational	1	—	30	ns
	2	O, Q	O	Feedback → O, OLMC = Combinational	1	—	30	ns
	3	I	O	ILMC = Latch, OLMC = Combinational	1	—	35	ns
t_{co}	4	ICLK ↑	O	ILMC = Reg, OLMC = Combinational	1	—	35	ns
	5	ICLK ↑	O	ILMC = Latch, OLMC = Combinational	1	—	35	ns
	6	OCLK ↑	Q	OLMC = D/E Reg	1	—	12	ns
	7	STCLK ↑	Q	OLMC = DReg STCLK	1	—	35	ns
t_{en}	8	I, I/O	O, Q	Output Enable, Z → O, Q	2	—	25	ns
t_{dis}	9	I, I/O	O, Q	Output Disable, O, Q → Z	3	—	25	ns
t_{res}	10	I, I/O	Q	Register Reset, Q → 1	1	—	35	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL6001-30 Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	11	Clock Frequency, OCLK or STCLK	—	0	27	MHz
t_{su}	12	Input Setup Time before ICLK ↓ , ILMC = Latch	—	2.5	—	ns
	13	Input Setup Time before ICLK ↑ , ILMC = Reg	—	2.5	—	ns
	14	Setup Time, input or feedback, before OCLK ↑ , OLMC = D/E Reg	—	25	—	ns
	15	Setup Time, input or feedback, before STCLK ↑ , OLMC = DReg STCLK	—	7.5	—	ns
	16	Setup Time, ICLK ↑, before OCLK ↑ , OLMC = D/E Reg	—	30	—	ns
	17	Setup Time, ICLK ↑ , before STCLK ↑ , OLMC = DReg STCLK	—	15	—	ns
t_h	18	Hold Time after ICLK ↓ , ILMC = Latch	—	5	—	ns
	19	Hold Time after ICLK ↑, ILMC = Reg	—	5	—	ns
	20	Hold Time after OCLK ↑ , OLMC = D/E Reg	—	-5	—	ns
	21	Hold Time after STCLK ↑, OLMC = DReg STCLK	—	10	—	ns
t_w	22	ICLK or OCLK pulse duration, high	—	10	—	ns
	23	ICLK or OCLK pulse duration, low	—	10	—	ns
	24	STCLK pulse duration, high	—	15	—	ns
	25	STCLK pulse duration, low	—	15	—	ns
	26	Reset pulse duration	—	15	—	ns
t_{rec}	27	Reset to OCLK Recovery Time	—	20	—	ns
	28	Reset to STCLK Recovery Time	—	10	—	ns

ELECTRICAL CHARACTERISTICS — GAL6001-35 Commercial

Over Recommended Operating Conditions (Unless Otherwise Specified)

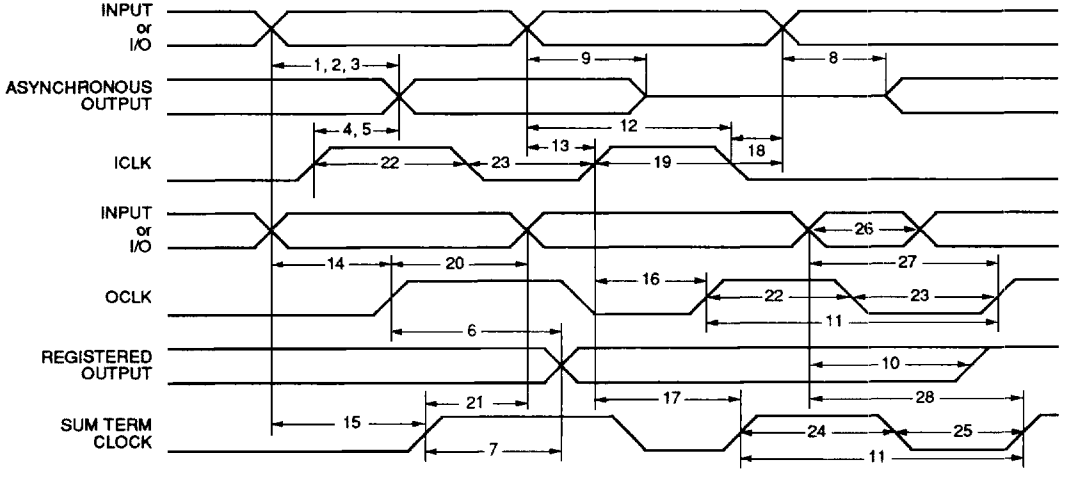
SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage		—	—	0.5	V
V_{OH}	Output High Voltage		2.4	—	—	V
I_{IL}, I_{IH}	Input Leakage Current		—	—	±10	µA
$I_{I/O/Q}$	Bidirectional Pin Leakage Current		—	—	±10	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = Gnd	–30	—	–130	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz	—	90	150	mA

1) One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

DC RECOMMENDED OPERATING CONDITIONS — GAL6001-35 Commercial

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	75	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	Vss – 0.5	0.8	V
V_{IH}	Input High Voltage	2.0	Vcc+1	V
I_{OL}	Low Level Output Current	—	16	mA
I_{OH}	High Level Output Current	—	–3.2	mA

SWITCHING WAVEFORMS



SWITCHING CHARACTERISTICS — GAL6001-35 Commercial

Over Recommended Operating Conditions

PARAMETER	#	FROM	TO	DESCRIPTION	TEST COND.[1]	MIN.	MAX.	UNITS
t_{pd}	1	I	O	ILMC = Async, OLMC = Combinational	1	—	35	ns
	2	O, Q	O	Feedback → O, OLMC = Combinational	1	—	35	ns
	3	I	O	ILMC = Latch, OLMC = Combinational	1	—	40	ns
t_{co}	4	ICLK ↑	O	ILMC = Reg, OLMC = Combinational	1	—	40	ns
	5	ICLK ↑	O	ILMC = Latch, OLMC = Combinational	1	—	40	ns
	6	OCLK ↑	Q	OLMC = D/E Reg	1	—	13.5	ns
	7	STCLK ↑	Q	OLMC = DReg STCLK	1	—	40	ns
t_{en}	8	I, I/O	O, Q	Output Enable, Z → O, Q	2	—	30	ns
t_{dis}	9	I, I/O	O, Q	Output Disable, O, Q → Z	3	—	30	ns
t_{res}	10	I, I/O	Q	Register Reset, Q → 1	1	—	35	ns

1) Refer to **Switching Test Conditions** section.

AC RECOMMENDED OPERATING CONDITIONS — GAL6001-35 Commercial

PARAMETER	#	DESCRIPTION	TEST COND.	MIN.	MAX.	UNITS
f_{clk}	11	Clock Frequency, OCLK or STCLK	—	0	22.9	MHz
t_{su}	12	Input Setup Time before ICLK ↓ , ILMC = Latch	—	3.5	—	ns
	13	Input Setup Time before ICLK ↑ , ILMC = Reg	—	3.5	—	ns
	14	Setup Time, input or feedback, before OCLK ↑ , OLMC = D/E Reg	—	30	—	ns
	15	Setup Time, input or feedback, before STCLK ↑ , OLMC = DReg STCLK	—	10	—	ns
	16	Setup Time, ICLK ↑, before OCLK ↑ , OLMC = D/E Reg	—	35	—	ns
	17	Setup Time, ICLK ↑ , before STCLK ↑ , OLMC = DReg STCLK	—	17	—	ns
t_h	18	Hold Time after ICLK ↓ , ILMC = Latch	—	5	—	ns
	19	Hold Time after ICLK ↑, ILMC = Reg	—	5	—	ns
	20	Hold Time after OCLK ↑ , OLMC = D/E Reg	—	-5	—	ns
	21	Hold Time after STCLK ↑, OLMC = DReg STCLK	—	12.5	—	ns
t_w	22	ICLK or OCLK pulse duration, high	—	10	—	ns
	23	ICLK or OCLK pulse duration, low	—	10	—	ns
	24	STCLK pulse duration, high	—	15	—	ns
	25	STCLK pulse duration, low	—	15	—	ns
	26	Reset pulse duration	—	15	—	ns
t_{rec}	27	Reset to OCLK Recovery Time	—	20	—	ns
	28	Reset to STCLK Recovery Time	—	10	—	ns

INPUT LOGIC MACROCELL (ILMC) AND I/O LOGIC MACROCELL (IOLMC)

The GAL6001 features two configurable input sections. The ILMC section corresponds to the dedicated input pins (2-11) and the IOLMC to the I/O pins (14-23). Each input section is configurable as a block for asynchronous, latched, or registered inputs. Pin 1 (ICLK) is used as an enable input for latched macrocells or as a clock input for registered macrocells. Configurable input blocks provide systems designers with unparalled design flexibility. With the GAL6001, external registers and latches are not necessary.

Both the ILMC and the IOLMC are block configurable. However, the ILMC can be configured independently of the IOLMC. The three valid macrocell configurations are shown in the macrocell equivalent diagrams on the following pages.

OUTPUT LOGIC MACROCELL (OLMC) AND BURIED LOGIC MACROCELL (BLMC)

The outputs of the OR array feed two groups of macrocells. One group of eight macrocells is buried; its outputs feed back directly into the AND array rather than to device pins. These cells are called the Buried Logic Macrocells (BLMC), and are useful for building state machines. The second group of macrocells consists of 10 cells whose outputs, in addition to feeding back into the AND array, are available at the device pins. Cells in this group are known as Output Logic Macrocells (OLMC).

The Output and Buried Logic Macrocells are configurable on a macrocell by macrocell basis. Buried and Output Logic Macrocells may be set to one of three configurations: combinational, "D-type register with sum term (asynchronous) clock", or "D/E-type register." Output macrocells always have I/O capability, with directional control provided by the 10 output enable (OE) product terms. Additionally, the polarity of each OLMC output is selected through the "D" XOR. Polarity selection is available for BLMCs, since both the true and complemented forms of their outputs are available in the AND array. Polarity of all "E" sum terms is selected through the "E" XOR.

When the macrocell is configured as a "D/E type registered", the register is clocked from the common OCLK and the register clock enable input is controlled by the associated "E" sum term. This configuration is useful for building counters and state-machines with state hold functions.

When the macrocell is configured as a "D type register with a sum term clock", the register is always enabled and its "E" sum term is routed directly to the clock input. This permits asynchronous programmable clocking, selected on a register-by-register basis.

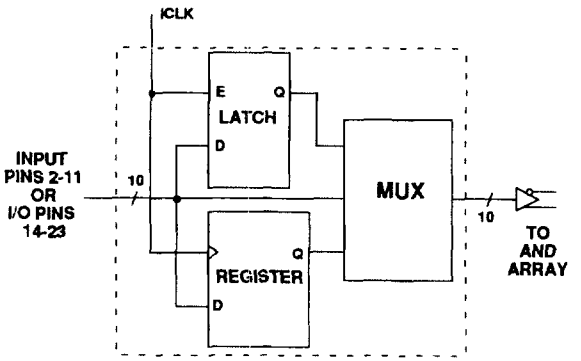
Registers in both the Output and Buried Logic Macrocells feature a common RESET product term. This active high product term allows the registers to be asynchronously reset. Registers are reset to a logic zero. If connected to an ouput pin, a logic one will occur because of the inverting output buffer.

There are two possible feedback paths from each OLMC. The first path is directly from the OLMC (this feedback is before the output buffer and always present). When the OLMC is used as an output, the second feedback path is through the IOLMC. With this dual feedback arrangement, the OLMC can be permanently buried (the associated OLMC pin is an input), or dynamically buried with the use of the output enable product term.

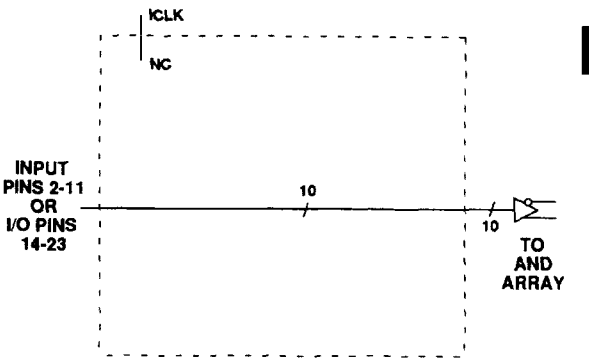
The D/E registers used in this device offer the designer the ultimate in flexibility and utility. The D/E register architecture can emulate RS-, JK-, and T-type registers with the same efficiency as a dedicated RS-, JK-, or T-register.

The three macrocell configurations are shown in the macrocell equivalent diagrams on the following pages.

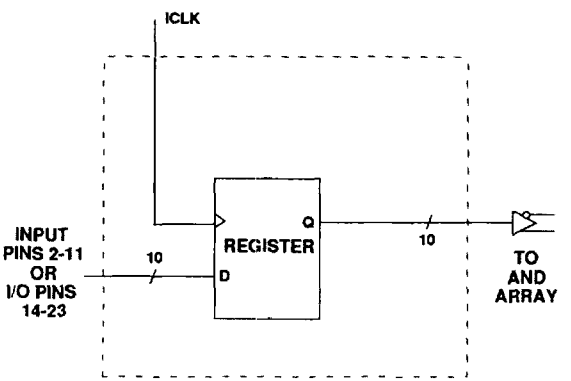
ILMC AND IOLMC CONFIGURATIONS



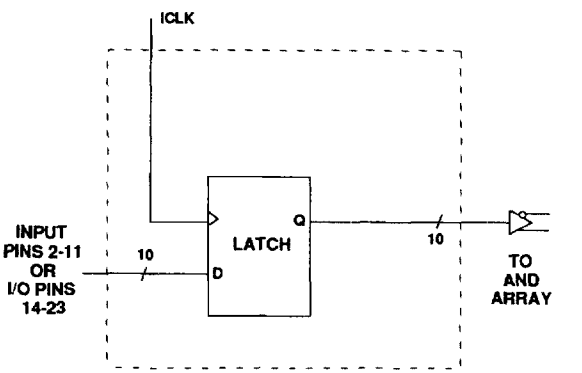
ILMC/IOLMC
Generic Block Diagram



Asynchronous Input

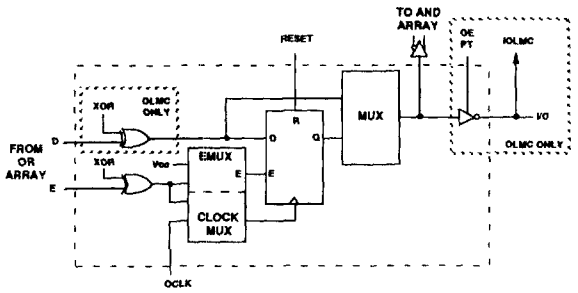


Registered Input

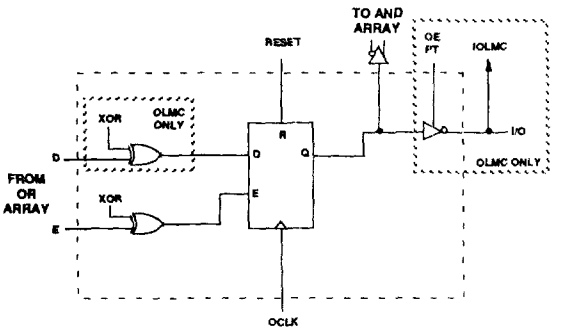


Latched Input

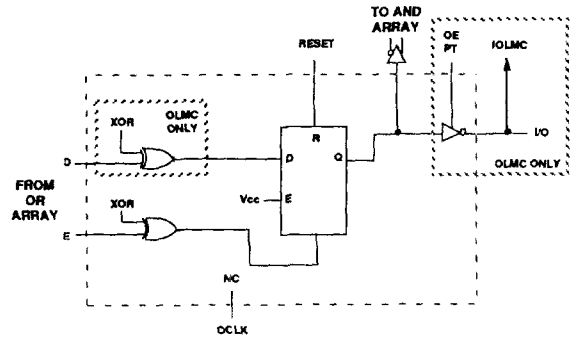
OLMC AND BLMC CONFIGURATIONS



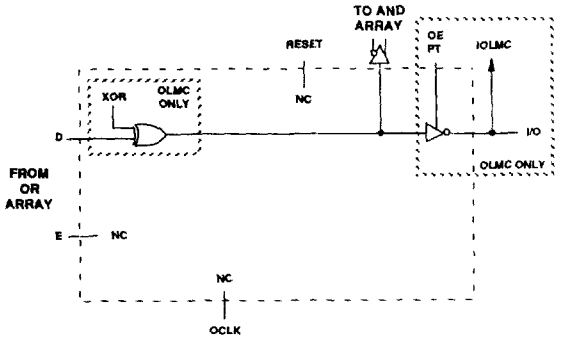
OLMC/BLMC
Generic Block Diagram



D/E Type Registered



D Type Register with Sum Term Asynchronous Clock



Combinational

ARRAY DESCRIPTION

The GAL6001 contains two E^2 reprogrammable arrays. The first is an AND array and the second is an OR array. These arrays are described in detail below.

AND ARRAY

The AND array is organized as 78 inputs by 75 product term outputs. The 10 ILMCs, 10 IOLMCs, 8 BLMC feedbacks, 10 OLMC feedbacks, and ICLK comprise the 39 inputs to this array (each available in true and complemented forms). 64 product terms serve as inputs to the OR array. There is a RESET PT; it generates the RESET signal described in the earlier discussion of Output and Buried Logic Macrocells. There are 10 output enables, thus allowing device pins 14-23 to be bi-directional or tri-state.

OR ARRAY

The OR array is organized as 64 inputs by 36 sum term outputs. 64 product terms from the AND array serve as the inputs to the OR array. Of the 36 sum term outputs, 18 are data ("D") terms and 18 are enable/clock ("E") terms. These terms feed into the 10 OLMCs and 8 BLMCs, one "D" term and one "E" term to each.

The programmable OR array offers unparalleled versatility in product term usage. This programmability allows from 1 to 64 product terms to be connected to a single sum term. A programmable OR array is more flexible than a fixed, shared, or variable product term architecture.

ELECTRONIC SIGNATURE

An electronic signature (ES) is provided with every GAL6001 device. It contains 72 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The ES is included in checksum calculations. Changing the ES will alter the checksum.

SECURITY CELL

A security cell is provided with every GAL6001 device as a deterrent to unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the AND and OR array. This cell can be erased only during a bulk erase cycle, so the original configuration can never be examined once this cell is programmed. The Electronic Signature is always available to the user, regardless of the state of this control cell.

BULK ERASE

Before writing a new pattern into a previously programmed part, the old pattern must first be erased. This erasure is done automatically by the programming hardware as part of the programming cycle and takes only 50 milliseconds.

REGISTER PRELOAD

2

When testing state machine designs, all possible states and state transitions must be verified, not just those required during normal operations. This is because in system operation, certain events may occur that cause the logic to assume an illegal state: power-up, brown out, line voltage glitches, etc. To test a design for proper treatment of these conditions, a method must be provided to break the feedback paths and force any desired state (i.e., illegal) into the registers. Then the machine can be sequenced and the outputs tested for correct next state generation.

All of the registers in the GAL6001 can be preloaded, including the ILMC, IOLMC, OLMC, and BLMC registers. In addition, the contents of the state and output registers can be examined in a special diagnostics mode. Programming hardware takes care of all preload timing and voltage requirements.

LATCH-UP PROTECTION

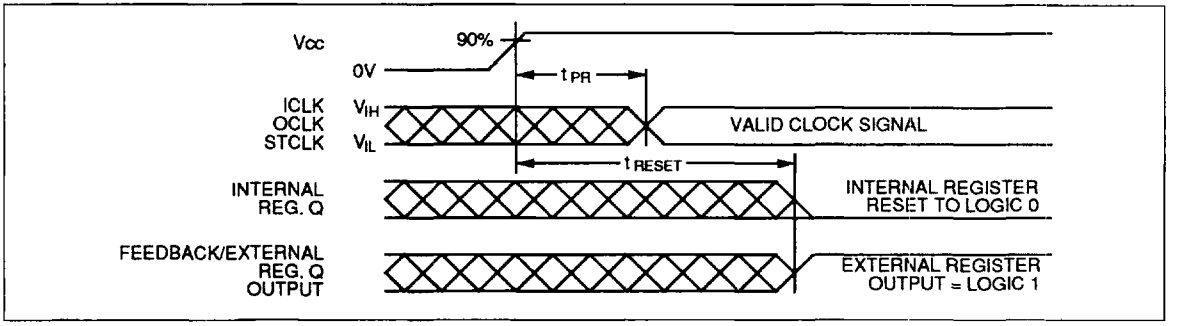
GAL6001 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pull-up instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

INPUT BUFFERS

GAL devices are designed with TTL level compatible input buffers. These buffers, with their characteristically high impedance, load driving logic much less than traditional bipolar devices. This allows for a greater fan out from the driving logic.

GAL6001 devices do not possess active pull-ups within their input structures. As a result, Lattice recommends that all unused inputs and tri-stated I/O pins be connected to another active input, V_{CC}, or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

POWER-UP RESET



Circuitry within the GAL6001 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (t_{RESET}, 45µs). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up.

The timing diagram for power-up is shown above. Because of the asynchronous nature of system power-up, some conditions must be met to guarantee a valid power-up reset of the GAL6001. First, the Vcc rise must be monotonic. Second, the clock inputs must become a proper TTL level within the specified time (t_{PR}, 100µs). The registers will reset within a maximum of t_{RESET} time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met.

DIFFERENTIAL PRODUCT TERM SWITCHING (DPTS) APPLICATIONS

The number of Differential Product Term Switching (DPTS) for a given design is calculated by subtracting the total number of product terms that are switching from a Logical HI to a Logical LO from those switching from a Logical LO to a Logical HI within a 5ns period. After subtracting take the absolute value.

$$DPTS = \left| (\text{P-Terms})_{LH} - (\text{P-Terms})_{HL} \right|$$

DPTS restricts the number of product terms that can be switched simultaneously - there is no limit on the number of product terms that can be used.

A software utility is available from Lattice Applications Engineering that will perform this calculation on any GAL6001 JEDEC file. This program, DPTS, and additional information may be obtained from your local Lattice representative or by contacting Lattice Applications Engineering (Tel: 503-681-0118 or 800-FASTGAL; FAX: 681-3037).