Preliminary Data Sheet
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microelectronics group

Lucent Technologies
Bell Labs Innovations

LU1X54
QUAD Transceiver for 10Base-T

Features

- Compatible with *IEEE* * 802.3 10Base-T standard for twisted-pair cable
- Autopolarity detection and correction
- Adjustable squelch level for extended line length capability (two levels)
- Interfaces with *IEEE* 802.3u media independent interfaces (MII) or a 7-pin 10 Mbits/s serial interface
- Bused mode:
  — Buses all four channels into a single 10 Mbits serial port
  — Separate TX_EN, RX_EN, CRS, and COL pins for each channel
  — Drivers on bused signals can drive up to eight LU1X54s (32 ports)
- On-chip filtering eliminates the need for external filters
- Autonegotiation (*IEEE* 802.3u, clause 28):
  — Fast link pulse (FLP) burst generator
  — Arbitration function
- Supports the station management protocol and frame format (clause 22):
  — Basic and extended registers
  — Supports next-page function
  — Operates up to 10 MHz
  — Accepts preamble suppression
  — Maskable status interrupts
- Supports the following management functions via pins if station management is unavailable:
  — Full duplex
  — No link pulse mode
  — Carrier sense select
  — Autonegotiation
  — 10 Mbits/s repeater reference select
- Single 20 MHz crystal input or 20 MHz clock input
- Supports half- and full-duplex operations
- Provides five status signals: receive activity, transmit activity, full duplex, collision/jabber, and link integrity
- Optional LED pulse stretching
- Per-channel powerdown mode
- Loopback mode
- Internal pull-up or pull-down resistors to set default powerup mode
- 0.35 µm low-power CMOS technology
- 208-pin SQFP
- Single 5 V power supply

* *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Note: Advisories are issued as needed to update product information. When using this data sheet for design purposes, please contact your Lucent Technologies Microelectronics Group Account Manager to obtain the latest advisory on this product.

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Table of Contents

Contents

Page

Features
Description 4
Configuration 4
Bused Mode 4
Clocking 4
Functional Block Diagrams 5
Application Diagram 7
Bused Mode Block Diagram 8
Pin Information 9
Preliminary Pin Diagram for Normal Mode 9
Preliminary Pin Diagram for Bused Mode (Security Not Selected) 10
Preliminary Pin Diagram for Bused Mode (Security Selected) 11
Pin Maps 12
Pin Descriptions 13
MII Station Management 23
Basic Operations 23
MII Management Frames 23
Management Registers (MR) 24
Unmanaged Operations 34
Mode Select 34
Absolute Maximum Ratings (T_A = 25 °C) 35
Electrical Characteristics 35
Timing Characteristics (Preliminary) 36
Outline Diagram 42
208-Pin SQFP 42
Ordering Information 43
Revison List 43

Table of Contents (continued)

Tables

Page

Table 1. Crystal Specifications 4
Table 2. LU1X54 Pin Maps 12
Table 3. MII/Serial Interface Pins in Normal Mode (Four Separate MII/Serial Ports) 13
Table 4. Serial Interface Pins in Bused Mode (Security Not Selected) 15
Table 5. Serial Interface Pins in Bused Mode (Security Selected) 16
Table 6. MII Management Pins 17
Table 7. Twisted-Pair (TP) Interface Pins 17
Table 8. Miscellaneous Pins 18
Table 9. MII Management Frame Format 23
Table 10. MII Management Frames—Field Descriptions 23
Table 11. MII Management Registers (MR) 24
Table 12. MR0—Control Register Bit Descriptions 25
Table 13. MR1—Status Register Bit Descriptions 26
Table 14. MR2, 3—PHY Identifier Registers (1 and 2) Bit Descriptions 27
Table 15. MR4—Autonegotiation Advertisement Register Bit Descriptions 27
Table 16. MR5—Autonegotiation Link Partner (LP) Ability Register (Base Page) Bit Descriptions 28
Table 17. MR5—Autonegotiation Link Partner (LP) Ability Register (Next Page) Bit Descriptions 28
Table 18. MR6—Autonegotiation Expansion Register Bit Descriptions 29
Table 19. MR7—Next-Page Transmit Register Bit Descriptions 29
Table 20. MR28—Device-Specific Register 1 (Status Register) Bit Descriptions 30
Table 21. MR29—Device-Specific Register 2 Bit Descriptions 31
Table 22. MR30—Device-Specific Register 3 (Control) Bit Descriptions 32
Table 23. MR31—Device-Specific Register 4 (Quick Status) Bit Descriptions 33
Table 24. Output Pins 34
Table 25. LU1X54 Modes 34
Table 26. Absolute Maximum Ratings 35
Table 27. Operating Conditions 35
Table 28. dc Characteristics 35
Table 29. MII Management Interface Timing (100 pF Load) 36
Table 30. MII Data Timing 37
Table 31. Serial 10 Mbits/s Timing for TPIN±, CRS, and RX_CLK 38
Table 32. Serial 10 Mbits/s Timing for TX_EN, TPOUT±, CRS, and RX_CLK 38
Table 33. Serial 10 Mbits/s Timing for TX_EN, TPIN±, and COL 39
Table 34. Serial 10 Mbits/s Timing for RX_CLK, CRS, RXD, TX_CLK, TX_EN, and TXD 40
Table 35. Serial 10 Mbits/s Timing for RX_CLK and TX_CLK 41

Figures

Page

Figure 1. LU1X54 Device Overview 5
Figure 2. LU1X54 Single-Channel Detail Block Diagram 6
Figure 3. Typical Single-Channel Twisted-Pair (TP) Interface 7
Figure 4. LU1X54 in Bused Mode 8
Figure 5. Preliminary Pinout for Normal Mode 9
Figure 6. Preliminary Pinout for Bused Mode (Security Not Selected) 10
Figure 7. Preliminary Pinout for Bused Mode (Security Selected) 11
Figure 8. MDIO Input Timing 36
Figure 9. MDIO Output Timing 36
Figure 10. MDIO During TA (Turnaround) of a Read Transaction 36
Figure 11. MII Data Timing Requirements 37
Figure 12. Serial 10 Mbits/s Timing for TPIN±, CRS, and RX_CLK 38
Figure 13. Serial 10 Mbits/s Timing for TX_EN, TPOUT±, CRS, and RX_CLK 38
Figure 14. Serial 10 Mbits/s Timing for TX_EN, TPIN±, and COL 39
Figure 15. Serial 10 Mbits/s Timing for RX_CLK, CRS, RXD, TX_CLK, TX_EN, and TXD 40
Figure 16. Serial 10 Mbits/s Timing Diagram for RX_CLK and TX_CLK 41

Description

Configuration

The LU1X54 is a four-channel, single-chip complete transceiver designed specifically for 10Base-T repeaters and switches.

Each channel implements the 10Base-T transceiver function of *IEEE* 802.3. This device supports operations over two pairs of category 3 unshielded twisted-pair (UTP) cable.

Bused Mode

The LU1X54 has been designed for operation in two basic system interface modes of operation:

- **Separate MII/Serial Ports.** The separate mode provides four independent RJ-45 to MII/serial ports and is similar to having four independent 10 transceivers.
- **Bused Mode.** This mode is designed specifically for repeater applications to save pins. In bused mode, data from all four channels will be internally bused to a single system interface (port B).

The signals RX_CLK, RXD, TX_CLK, and TXD (all from channels A, B, C, and D) are internally bused together and connected to port B.

The SECURITY_MODE_SELECT is used to select the security feature in bused mode. The security feature is enabled by using the SECURITY pins. Figure 4 shows a block diagram of the bused mode of operation. In this mode, separate pins are used for CRS, RX_EN, TX_EN, and COL.

Figure 1 gives a functional overview of the LU1X54 while Figure 2 details its single-channel functions.

The application drawing in Figure 3 shows how the LU1X54 single channel interfaces to the twisted pair (TP).

Clocking

The LU1X54 requires a 20 MHz clock. This clock can be supplied with an external clock oscillator or an external crystal using the on-chip oscillator.

The LU1X54 will automatically detect if a 20 MHz clock is supplied, or if a crystal is being used to generate the 20 MHz clock.

The crystal specifications are listed in Table 1, and the crystal circuit is shown in Figure 3.

Table 1. Crystal Specifications

Parameter	Requirement
Type	Quartz Fundamental Mode
Frequency	20 MHz
Stability	±25 ppm, 0—70 °C
Shunt Capacitor	7 pF
Load Capacitor	20 pF
Series Resistance	<30 Ω

Description (continued)

Functional Block Diagrams

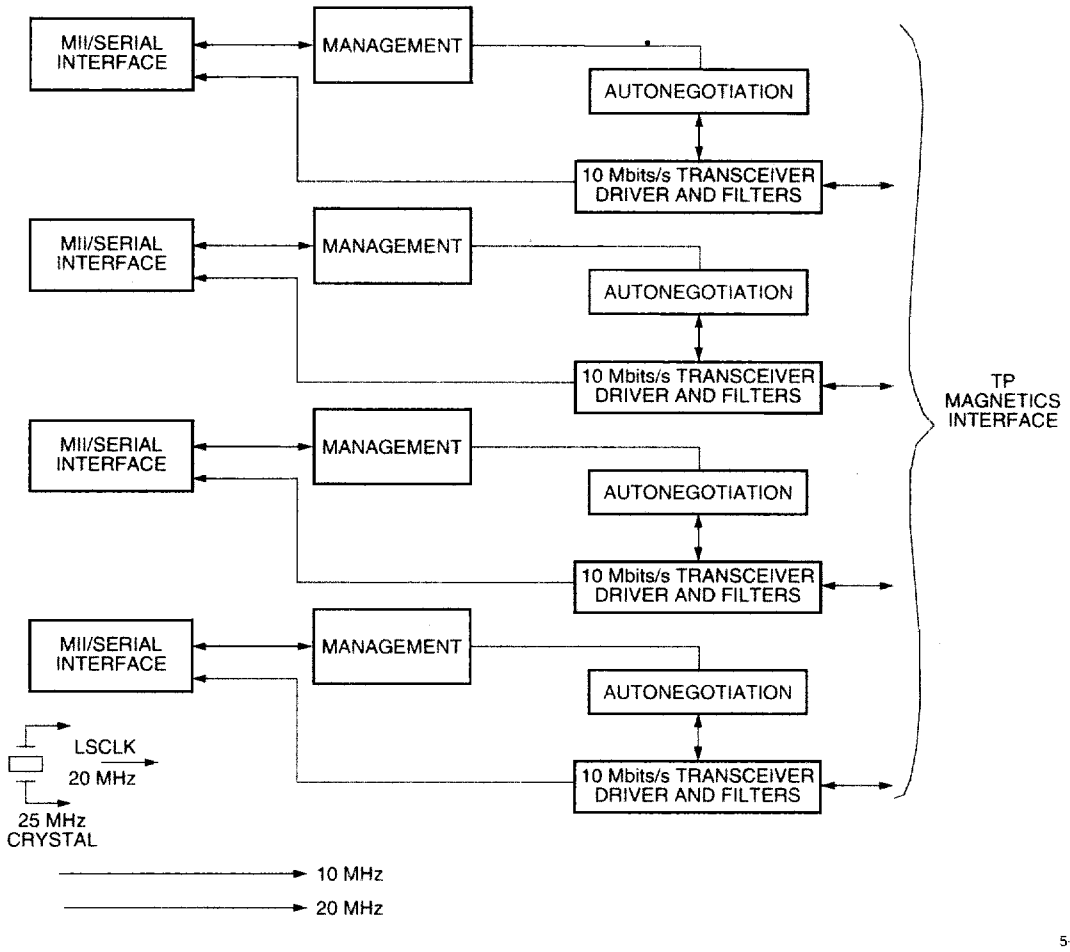


Figure 1. LU1X54 Device Overview

Description (continued)

Functional Block Diagrams (continued)

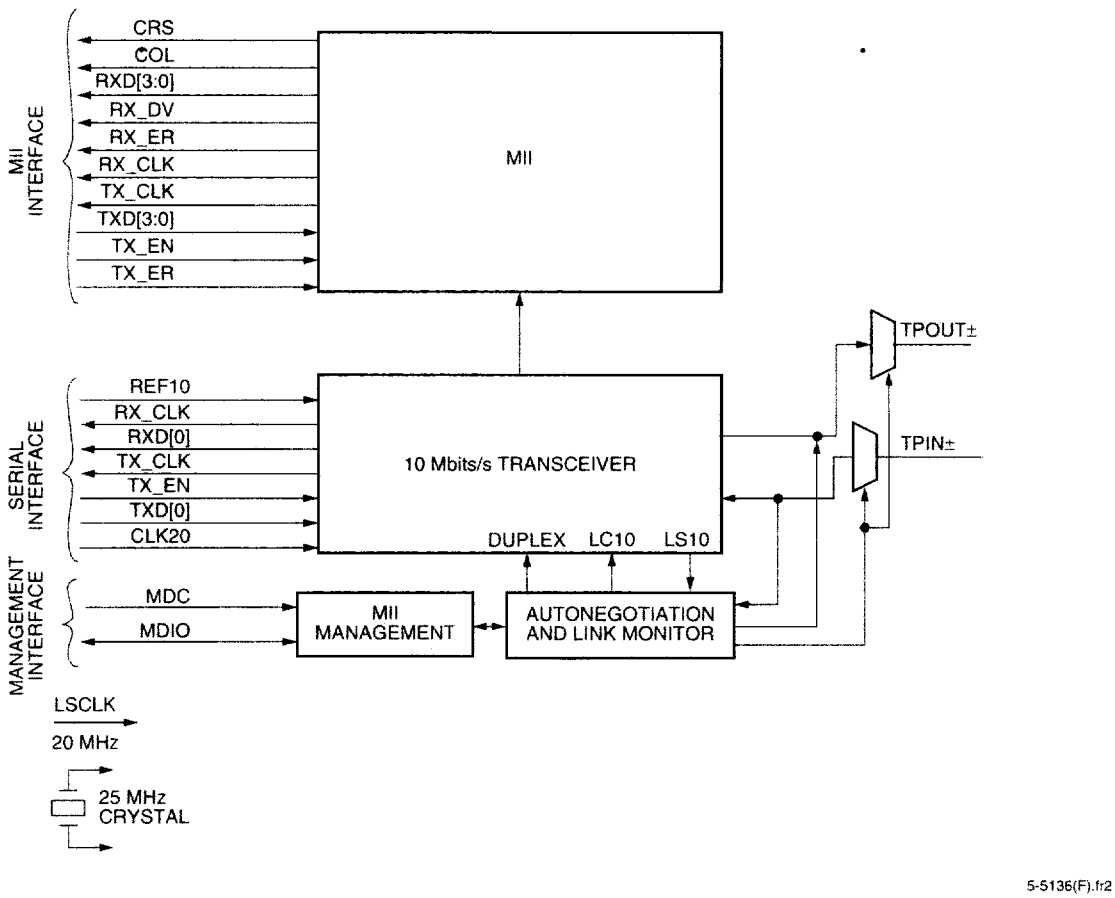
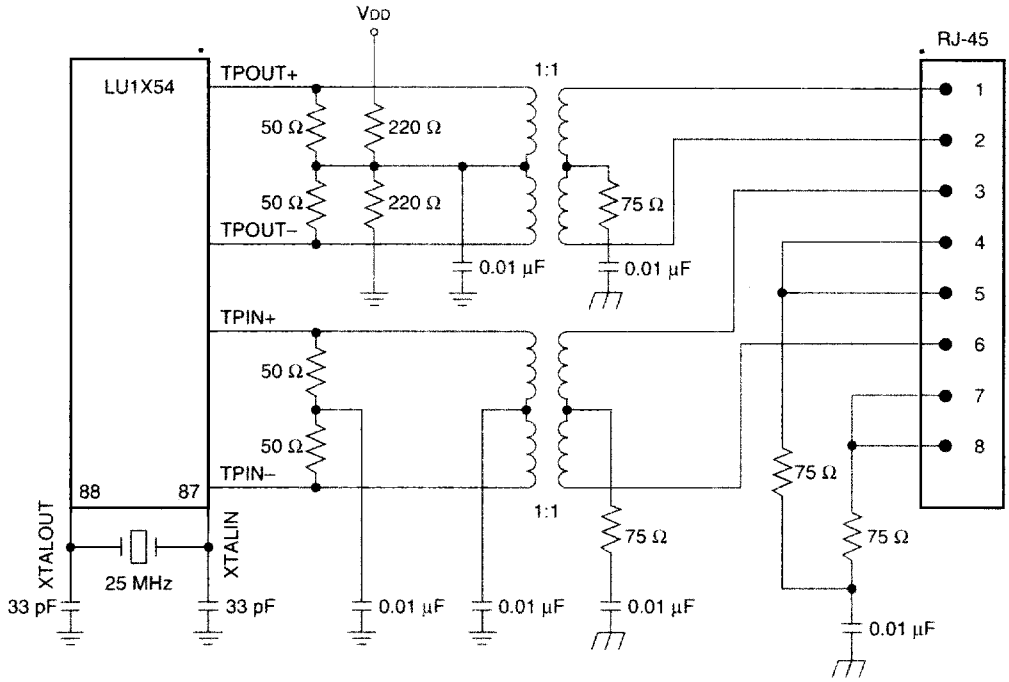


Figure 2. LU1X54 Single-Channel Detail Block Diagram

Description (continued)

Application Diagram

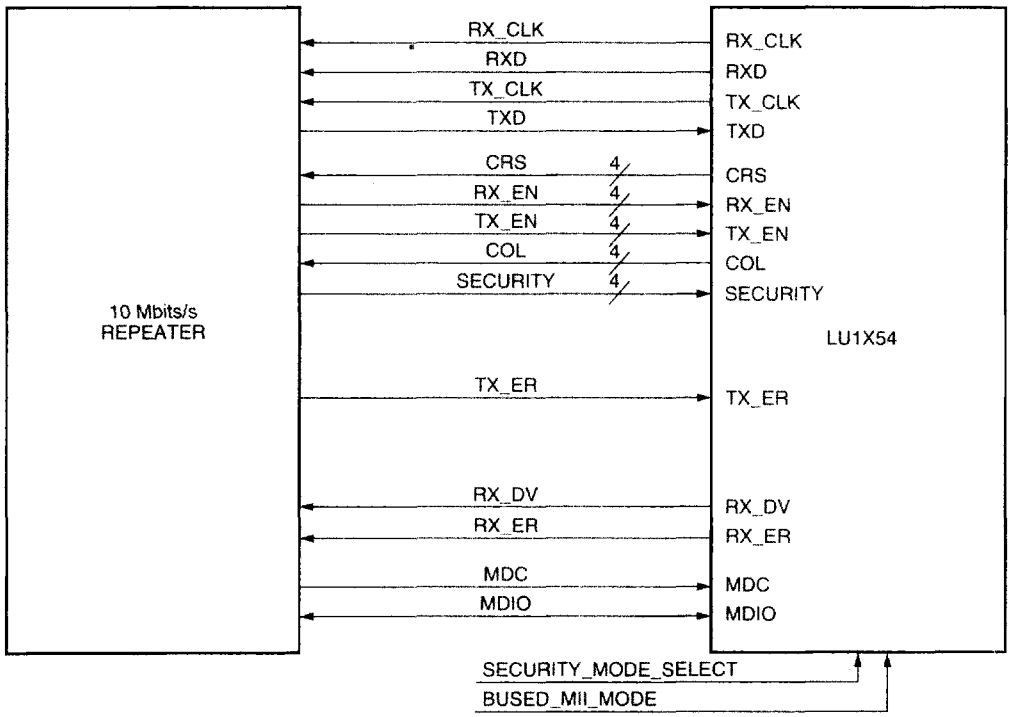


5-5433(F).br2

Figure 3. Typical Single-Channel Twisted-Pair (TP) Interface

Description (continued)

Bused Mode Block Diagram

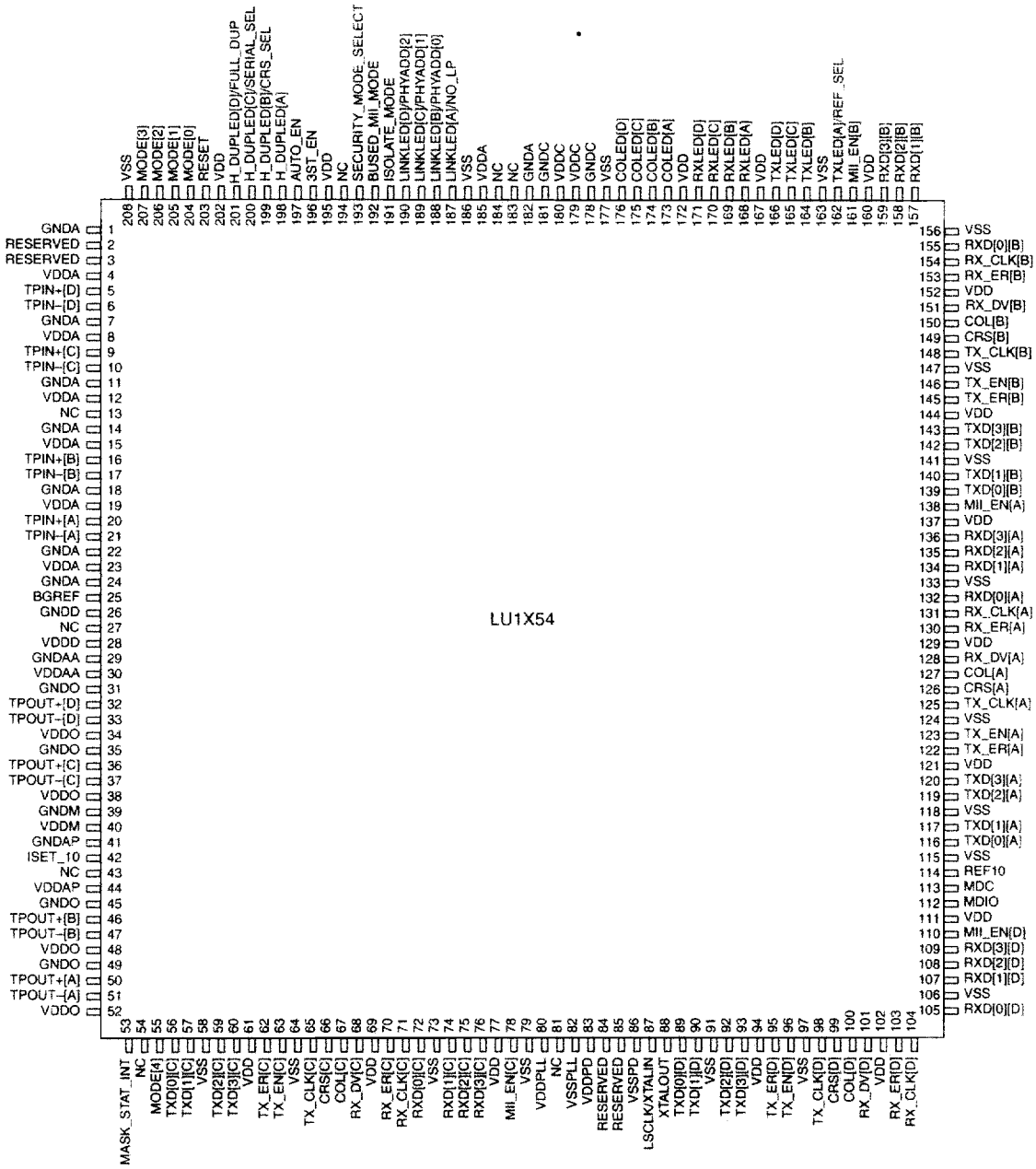


5-5599.dr1

Figure 4. LU1X54 in Bused Mode

Pin Information

Preliminary Pin Diagram for Normal Mode



5-6328(F) r2

Figure 5. Preliminary Pinout for Normal Mode

Pin Information (continued)

Preliminary Pin Diagram for Bused Mode (Security Not Selected)

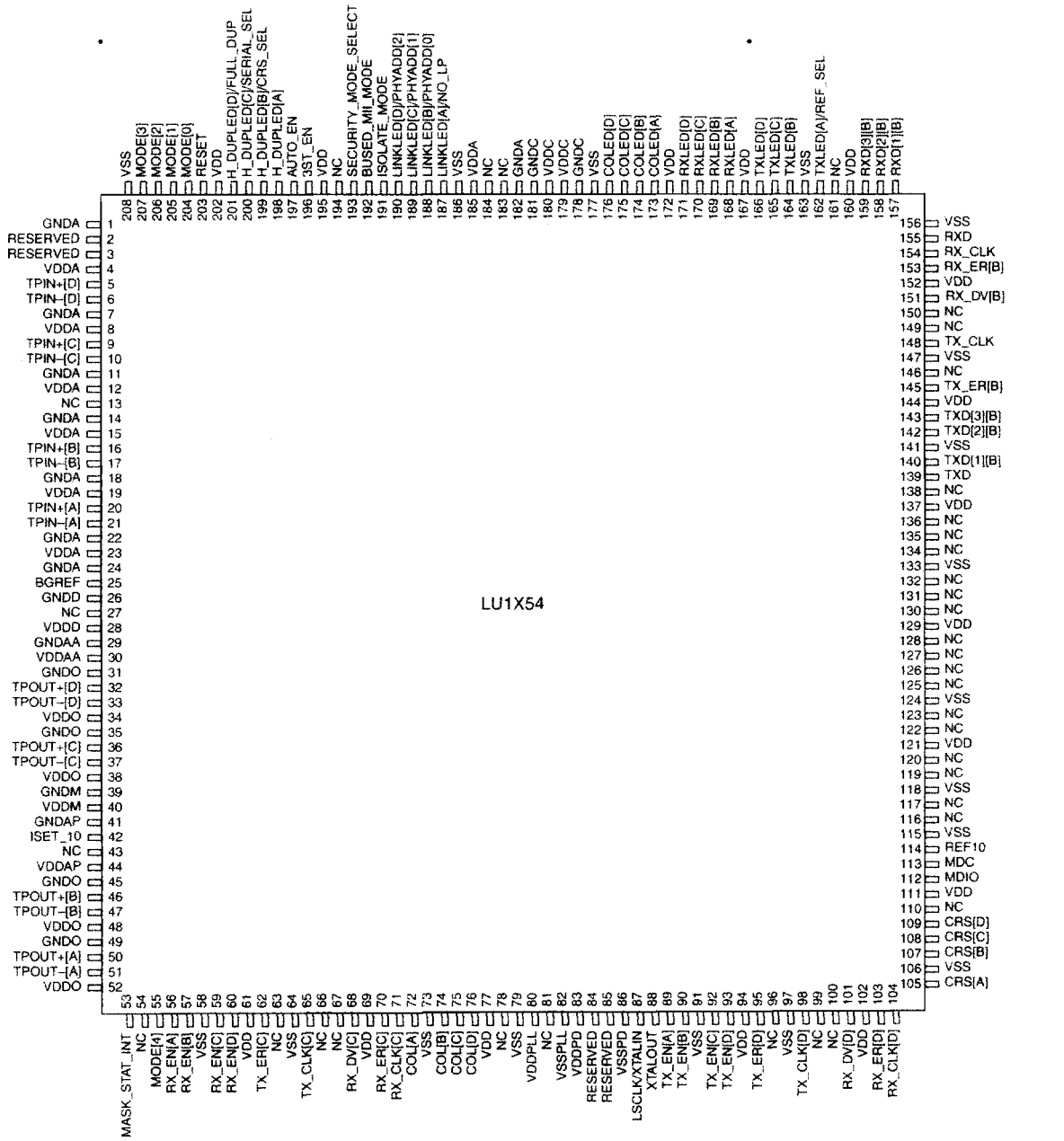
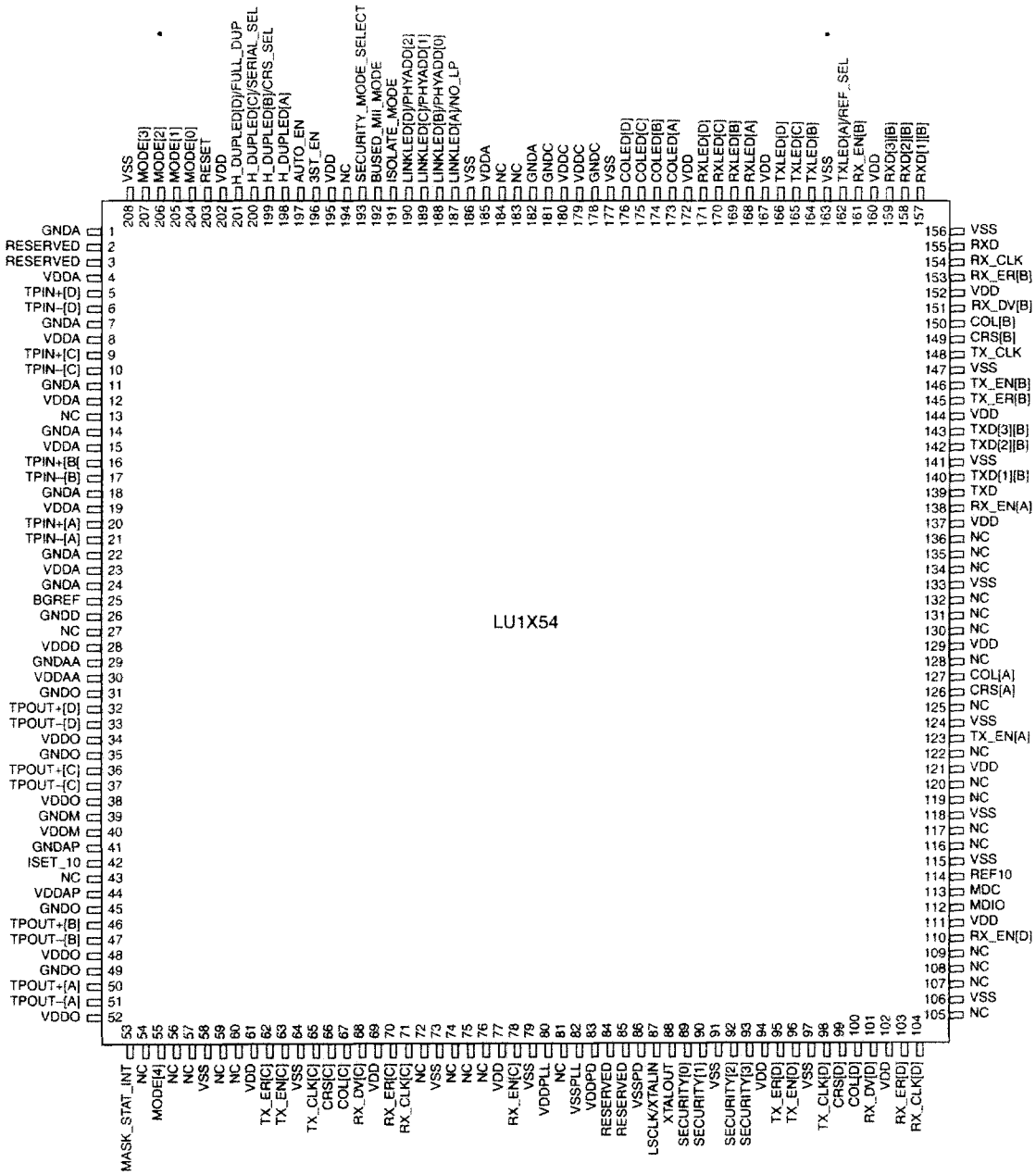


Figure 6. Preliminary Pinout for Bused Mode (Security Not Selected)

Pin Information (continued)

Preliminary Pin Diagram for Bused Mode (Security Selected)



5-6329(F).r3

Figure 7. Preliminary Pinout for Bused Mode (Security Selected)

Pin Information (continued)

Pin Maps

Table 2. LU1X54 Pin Maps

Normal Mode Pins	Bused Mode Pin Functions (Security Not Selected)	Bused Mode Pin Functions (Security Selected)
RXD[3:0][D]	CRS[D:A]	Not used
CRS[D:A]	CRS[D:A]	Not used
TXD[3:0][C]	RX_EN[D:A]	Not use
MII_EN[D:A]	Not used	RX_EN[D:A
TXD[3:0][D]	TX_EN[D:A]	SECURIT
TX_EN[D:A]	Not used	TX_EN[D:A]
RXD[3:0][C]	COL[D:A]	Not used
COL[D:A]	Not used	COL[D:A]
SECURITY_MODE_SELECT	SECURITY_MODE_SELECT	SECURITY_MODE_SELEC
BUSED_MII_MODE	BUSED_MII_MODE	BUSED_MII_MODE
TX_CLK[A]	Not used	Not used
TX_CLK[B]	TX_CLK	TX_CLK
RX_CLK[B]	RX_CLK	RX_CLK
RX_CLK[A]	Not used	Not used
RXD[0][B]	RXD	RXD
RXD[3:0][A]	Not used	Not used
RX_DV[A]	Not used	Not used
RX_ER[A]	Not used	Not used
TXD[0][B]	TXD	TXD
TXD[3:0][A]	Not used	Not used
TX_ER[A]	Not used	Not used

Pin Information (continued)

Pin Descriptions

This section describes the LU1X54 signal pins. Note that any register bit referenced includes the register number and bit position. For example, register bit [29.8] is register 29, bit 8.

Table 3. MII/Serial Interface Pins in Normal Mode (Four Separate MII/Serial Ports)

Pin	Signal	Type	Description
100 67 150 127	COL[D:A]	O	**Collision Detect.** This signal signifies in half-duplex mode that a collision has occurred on the network. COL is asserted high whenever there is transmit and receive activity on the UTP media. COL is the logical AND of TX_EN and receive activity, and is an asynchronous output. When SERIAL_SEL is high, this signal indicates the jabber timer has expired.
99 66 149 126	CRS[D:A]	O	**Carrier Sense.** When CRS_SEL is low, this signal is asserted high when either the transmit or receive medium is nonidle. This signal remains asserted throughout a collision condition. When CRS_SEL is high, CRS is asserted on receive activity only. CRS_SEL is set via the MII management interface or the CRS_SEL pin.
104 71 154 131	RX_CLK[D:A]	O	**Receive Clock.** 2.5 MHz clock output in nibble mode, 10 MHz in serial mode. RX_CLK has a worst-case 45/55 duty cycle. RX_CLK provides the timing reference for the transfer of RX_DV, RXD, and RX_ER signals.
109, 76 159, 136 108, 75 158, 135 107, 74 157, 134 105, 72 155, 132	RXD[3:0][D:A]	O	**Receive Data.** 4-bit parallel data outputs that are synchronous to RX_CLK. When SERIAL_SEL is active-high, RXD[0] is used for data output and RXD[3:1] are 3-stated.
101 68 151 128	RX_DV[D:A]	O	**Receive Data Valid.** When this pin is high, it indicates the LU1X54 is recovering and decoding valid nibbles on RXD[3:0], and the data is synchronous with RX_CLK. RX_DV is synchronous with RX_CLK. This pin is not used in serial mode.
103 70 153 130	RX_ER[D:A]	O	**Receive Error.** When high, RX_ER indicates the LU1X54 has detected a coding error in the frame presently being transferred. RX_ER is synchronous with RX_CLK. When SERIAL_SEL is active-high, this pin is ignored.
98 65 148 125	TX_CLK[D:A]	O	**Transmit Clock.** 2.5 MHz clock output in MII mode, 10 MHz output in serial mode. TX_CLK provides timing reference for the transfer of the TX_EN, TXD, and TX_ER signals sampled on the rising edge of TX_CLK.

Pin Information (continued)

Pin Descriptions (continued)

Table 3. MII/Serial Interface Pins in Normal Mode (Four Separate MII Ports) (continued)

Pin	Signal	Type	Description
93, 60 143, 120 92, 59 142, 119 90, 57 140, 117 89, 56 139, 116	TXD[3:0][D:A]	I	**Transmit Data.** 4-bit parallel input synchronous with TX_CLK. When SERIAL_SEL is active-high, only TXD[0][D:A] are valid.
96 63 146 123	TX_EN[D:A]	I	**Transmit Enable.** When driven high, this signal indicates there is valid data on TXD[3:0]. TX_EN is synchronous with TX_CLK. When SERIAL_SEL is active-high, this pin indicates there is valid data on TXD[0].
95 62 145 122	TX_ER[D:A]	I	**Transmit Coding Error.** When driven high, this signal causes the encoder to intentionally corrupt the byte being transmitted across the MII (00100 will be transmitted). When SERIAL_SEL is active-high, this pin is ignored.
110 78 161 138	MII_EN[D:A]	I	**MII Enable.** For normal MII mode of operation (nonbused mode), MII_EN for each channel must be tied high to enable each individual port being used.

Pin Information (continued)

Pin Descriptions (continued)

Table 4. Serial Interface Pins in Bused Mode (Security Not Selected)

Pin	Signal	Type	Description
148	TX_CLK	O	**Shared Transmit Clock.** 10 MHz clock output in serial mode. TX_CLK provides timing reference for the transfer of the TX_EN and TXD signals that are sampled on the rising edge of TX_CLK. When operating in bused mode, the REF10 input clock must be used, and the REF_SEL pin must be pulled high through a 4.7 kΩ resistor (TXLED[A] pin).
109 108 107 105	CRS[D:A]	O	**Carrier Sense.** When CRS_SEL is low, this signal is asserted high when either the transmit or receive medium is nonidle. This signal remains asserted throughout a collision condition. When CRS_SEL is high, CRS is asserted on receive activity only. CRS_SEL is set via the MII management interface or the CRS_SEL pin.
154	RX_CLK	O	**Shared Receive Clock.** 10 MHz clock output. RX_CLK has a worst-case 45/55 duty cycle. RX_CLK provides the timing reference for the transfer of RXD.
155	RXD	O	**Shared Receive Data.** Serial data output that is synchronous to the falling edge of RX_CLK.
60 59 57 56	RX_EN[D:A]	I	**Receive Enable.** When SECURITY_MODE_SELECT is not enabled and RX_EN is driven high, its channel's data and clock (RXD[0] and RX_CLK) are driven onto the shared serial bus. When RX_EN[D:A] are set low, the serial bus will float. Care should be taken that no more than one RX_EN is asserted at a time. When SECURITY_MODE_SELECT is enabled, these pins are ignored.
139	TXD	I	**Shared Transmit Data.** 10 Mbits/s serial input synchronous with TX_CLK.
93 92 90 89	TX_EN[D:A]	I	**Transmit Enable.** When driven high, this signal indicates that there is valid data on TXD.
76 75 74 72	COL[D:A]	O	**Collision Detect.** In half-duplex mode, this signal signifies that a collision has occurred on the network. COL is asserted high whenever there is transmit and receive activity on the UTP media. COL is the logical AND of TX_EN and receive activity, and it is an asynchronous output. When SERIAL_SEL is high, this signal indicates that the jabber timer has expired.
63, 66, 67, 78, 96, 99, 100, 110, 116, 117, 119, 120, 122, 123, 125, 126, 127, 128, 130, 131, 132, 134, 135, 136, 138, 146, 149, 150, 161	NC	—	**No Connect.** Do not connect these pins.

Pin Information (continued)

Pin Descriptions (continued)

Table 5. Serial Interface Pins in Bused Mode (Security Selected)

Pin	Signal	Type	Description
148	TX_CLK	O	**Shared Transmit Clock.** 10 MHz clock output in serial mode. TX_CLK provides timing reference for the transfer of the TX_EN and TXD signals that are sampled on the rising edge of TX_CLK. When operating in bused mode, the REF10 input clock must be used, and the REF_SEL pin must be pulled high through a 4.7 kΩ resistor (TXLED[A] pin).
99 66 149 126	CRS[D:A]	O	**Carrier Sense.** When SECURITY_MODE_SELECT is asserted, the LU1X54 will output CRS on these pins.
154	RX_CLK	O	**Shared Receive Clock.** 10 MHz clock output. RX_CLK has a worst-case 45/55 duty cycle. RX_CLK provides the timing reference for the transfer of RXD.
155	RXD	O	**Shared Receive Data.** Serial data output that is synchronous to the falling edge of RX_CLK.
110 78 161 138	RX_EN[D:A]	I	**Receive Enable.** When SECURITY_MODE_SELECT is enabled and RX_EN is driven high, its channel's data and clock (RXD and RX_CLK) are driven onto the shared serial bus.
139	TXD	I	**Shared Transmit Data.** 10 Mbits/s serial input synchronous with TX_CLK.
93 92 90 89	SECURITY[3:0]	I	**Security.** When SECURITY is enabled, these pins are redefined to be the security input pins. When SECURITY is activated, the LU1X54 will ignore the transmit data, and a fixed pattern of all 1s is transmitted. Security should not be asserted until after the entire preamble has been transmitted.
96 63 146 123	TX_EN[D:A]	I	**Transmit Enable.** When driven high, this signal indicates there is valid data on TXD[3:0]. TX_EN is synchronous with TX_CLK. When SERIAL_SEL active-high is selected, this pin indicates there is valid data on TXD[0].
100 67 150 127	COL[D:A]	O	**Collision Detect.** In half-duplex mode, this signal signifies that a collision has occurred on the network. COL is asserted high whenever there is transmit and receive activity on the UTP media. COL is the logical AND of TX_EN and receive activity, and it is an asynchronous output. When SERIAL_SEL is high, this signal indicates that the jabber timer has expired.
56, 57, 59, 60, 72, 74, 75, 76, 105, 107, 108, 109, 116, 117, 119, 120, 122, 125, 128, 130, 131, 132, 134, 135, 136	NC	—	**No Connect.** Do not connect these pins.

Pin Information (continued)

Pin Descriptions (continued)

Table 6. MII Management Pins

Pin	Signal	Type	Description
113	MDC	I	**Management Data Clock.** This is the timing reference for the transfer of data on the MDIO signal. This signal may be asynchronous to RX_CLK and TX_CLK. The maximum clock rate is 10 MHz. When running MDC above 5 MHz, MDC must be synchronous with LSCLK and have a setup time of 15 ns and a hold time of 5 ns with respect to LSCLK. When using an external crystal instead of an LSCLK input, the maximum MDC rate is 5 MHz.
112	MDIO	I/O	**Management Data Input/Output.** This I/O is used to transfer control and status information between the LU1X54 and the station management. Control information is driven by the station management synchronous with MDC. Status information is driven by the LU1X54 synchronous with MDC. This pin requires a 1.5 kΩ pull-up resistor
53	MASK_STAT_INT	O	**Maskable Status Interrupt.** This pin will go high whenever there is a change in status as defined in Table 23.

Table 7. Twisted-Pair (TP) Interface Pins

Pin	Signal	Type	Description
5 9 16 20	TPIN+[D:A]	I	**Received Data.** Positive differential received 10 Mbaud Manchester data from magnetics.
6 10 17 21	TPIN–[D:A]	I	**Received Data.** Negative differential received 10 Mbaud Manchester data from magnetics.
32 36 46 50	TPOUT+[D:A]	O	**Transmit Data.** Positive differential transmit 10 Mbaud Manchester data to magnetics.
33 37 47 51	TPOUT–[D:A]	O	**Transmit Data.** Negative differential transmit 10 Mbaud Manchester data to magnetics.

Pin Information (continued)

Pin Descriptions (continued)

Table 8. Miscellaneous Pins

Pin	Signal	Type	Description
197	AUTO_EN	I	**Autonegotiation Enable.** When this pin is high, autonegotiation is enabled. Pulsing this pin will cause autonegotiation to restart. This input has the same function as register 0, bit 12. This input and the register bit are ANDed together.
1, 7, 11, 14, 18, 22, 24, 26, 29, 31, 35, 39, 41, 45, 49, 58, 64, 73, 79, 82, 86, 91, 97, 106, 115, 118, 124, 133, 141, 147, 156, 163, 177, 178, 181, 182, 186, 208	GND/Vss	PWR	**Ground.** (38 pins.)
4, 8, 12, 15, 19, 23, 28, 30, 34, 38, 40, 44, 48, 52, 61, 69, 77, 80, 83, 94, 102, 111, 121, 129, 137, 144, 152, 160, 167, 172, 179, 180, 185, 195, 202	VDD	PWR	**VDD.** Single 5.0 V ± 5% power supply. (35 pins.)
196	3ST_EN	I	**3-State Enable.** When this pin is high, all digital outputs will be 3-stated. For normal operating conditions, pull this pin low.
13	BGREF	I	**Band Gap Reference.** Connect these pins to a 22.1 kΩ ± 1% resistor to ground. The parasitic load capacitance should be less than 15 pF.
42	ISET_10	I	**Current Set 10 Mbits/s.** An external resistor (24.9 kΩ) is placed from this pin to ground to set the 10 Mbits/s TP driver transmit output level.
114	REF10	I	**10 MHz Input Clock.** Optional reference clock for 10 Mbits/s repeater mode for phase alignment. When used, TX_CLK will be driven from REF10. If not used, let this pin float. This pin has an internal 50 kΩ pull-down resistor.
166	TXLED[D]	O	**Transmit LED[D].** This pin indicates transmit activity on port D. External buffers are necessary to drive the LEDs.
165	TXLED[C]	O	**Transmit LED[C].** This pin indicates transmit activity on port C. External buffers are necessary to drive the LEDs.
164	TXLED[B]	O	**Transmit LED[B].** This pin indicates transmit activity on port B. External buffers are necessary to drive the LEDs.

Pin Information (continued)

Pin Descriptions (continued)

Table 8. Miscellaneous Pins (continued)

Pin	Signal	Type	Description
162	TXLED[A]/ REF_SEL	I/O	**Transmit LED[A].** This pin indicates transmit activity on port A. External buffers are necessary to drive the LEDs.
			Reference Select. At powerup, this pin may be used to select the 10 MHz reference input of pin REF10 by pulling it high through a 4.7 kΩ resistor, if station management is unavailable. This is the same function as register 30, bit 2. This pin has an internal 50 kΩ pull-down resistor for normal operation (REF10 not used). This input and the register bit are ORed together.
171 170 169 168	RXLED[D:A]	O	**Receive LED[D:A].** These pins indicate receive activity. External buffers are necessary to drive the LEDs. These pins have internal 50 kΩ pull-down resistors.
176 175 174 173	COLED[D:A]	O	**Collision LED.** These pins indicate collision occurrence. External buffers are necessary to drive the LEDs. Channels A and B have internal 50 kΩ pull-down resistors but not channels C and D.
190	LINKLED[D]/ PHYADD[2]	I/O	**Link LED[D].** This pin indicates good link status on port D. External buffers are necessary to drive the LEDs.
			PHY Address 2. At powerup or reset, this pin is used to set the PHY address bit 2. If this pin is pulled high through a 50 kΩ resistor, it will set PHYADD[2] to a 1. If this pin is pulled low through a 50 kΩ resistor, it will set PHYADD[2] to a 0.
189	LINKLED[C]/ PHYADD[1]	I/O	**Link LED[C].** This pin indicates good link status on port C. External buffers are necessary to drive the LEDs.
			PHY Address 1. At powerup or reset, this pin is used to set the PHY address bit 1. If this pin is pulled high through a 50 kΩ resistor, it will set PHYADD[1] to a 1. If this pin is pulled low through a 50 kΩ resistor, it will set PHYADD[1] to a 0.
188	LINKLED[B]/ PHYADD[0]	I/O	**Link LED[B].** This pin indicates good link status on port B. External buffers are necessary to drive the LEDs.
			PHY Address 0. At powerup or reset, this pin may be used to set the PHY address bit 0. If this pin is pulled high through a 50 kΩ resistor, it will set PHYADD[0] to a 1. If this pin is pulled low through a 50 kΩ resistor, it will set PHYADD[0] to a 0.

Pin Information (continued)

Pin Descriptions (continued)

Table 8. Miscellaneous Pins (continued)

Pin	Signal	Type	Description
187	LINKLED[A]/ NO_LP	I/O	**Link LED[A].** This pin indicates good link status on port A. External buffers are necessary to drive the LEDs.
			No Link Pulse. This pin is used at powerup or reset to select the NO_LP function of register 30, bit 0 for all four channels by pulling this pin high through a 4.7 kΩ resistor. This input and the register bit [30.0] are ORed together. This pin has an internal 50 kΩ pull-down resistor to set the default to normal link pulse ON mode.
193	SECURITY_MODE_SELECT	I	**Security Mode Select.** At powerup or reset, if this pin is pulled high through a 4.7 kΩ resistor, it enables the use of the security feature and redefines the CRS, COL, and TX_EN10 pins. This pin is internally pulled low through a 50 kΩ pull-down resistor. The default value is SECURITY_MODE _SELECT disabled. When SECURITY_MODE_SELECT is asserted, the TX_EN inputs are used as the security inputs. When security is activated high, the LU1X54 will transmit a jam signal instead of data.
192	BUSED_MII_MODE	I	**Bused MII Mode Select.** At powerup or reset, if the bused MII mode select pin is pulled high through a 4.7 kΩ resistor, data streams from ports running at 100 Mbits/s will appear on the single 100 Mbits/s MII (port A), and data streams from ports running at 10 Mbits/s will appear at the single 10 Mbits/s serial interface (port B). In addition, control signals TX_EN[D:A], RX_EN[D:A], and CRS[D:A] become active. This pin is internally pulled low through a 50 kΩ pull-down resistor. The default value is bused mode disabled.
191	ISOLATE_MODE	I	**Isolate Mode.** As an input, this pin can be used at powerup or reset to select the isolate operation mode. If this pin is pulled high through a 4.7 kΩ resistor, the LU1X54 will powerup or reset to the isolate mode. (MII outputs to high-impedance state.) This pin is internally pulled low through a 50 kΩ resistor. The default state is for the LU1X54 to powerup or reset in a nonisolate mode. This pin and register bit [10.0] are ORed together during powerup and reset.

Pin Information (continued)

Pin Descriptions (continued)

Table 8. Miscellaneous Pins (continued)

Pin	Signal	Type	Description
201	H_DUPLED[D]/ FULL_DUP	I/O	**Half-Duplex LED[D].** When this output is high, it indicates half-duplex mode. When it is low, it indicates full duplex. External buffers are necessary to drive the LEDs. This output is only valid when the link is up.
			Full Duplex. At powerup, this pin may be used to select full-duplex operation for all four channels by pulling it high through a 4.7 kΩ resistor, if station management is unavailable. This is the same function as register 0, bit 8. This pin has an internal 50 kΩ pull-down resistor to default to half duplex for normal operation. This input and the register bit [0.8] are ORed together during powerup and reset.
198	H_DUPLED[A]	I/O	**Half-Duplex LED[A].** When this output is high, it indicates half-duplex mode. When low, it indicates full duplex. External buffers are necessary to drive the LEDs. This output is only valid when the link is up.
87	LSCLK/XTALIN	I	**CMOS Local Symbol Clock.** A 20 MHz clock, ±100 ppm, 40%—60% duty cycle.
			Crystal Oscillator Input. A 20 MHz crystal ± 25 ppm can be connected across XTALIN and XTALOUT.
88	XTALOUT	I	**Crystal Oscillator Output.** A 20 MHz crystal ± 25 ppm can be connected across XTALIN and XTALOUT. If a single-ended external clock (LSCLK) is connected to XTALIN, the crystal output pin should be left floating.
55 207 206 205 204	MODE[4:0]	I	**Test Mode Select.** Reserved for manufacturing testing. These pins should be tied low for normal operation.
203	RESET	I	**Full Chip Reset.** Reset must be asserted high for at least five LSCLK cycles.
199	H_DUPLED[B]/ CRS_SEL	I/O	**Half-Duplex LED[B].** When this output is high, it indicates half-duplex mode. When it is low, it indicates full duplex. External buffers are necessary to drive the LEDs. This output is only valid when the link is up.
			Carrier Sense Select. At powerup, this pin may be used to select the mode of CRS operation. When this pin is pulled high through a 4.7 kΩ resistor, CRS will be asserted on receive activity only. This is the same function as register 29, bit 10. This pin has an internal 50 kΩ pull-down resistor for normal mode operation (default: CRS asserted on transmit or receive activity). This input and the register bit [29.10] are ORed together during powerup and reset.

Pin Information (continued)

Pin Descriptions (continued)

Table 8. Miscellaneous Pins (continued)

Pin	Signal	Type	Description
200	H_DUPLED[C]/ SERIAL_SEL	I/O	**Half-Duplex LED[C].** When this output is high, it indicates half- duplex mode. When low, it indicates full duplex. External buffers are necessary to drive the LEDs. This output is only valid when the link is up.
			Serial Select. At powerup, this pin may be used to set the SERIAL_SEL function of register 30, bit 1 for all four channels by pulling it high through a 4.7 kΩ resistor if station management is unavailable. This pin has an internal 50 kΩ pull-down resistor for normal mode operation (default). This input and the register bit [30.1] are ORed together during powerup and reset.
2 3 84 85	RESERVED	—	**Reserved.** Do not connect these pins.
25, 27, 43, 54, 81, 183, 184, 194	NC	—	**No Connect.** Do not connect these pins.

MII Station Management

Basic Operations

The primary function of station management is to transfer control and status information about the LU1X54 to a management entity. This function is accomplished by the MDC clock input, which has a maximum frequency of 12.5 MHz, along with the MDIO pin.

The management interface (MII) uses MDC and MDIO to physically transport information between the PHY and the station management entity.

A specific set of registers and their contents (described in Table 9) defines the nature of the information transferred across this interface. Frames transmitted on the MII management interface will have the frame structure shown in Table 9. The order of bit transmission is from left to right. Note that reading and writing of the management register must be completed without interruption.

Since the LU1X54 is a four-channel device, each of the management registers is duplicated four times as depicted in the functional block diagram shown in Figure 1. To select a particular channel [D:A], write to that channel's unique PHY address as described in Table 10.

MII Management Frames

The fields and format for management frames are described in the following tables.

Table 9. MII Management Frame Format

Read/Write (R/W)	Pre	ST	OP	PHYADD	REGAD	TA	DATA	Idle
R	1 . . . 1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
W	1 . . . 1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

Table 10. MII Management Frames—Field Descriptions

Field	Description
Pre	**Preamble.** The preamble is a series of 32 ones. The LU1X54 will accept frames with no preamble. This is indicated by a 1 in register 1, bit 6.
ST	**Start of Frame.** The start of frame is indicated by a 01 pattern.
OP	**Operation Code.** The operation code for a read transaction is 10. The operation code for a write transaction is 01.
PHYADD	**PHY Address.** The PHY address is 5 bits, allowing for 32 unique addresses. The first PHY address bit transmitted and received is the MSB of the address. A station management entity, which is attached to multiple PHY entities, must have prior knowledge of the appropriate PHY address for each entity. The address 00000 is the broadcast address. This address will produce a match regardless of the local address. The LU1X54 maps the PHYADD[2:0] to the most significant 3 bits, while the least significant 2 bits address the channel within the LU1X54 as follows: 00: Channel A. 01: Channel B. 10: Channel C. 11: Channel D.
REGAD	**Register Address.** The register address is 5 bits, allowing for 32 unique registers within each PHY. The first register address bit transmitted and received is the MSB of the address.
TA	**Turnaround.** The turnaround time is a 2-bit time spacing between the register address field and the data field of a frame to avoid drive contention on MDIO during a read transaction. During a write to the LU1X54, these bits are driven to a 10 by the station. During a read, the MDIO is not driven during the first bit time and is driven to a 0 by the LU1X54 during the second bit time.
DATA	**Data.** The data field is 16 bits. The first bit transmitted and received is bit 15 of the register being addressed.

MII Station Management (continued)

Management Registers (MR)

Register Overview

The MII management 16-bit register (MR) set is implemented as described in the table below.

Table 11. MII Management Registers (MR)

Register Address	Symbol	Name	Default (Hex Code)
0	MR0	Control Register	3000
1	MR1	Status Register	1849
2	MR 2	PHY Identifier Register 1	0180
3	MR 3	PHY Identifier Register 2	74F1
4	MR4	Autonegotiation Advertisement Register	0061
5	MR5	Autonegotiation Link Partner Ability Register (Base Page)	0000
5	MR5	Autonegotiation Link Partner Ability Register (Next Page)	—
6	MR6	Autonegotiation Expansion Register	0000
7	MR7	Next Page Transmit Register	0000
8—27	MR8—MR27	Reserved	0000
28	MR28	Device-Specific Register 1 (Status)	—
29	MR29	Device-Specific Register 2	0080
30	MR30	Device-Specific Register 3 (Control)	0000
31	MR31	Device-Specific Register 4 (Quick Status)	—

MII Station Management (continued)

Management Registers (MR) (continued)

This section discusses each management register and its bit definitions.

Table 12. MR0—Control Register Bit Descriptions

Register/Bit[1]	Type[2]	Description
0.15 (SW_RESET)	R/W	**Reset.** Setting this bit to a 1 will reset the entire LU1X54. All registers will be set to their default state. This bit is self-clearing. The default is 0.
0.14 (LOOPBACK)	R/W	**Loopback.** When this bit is set to 1, no data transmission will take place on the media. Any receive data will be ignored. The loopback signal path will contain all circuitry up to, but not including, the PMD. The default value is a 0.
0.13 (RESERVED)	R/W	**Reserved.** This bit should always be set to a 0.
0.12 (NWAY_ENA)	R/W	**Autonegotiation Enable.** The autonegotiation process will be enabled by setting this bit to a 1. The default state is a 1.
0.11 (PWRDN)	R/W	**Powerdown.** The LU1X54 may be placed in a low-power state by setting this bit to a 1. While in the powerdown state, the LU1X54 will respond to management transactions. The default state is a 0.
0.10 (ISOLATE)	R/W	**Isolate Mode.** When this bit is set to a 1, the MII outputs will be brought to the high-impedance state. The default state is a 0. This bit is ORed with the ISOLATE_MODE pin during powerup and reset.
0.9 (REDONWAY)	R/W	**Restart Autonegotiation.** Normally, the autonegotiation process is started at powerup. The process may be restarted by setting this bit to a 1. The default state is a 0. The NWAYDONE bit (register 1, bit 5) is reset when this bit goes to a 1. This bit is self-cleared when autonegotiation restarts.
0.8 (FULL_DUP)	R/W	**Duplex Mode.** This bit reflects the mode of operation (1 = full duplex; 0 = half duplex). This bit is ignored when the autonegotiation enable bit (register 0, bit 12) is enabled. The default state is a 0. This bit is ORed with the H_DUPLED[D] pin during powerup or reset.
0.7 (COLTST)	R/W	**Collision Test.** When this bit is set to a 1, the LU1X54 will assert the COL signal in response to TX_EN. This bit should only be set when in loopback mode.
0.6:0 (RESERVED)	R/W	**Reserved.** All bits will read 0.

1. Note that the format for the bit descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.
2. R = read, W = write.

MII Station Management (continued)

Management Registers (MR) (continued)

Table 13. MR1—Status Register Bit Descriptions

Register/Bit[1]	Type[2]	Description
1.15 (T4ABLE)	R	**100Base-T4 Ability.** This bit will always be a 0. 0: Not able. 1: Able.
1.14 (TXFULDUP)	R	**100Base-TX Full-Duplex Ability.** This bit will always be a 0. 0: Not able. 1: Able.
1.13 (TXHAFDUP)	R	**100Base-TX Half-Duplex Ability.** This bit will always be a 0. 0: Not able. 1: Able.
1.12 (ENFULDUP)	R	**10Base-T Full-Duplex Ability.** This bit will always be a 1. 0: Not able. 1: Able.
1.11 (ENHAFDUP)	R	**10Base-T Half-Duplex Ability.** This bit will always be a 1. 0: Not able. 1: Able.
1.10:7 (RESERVED)	R	**Reserved.** All bits will read as a 0.
1.6 (NO_PA_OK)	R	**Suppress Preamble.** This bit is set to a 1 indicating that the LU1X54 accepts management frames with the preamble suppressed.
1.5 (NWAYDONE)	R	**Autonegotiation Complete.** When this bit is a 1, it indicates the autonegotiation process has been completed. The contents of registers MR4, MR5, MR6, and MR7 are now valid. The default value is a 0. This bit is reset when autonegotiation is started.
1.4 (REM_FLT)	R	**Remote Fault.** When this bit is a 1, it indicates a remote fault has been detected. This bit will remain set until cleared by reading the register. The default is a 0.
1.3 (NWAYABLE)	R	**Autonegotiation Ability.** When this bit is a 1, it indicates the ability to perform autonegotiation. The value of this bit is always a 1.
1.2 (LSTAT_OK)	R	**Link Status.** When this bit is a 1, it indicates a valid link has been established. This bit has a latching function. A link failure will cause the bit to clear and stay cleared until it has been read via the management interface.
1.1 (JABBER)	R	**Jabber Detect.** This bit will be a 1 whenever a jabber condition is detected. It will remain set until it is read, and the jabber condition no longer exists.
1.0 (EXT_ABLE)	R	**Extended Capability.** This bit indicates that the LU1X54 supports the extended register set (MR2 and beyond). It will always read a 1.

1. Note that the format for the bit descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.
2. R = read.

MII Station Management (continued)

Management Registers (MR) (continued)

Table 14. MR2, 3—PHY Identifier Registers (1 and 2) Bit Descriptions

Register/Bit[1]	Type[2]	Description
2.15:0 (OUI[3:18])	R	**Organizationally Unique Identifier.** The third through the twenty-fourth bit of the OUI assigned to the PHY manufacturer by the *IEEE* are to be placed in bits 2.15:0 and 3.15:10. The value for bits 15:0 is 0180h.
3.15:10 (OUI[19:24])	R	**Organizationally Unique Identifier.** The remaining 6 bits of the OUI. The value for bits15:10 is 1Dh.
3.9:4 (MODEL[5:0])	R	**Model Number.** 6-bit model number of the device. The model number is 15d or Fh.
3.3:0 (VERSION[3:0])	R	**Revision Number.** The value of the present revision number. The value is 01h for the first version.

1. Note that the format for the pin descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.
2. R = read.

Table 15. MR4—Autonegotiation Advertisement Register Bit Descriptions

Register/Bit[1]	Type[2]	Description
4.15 (NEXT_PAGE)	R/W	**Next Page.** The next-page function is activated by setting this bit to a 1. This will allow the exchange of additional data. Data is carried by optional next pages of information.
4.14 (ACK)	R/W	**Link Partner Acknowledge.** This bit is the acknowledge bit from the link code word.
4.13 (REM_FAULT)	R/W	**Remote Fault.** When set to 1, the LU1X54 indicates to the link partner a remote fault condition.
4.12:11 (RESERVED)	R/W	**Reserved.** These bits will read 0.
4.10 (PAUSE)	R/W	**Pause.** When set to a 1, it indicates that the LU1X54 wishes to exchange flow control information with its link partner.
4.9 (100BASET4)	R/W	**100Base-T4.** This bit should always be set to a 0.
4.8 (100BASET_FD)	R/W	**100Base-TX Full Duplex.** This bit should always be set to a 0.
4.7 (100BASETX)	R/W	**100Base-TX Half Duplex.** This bit should always be set to a 0.
4.6 (10BASET_FD)	R/W	**10Base-T Full Duplex.** If written to 1, autonegotiation will advertise that the LU1X54 is capable of 10Base-T full-duplex operation.
4.5 (10BASET)	R/W	**10Base-T.** If written to 1, autonegotiation will advertise that the LU1X54 is capable of 10Base-T operation.
4.4:0 (SELECT)	R/W	**Selector Field.** Reset with the value 00001 for *IEEE* 802.3.

1. Note that the format for the bit descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.
2. R = read, W = write.

MII Station Management (continued)

Management Registers (MR) (continued)

Table 16. MR5—Autonegotiation Link Partner (LP) Ability Register (Base Page) Bit Descriptions

Register/Bit[1]	Type[2]	Description
5.15 (LP_NEXT_PAGE)	R	**Link Partner Next Page.** When this bit is set to 1, it indicates that the link partner wishes to engage in next page exchange.
5.14 (LP_ACK)	R	**Link Partner Acknowledge.** When this bit is set to 1, it indicates that the link partner has successfully received at least three consecutive and consistent FLP bursts.
5.13 (LP_REM_FAULT)	R	**Remote Fault.** When this bit is set to 1, it indicates that the link partner has a fault.
5.12:5 (LP_TECH_ABILITY)	R	**Technology Ability Field.** This field contains the technology ability of the link partner. These bits are similar to the bits defined for the MR4 register (see Table 15).
5.4:0 (LP_SELECT)	R	**Selector Field.** This field contains the type of message sent by the link partner. For *IEEE* 802.3u compliant link partners, this field should read 00001.

1. Note that the format for the pin descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.
2. R = read.

Table 17. MR5—Autonegotiation Link Partner (LP) Ability Register (Next Page) Bit Descriptions

Register/Bit[1]	Type[2]	Description
5.15 (LP_NEXT_PAGE)	R	**Next Page.** When this bit is set to a logic 0, it indicates that this is the last page to be transmitted. A logic 1 indicates that additional pages will follow.
5.14 (LP_ACK)	R	**Acknowledge.** When this bit is set to a logic 1, it indicates that the link partner has successfully received its partner's link code word.
5.13 (LP__MES_PAGE)	R	**Message Page.** This bit is used by the next page function to differentiate a message page (logic 1) from an unformatted page (logic 0).
5.12 (LP_ACK2)	R	**Acknowledge 2.** This bit is used by the next page function to indicate that a device has the ability to comply with the message (logic 1) or not (logic 0).
5.11 (LP_TOGGLE)	R	**Toggle.** This bit is used by the arbitration function to ensure synchronization with the link partner during next-page exchange. Logic 0 indicates that the previous value of the transmitted link code word was logic 1. Logic 1 indicates that the previous value of the transmitted link code word was logic 0.
5.10:0 (MCF)	R	**Message/Unformatted Code Field.** With these 11 bits, there are 2048 possible messages. Message code field definitions are described in annex 28C of the *IEEE* 802.3u standard.

1. Note that the format for the bit descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.
2. R = read.

MII Station Management (continued)

Management Registers (MR) (continued)

Table 18. MR6—Autonegotiation Expansion Register Bit Descriptions

Register/Bit[1]	Type[2]	Description
6.15:5 (RESERVED)	R	**Reserved.**
6.4 (PAR_DET_FAULT)	R/LH	**Parallel Detection Fault.** When this bit is set to 1, it indicates that a fault has been detected in the parallel detection function. This fault is due to more than one technology detecting concurrent link conditions. This bit can only be cleared by reading this register.
6.3 (LP_NEXT_PAGE_ABLE)	R	**Link Partner Next Page Able.** When this bit is set to 1, it indicates that the link partner supports the next-page function.
6.2 (NEXT_PAGE_ABLE)	R	**Next Page Able.** This bit is set to 1, indicating that this device supports the next-page function.
6.1 (PAGE_REC)	R/LH	**Page Received.** When this bit is set to 1, it indicates that a next page has been received.
6.0 (LP_NWAY_ABLE)	R	**Link Partner Autonegotiation Capable.** When this bit is set to 1, it indicates that the link partner is autonegotiation capable.

1. Note that the format for the pin descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.
2. R = read, LH = latched high.

Table 19. MR7—Next-Page Transmit Register Bit Descriptions

Register/Bit[1]	Type[2]	Description
7.15 (NEXT_PAGE)	R/W	**Next Page.** This bit indicates whether or not this is the last next page to be transmitted. When this bit is 0, it indicates that this is the last next page. When this bit is 1, it indicates there is an additional next page.
7.14 (ACK)	R	**Acknowledge.** This bit is the acknowledge bit from the link code word.
7.13 (MESSAGE)	R/W	**Message Page.** This bit is used to differentiate a message page from an unformatted page. When this bit is 0, it indicates an unformatted page. When this bit is 1, it indicates a formatted page.
7.12 (ACK2)	R/W	**Acknowledge 2.** This bit is used by the next-page function to indicate that a device has the ability to comply with the message. It is set as follows: ■ When this bit is 0, it indicates the device cannot comply with the message. ■ When this bit is 1, it indicates the device will comply with the message.
7.11 (TOGGLE)	R	**Toggle.** This bit is used by the arbitration function to ensure synchronization with the link partner during next-page exchange. This bit will always take the opposite value of the toggle bit in the previously exchanged link code word: ■ If the bit is a logic 0, the previous value of the transmitted link code word was a logic 1. ■ If the bit is a 1, the previous value of the transmitted link code word was a 0. The initial value of the toggle bit in the first next-page transmitted is the inverse of the value of bit 11 in the base link code word, and may assume a value of 1 or 0.
7.10:0 (MCF)	R/W	**Message/Unformatted Code Field.** With these 11 bits, there are 2048 possible messages. Message code field definitions are described in annex 28C of the *IEEE* 802.3u standard.

1. Note that the format for the bit descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.
2. R = read, W = write.

MII Station Management (continued)

Management Registers (MR) (continued)

Table 20. MR28—Device-Specific Register 1 (Status Register) Bit Descriptions

Register/Bit[1]	Type[2]	Description
28.15:9 (R28[15:9])	R	**Unused.** Read as 0.
28.8 (BAD_FRM)	R/LH	**Bad Frame.** If this bit is a 1, it indicates a packet has been received without an SFD.This bit is latching high and will only clear after it has been read or the device has been reset. This bit defaults to 0.
28.7 (CODE)	R/LH	**Code Violation.** When this bit is a 1, it indicates a Manchester code violation has occurred. The error code will be output on the RXD lines. Refer to Table 3 for a detailed description of the RXD pin error codes. This bit is latching high and will only clear after it has been read or the device has been reset. This bit defaults to 0.
28.6 (APS)	R	**Autopolarity Status.** When register 30, bit 3 is set and this bit is a 1, it indicates the LU1X54 has detected and corrected a polarity reversal on the twisted pair. If the APF_DIS bit (register 30, bit 3) is set, the reversal will be corrected inside the LU1X54. This bit defaults to 0.
28.5:2 (RESERVED)	R/LH	**Reserved.**
28.1 (RESERVED)	R	**Reserved.**
28.0 (LNK10UP)	R	**Link Up 10.** This bit, when set to a 1, indicates a 10 Mbits/s transceiver is up and operational. This bit defaults to 0.

1. Note that the format for the bit descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.
2. R = read, LH = latched high.

MII Station Management (continued)

Management Registers (MR) (continued)

Table 21. MR29—Device-Specific Register 2 Bit Descriptions

Register/Bit[1]	Type[2]	Description
29.15 (LOCALRST)	R/W	**Management Reset.** This is the local management reset bit. Writing a logic 1 to this bit will cause register 0, register 28, and register 29 to be reset to their default values. This bit is self-clearing. Default state is 0.
29.14 (RST1)	R/W	**Generic Reset 1.** This register is used for manufacture test only. Default state is 0.
29.13 (RST2)	R/W	**Generic Reset 2.** This register is used for manufacture test only. Default state is 0.
29.12 (RESERVED)	R/W	**Reserved.** This bit must remain as a zero.
29.11 (RESERVED)	R/W	**Reserved.** Program to zero.
29.10 (CRS_SEL)	R/W	**Carrier Sense Select.** CRS will be asserted on receive only when this bit is set to a 1. If this bit is set to logic 0, CRS will by asserted on receive or transmit. This bit is ORed with the H_DUPLED[B] pin during powerup and reset. Default state is 0.
29.9 (LINK_ERR)	R/W	**Link Error Indication.** When this bit is a 1, a link error code will be reported on RXD[3:0] of the LU1X54 when RX_ER is asserted on the MII. The specific RXD error codes are listed in Table 3. If this bit is 0, it will disable this function. Default state is 0.
29.8 (PKT_ERR)	R/W	**Packet Error Indication Enable.** When this bit is a 1, a packet error code, which indicates that the scrambler is not locked, will be reported on RXD[3:0] of the LU1X54 when RX_ER is asserted on the MII. When this bit is 0, it will disable this function. Default state is 0.
29.7 (PULSE_STR)	R/W	**Pulse Stretching.** When this bit is set to 1, the COLED[D:A], TXLED[D:A], and RXLED[D:A] output signal will be stretched between approximately 42 ms—84 ms. If this bit is set to 0, it will disable this feature. Default state is 1.
29.6:3 (RESERVED)	R/W	**Reserved.** These bits must remain as a zero.
29.2 (JAM_COL)	R/W	**Jam Enable.** When this bit is a 1, it enables JAM associated with carrier integrity to be ORed with COL. Default state is 0.
29.1 (FEF_EN)	R/W	**Far-End Fault Enable.** This bit is used to enable the far-end fault detection and transmission capability. This capability may only be used if autonegotiation is disabled. This capability is to be used only with media which does not support autonegotiation. Setting this bit to 1 enables far-end fault detection and generation. Logic 0 will disable the function. Default state is 0.
29.0 (RESERVED)	R/W	**Reserved.** This bit must remain as a zero.

1. Note that the format for the bit descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.
2. R = read, W = write.

MII Station Management (continued)

Management Registers (MR) (continued)

Table 22. MR30—Device-Specific Register 3 (Control) Bit Descriptions

Register/Bit[1]	Type[2]	Description
30.15:7 (R28[15:7])	R/W	**Unused.** Read as 0.
30.6 (RESERVED)	R/W	**Reserved.** This bit must remain as a zero.
30.5 (HBT_EN)	R/W	**Heartbeat Enable.** When this bit is a 1, the heartbeat function will be enabled. Valid in 10 Mbits/s mode only. Default state is 0.
30.4 (ELL_EN)	R/W	**Extended Line Length Enable.** When this bit is a 1, the receive squelch levels are reduced from a nominal 435 mV to 350 mV, allowing reception of signals with a lower amplitude. Valid in 10 Mbits/s mode only. Default state is 0.
30.3 (APF_DIS)	R/W	**Autopolarity Function Disable.** When this bit is a 0 and the LU1X54 is in 10 Mbits/s mode, the autopolarity function will determine if the TP link is wired with a polarity reversal. If there is a polarity reversal, the LU1X54 will assert the APS bit (register 28, bit 6) and correct the polarity reversal. If this bit is a 1 and the device is in 10 Mbits/s mode, the reversal will not be corrected. Default state is 0.
30.2 (REF_SEL)	R/W	**Reference Select.** When this bit is a 1, the external 10 MHz reference input clock REF10 is used for phase alignment. Default state is 0.
30.1 (SERIAL _SEL)	R/W	**Serial Select.** When this bit is set to a 1, 10 Mbits/s serial mode will be selected. This bit is ORed with the H_DUPLED[C] pin during powerup and reset. Default state is 0.
30.0 (ENA_NO_LP)	R/W	**No Link Pulse Mode.** Setting this bit to a 1 will allow 10 Mbits/s operation with link pulses disabled. This bit is ORed with the LINKLED[A] pin during powerup and reset. Default state is 0.

1. Note that the format for the bit descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.
2. R = read, W = write.

MII Station Management (continued)

Management Registers (MR) (continued)

Table 23. MR31—Device-Specific Register 4 (Quick Status) Bit Descriptions

Register/Bit[1]	Type[2]	Description
31.15 (RESERVED)	R	**Reserved.** This bit will always be a 0.
31.14 (LINK_STAT_CHANGE)	R	**Link Status Change.** When bit [31.7] is set to a 1, this bit will go high whenever there is a change in link status (bit [31.11]).
31.13 (REM_FLT)	R	**Remote Fault.** When this bit is a 1, it indicates a remote fault has been detected. This bit will remain set until cleared by reading the register. Default is a 0.
31.12 (JABBER)	R	**Jabber.** If this bit is set, it indicates a jabber condition has been detected. This bit will remain set until cleared by reading the register.
31.11 (LSTAT_OK)	R	**Link Status.** When this bit is a 1, it indicates a valid link has been established. This bit has a latching low function. A link failure will cause the bit to clear and stay cleared until it has been read via the management interface.
31.10 (PAUSE)	R	**Link Partner Pause.** When this bit is set to a 1, it indicates that the LU1X54 wishes to exchange flow control information.
31.9 (RESERVED)	R	**Reserved.** This bit will always be a 0.
31.8 (FULL_DUP)	R	**Duplex Mode.** When this bit is set to a 1, it indicates that the link has negotiated to full-duplex mode. When this bit is a 0, it indicates that the link has negotiated to half-duplex mode.
31.7 (INT_CONF)	R/W	**Interrupt Configuration.** When this bit is set high, it redefines bit [31.14] to become the LINK_STAT_CHANGE bit, and the interrupt pin (MASK_STAT_INT) goes high only when the link status changes (bit [31.14] goes high). This bit defaults to 0.
31.6 (MASK_STAT_INT)	R/W	**Interrupt Mask.** When set high, no interrupt is generated by this channel under any condition. When set low, interrupts are generated according to bit [31:7].
31.5:3 (LOW_AUTO__STATE)	R	**Lowest Autonegotiation State.** These 3 bits report the state of the lowest autonegotiation state reached since the last register read, according to the priority order listed below: 000: Autonegotiation enable. 001: Transmit disable or ability detect. 010: Link status check. 011: Acknowledge detect. 100: Complete acknowledge. 101: FLP link good check. 110: Next page wait. 111: FLP link good.
31.2:0 (HI_AUTO_STATE)	R	**Highest Autonegotiation State.** These 3 bits report the state of the highest autonegotiation state reached since the last register read, as defined above for bit [31.5:3].

1. Note that the format for the bit descriptions is as follows: the first number is the register number, the second number is the bit position in the register, and the name of the instantiated pad is in capital letters.
2. R = read.

MII Station Management (continued)

Unmanaged Operations

The LU1X54 allows the user to set some of the station management functions during powerup or reset by strapping outputs high or low through weak resistors (50 kΩ). Table 24 shows the functions and their associated output pin. For detailed information on the function of these output pins, refer to the section on management registers described earlier in this data sheet. Also, information on how these output pins should be strapped is discussed in the Pin Descriptions section (Table 3 through Table 8).

Table 24. Output Pins

Function (Register/Bit)	Pin	Internal Pull-Up/Pull-Down
PHYADD[2:0]	LINKLED[D:B]	None
NO_LP	LINKLED[A]	50 kΩ down
REF_SEL	TXLED[A]	50 kΩ down
FULL _DUP	H_DUPLED[D]	50 kΩ down
SERIAL_SEL	H_DUPLED[C]	50 kΩ down
CRS_SEL	H_DUPLED[B]	50 kΩ down

Mode Select

Table 25. LU1X54 Modes

MODE[4:0]	Description
00000	Normal operation
00001—11111	Reserved

Absolute Maximum Ratings (T_A = 25 °C)

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 26. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Ambient Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{stg}	–40	125	°C
Voltage on Any Pin with Respect to Ground	—	–0.5	V_{DD} + 0.5	V
Maximum Supply Voltage	—	—	5.5	V

Table 27. Operating Conditions

Parameter	Symbol	Min	Type*	Max	Unit
Operating Supply Voltage	—	4.75	5.0	5.25	V
Power Dissipation:					
All Ports 10 Mbits/s	P_D	—	2.0	—	W
All Ports Autonegotiating	P_D	—	1.5	—	W

* Typical power dissipations are specified at 5.0 V and 25 °C. This is the power dissipated by the LU1X54. An additional 0.2 W of power is required for the external twisted-pair driver termination resistors.

Electrical Characteristics

The following specifications apply for V_{DD} = 5 V ± 5%.

Table 28. dc Characteristics

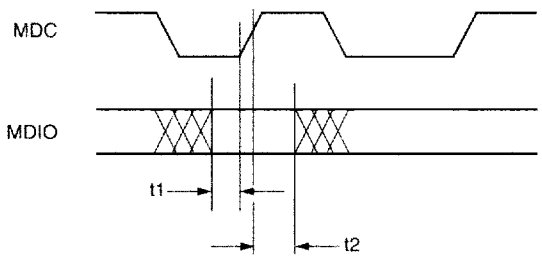
Parameter	Symbol	Min	Typ	Max	Unit
TTL Inputs:					
Input High Voltage	V_{IH}	2.0	—	—	V
Input Low Voltage	V_{IL}	—	—	0.8	V
Input High Current	I_{IH}	—	—	50	µA
Input Low Current	I_{IL}	—	—	–400	µA
Input Leakage Current	I_L	—	—	50	µA
TTL Outputs:					
Output High Voltage	V_{OH}	2.4	—	—	V
Output Low Voltage	V_{OL}	—	—	0.45	V
Output Short-circuit Current	I_{SC}	–15	—	–85	mA
10 Mbits/s Twisted Pair (TP): Input Voltage	V_{DIFF}	0.35	—	2.0	V
10 Mbits/s Twisted Pair (TP): Output Current	V_{DIFF}	45	50	55	mA

Timing Characteristics (Preliminary)

Table 29. MII Management Interface Timing (100 pF Load)

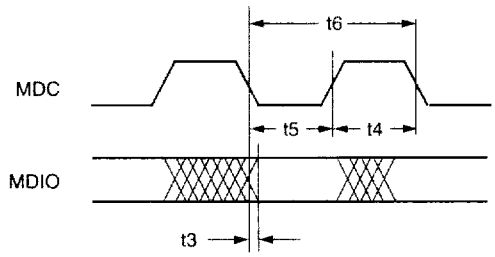
Name	Parameter	Min	Typ	Max	Unit
t1	MDIO Valid to Rising Edge of MDC (setup)	10	—	—	ns
t2	Rising Edge of MDC to MDIO Invalid (hold)	10	—	—	ns
t3	MDC Falling Edge to MDIO Valid (prop. delay)	0	—	40	ns
t4	MDC High*	—	200	—	ns
t5	MDC Low*	40	200	—	ns
t6	MDC Period*	80	400	—	ns

* When operating MDC above 6.25 MHz, MDC must be synchronous with LSCLK and have a setup time of 15 ns and a hold time of 5 ns, with respect to LSCLK.



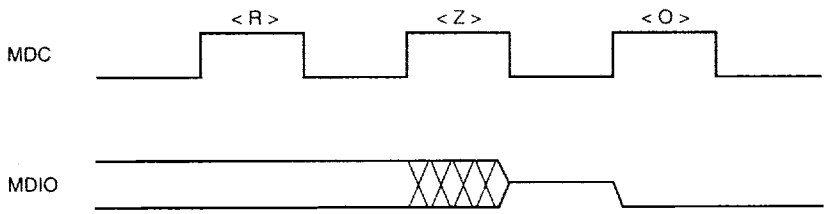
5-4959(F).r1

Figure 8. MDIO Input Timing



5-4960(F).c

Figure 9. MDIO Output Timing



5-5312(F).r1

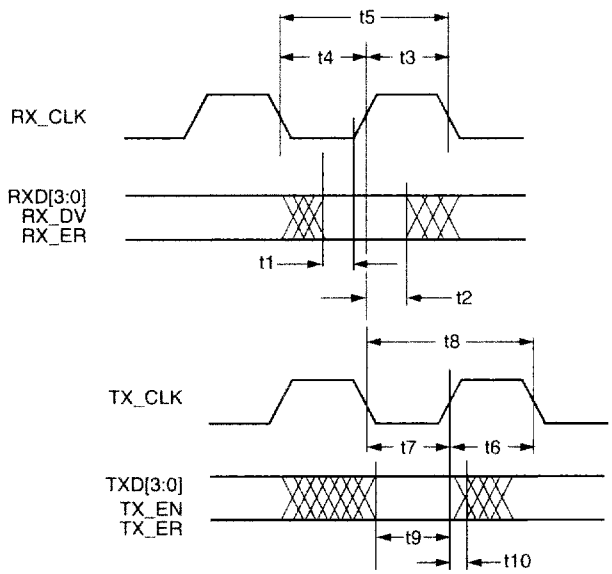
Note: MDIO turnaround (TA) time is a 2-bit time spacing between the register address field, and the data field of a frame to avoid drive contention on MDIO during a read transaction. During a write to the LU1X54, these bits are driven to a 10 by the station. During a read, the MDIO is not driven during the first bit time and is driven to a 0 by the LU1X54 during the second bit time.

Figure 10. MDIO During TA (Turnaround) of a Read Transaction

Timing Characteristics (Preliminary) (continued)

Table 30. MII Data Timing

Name	Parameter	Min	Typ	Max	Unit
t1	RXD[3:0], RX_ER, RX_DV Valid to RX_CLK High	100	—	—	ns
t2	RX_CLK High to RXD[3:0], RX_DV, RX_ER Invalid	100	—	—	ns
t3	RX_CLK High	180	—	220	ns
t4	RX_CLK Low	180	—	220	ns
t5	RX_CLK Period	—	40	—	ns
t6	TX_CLK High	180	—	220	ns
t7	TX_CLK Low	180	—	220	ns
t8	TX_CLK Period	—	40	—	ns
t9	TXD[3:0], TX_EN, TX_ER Setup to TX_CLK	140	—	—	n
t10	TXD[3:0], TX_EN, TX_ER Hold to TX_CLK	0	—	—	ns



5-5432(F).a

Figure 11. MII Data Timing Requirements

Timing Characteristics (Preliminary) (continued)

Table 31. Serial 10 Mbits/s Timing for TPIN±, CRS, and RX_CLK

Name	Parameter	Min	Max	Unit
t11	TPIN± Activity to CRS Assertion	40	500	ns
t12	TPIN± Activity to RX_CLK Valid	800	2300	ns
t13	IDL to CRS Deassertion	200	550	ns
t14	Dead Signal to CRS Deassertion	400	1000	ns

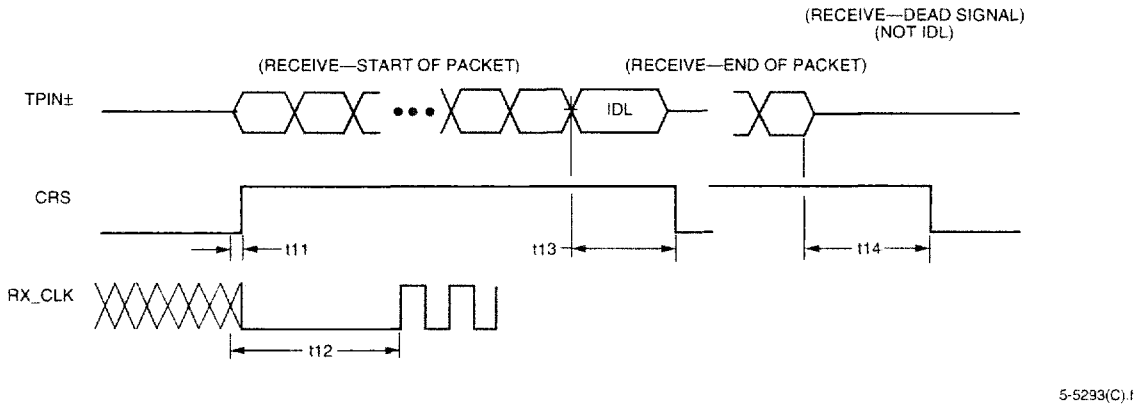


Figure 12. Serial 10 Mbits/s Timing for TPIN±, CRS, and RX_CLK

Table 32. Serial 10 Mbits/s Timing for TX_EN, TPOUT±, CRS, and RX_CLK

Name	Parameter	Min	Max	Unit
t15	TX_EN Asserted to Transmit Pair Activity	50	400	ns
t16	TX_EN Asserted to CRS Asserted Due to Internal Loopback	5	1900	ns
t17	TX_EN Asserted to RX_CLK Valid Due to Internal Loopback	1000	1700	ns
t18	TX_EN Deasserted to IDL Transmission	50	300	ns
t19	IDL Pulse Width	250	350	ns

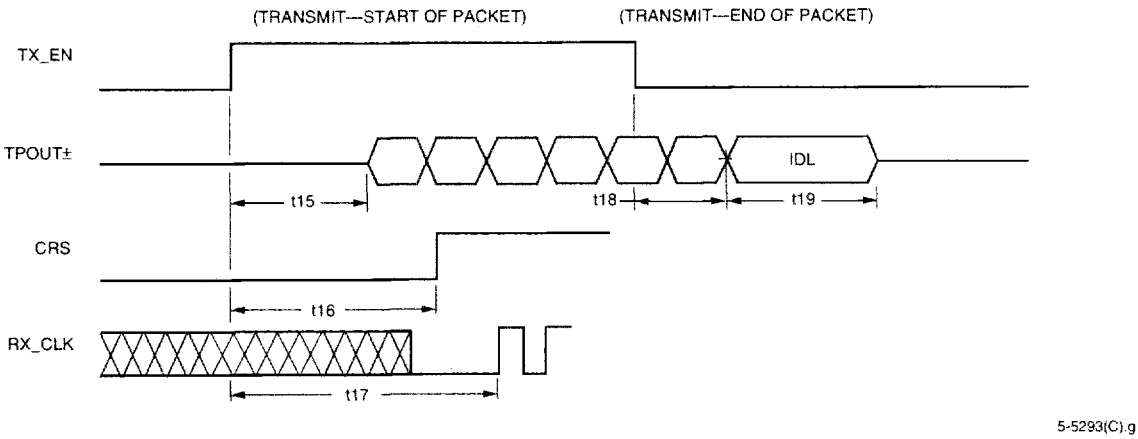
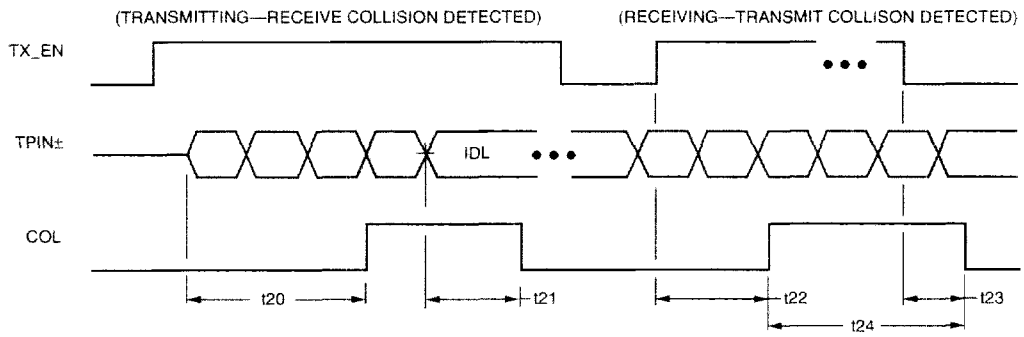


Figure 13. Serial 10 Mbits/s Timing for TX_EN, TPOUT±, CRS, and RX_CLK

Timing Characteristics (Preliminary) (continued)

Table 33. Serial 10 Mbits/s Timing for TX_EN, TPIN±, and COL

Name	Parameter	Min	Max	Unit
t20	Time to Assert COL; LU1X54 Is Transmitting; Receive Activity Starts	40	400	ns
t21	Time to Deassert COL; LU1X54 Is Transmitting; Receive Activity Ceases	300	900	ns
t22	Time to Assert COL; LU1X54 Is Receiving; Transmit Activity Starts	5	400	ns
t23	Time to Deassert COL; LU1X54 Is Receiving; Transmit Activity Ceases	5	900	ns
t24	COL Pulse Width	100	—	ns



5-5293(C).h

Figure 14. Serial 10 Mbits/s Timing for TX_EN, TPIN±, and COL

Timing Characteristics (Preliminary) (continued)

Table 34. Serial 10 Mbits/s Timing for RX_CLK, CRS, RXD, TX_CLK, TX_EN, and TXD

Name	Parameter	Min	Max	Unit
t25	RXD Setup Before RX_CLK Rising Edge	30	—	ns
t26	RXD Held Past RX_CLK Edge	30	—	ns
t27	RX_CLK Low to CRS Deassertion (at end of received packet)	40	—	ns
t28	TX_EN Setup Before TX_CLK Rising Edge	30	—	ns
t29	TX_EN Held Past TX_CLK Rising Edge	0	—	ns
t30	TXD Setup Before TX_CLK Rising Edge	30	—	ns
t31	TXD Held Past TX_CLK Rising Edge	0	—	ns

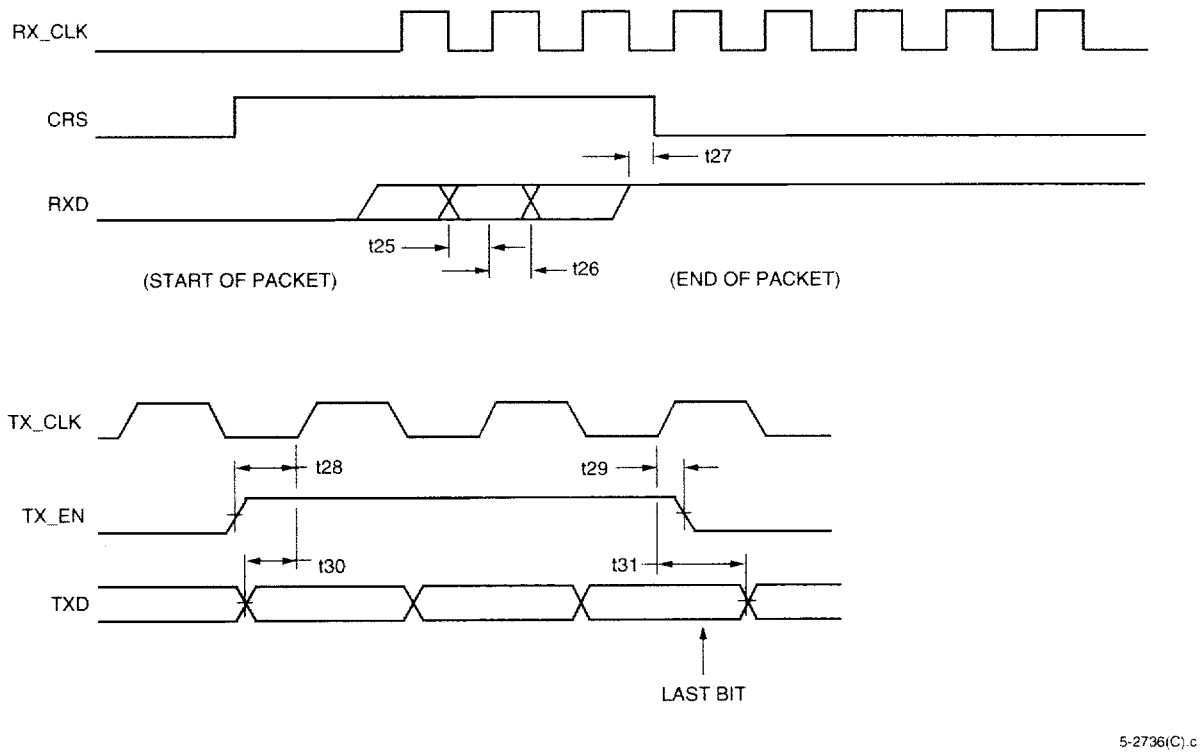
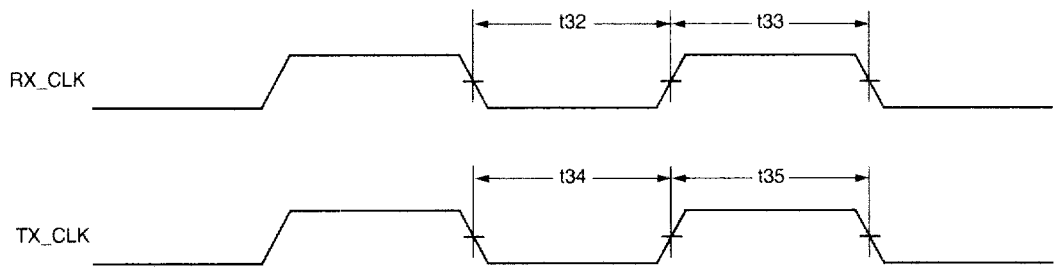


Figure 15. Serial 10 Mbits/s Timing for RX_CLK, CRS, RXD, TX_CLK, TX_EN, and TXD

Timing Characteristics (Preliminary) (continued)

Table 35. Serial 10 Mbits/s Timing for RX_CLK and TX_CLK

Name	Parameter	Min	Max	Unit
t32	RX_CLK Low Pulse Width	45	55	ns
t33	RX_CLK High Pulse Width	45	55	ns
t34	TX_CLK Low Pulse Width	45	55	ns
t35	TX_CLK High Pulse Width	45	55	ns



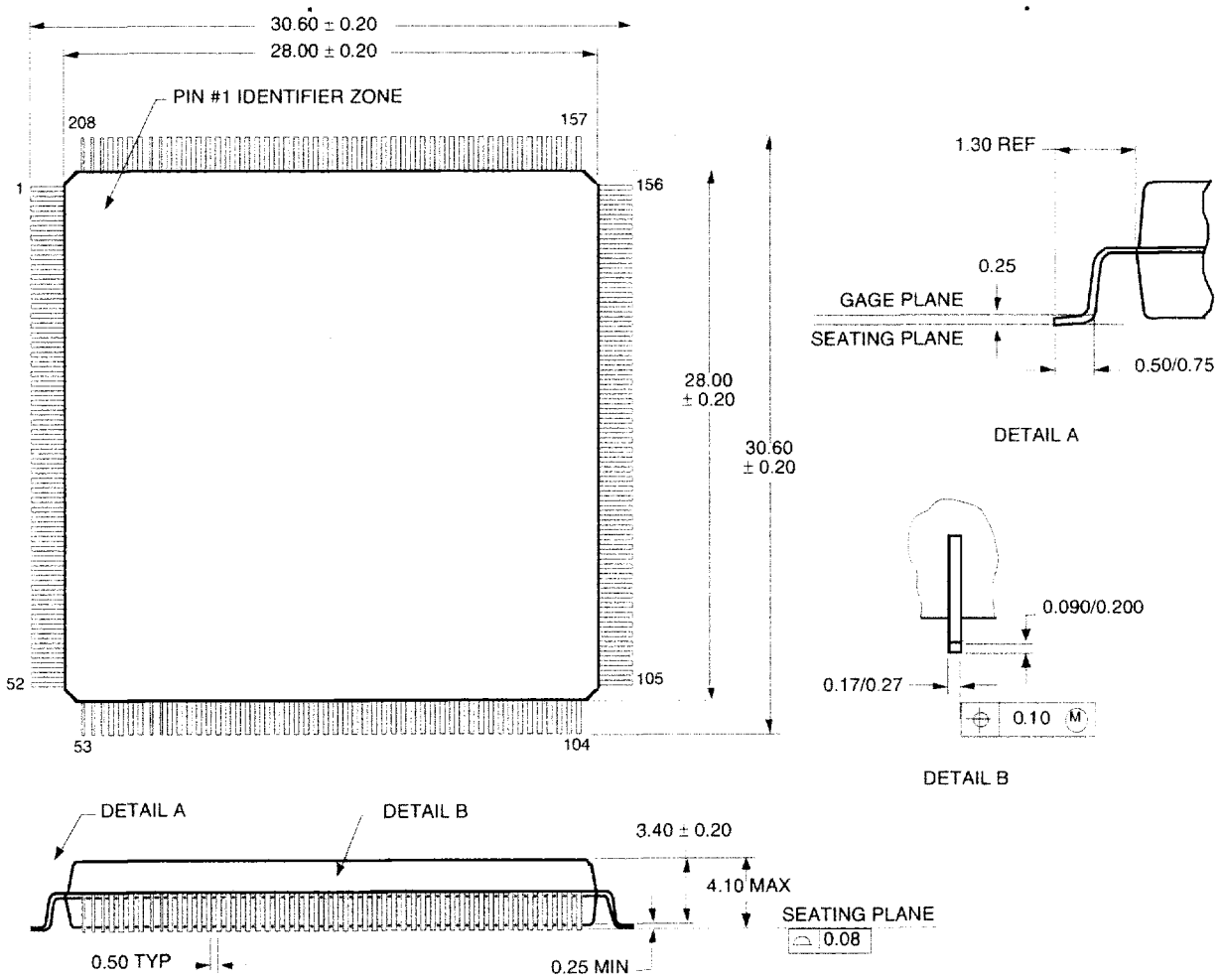
5-2737(C).c

Figure 16. Serial 10 Mbits/s Timing Diagram for RX_CLK and TX_CLK

Outline Diagram

208-Pin SQFP

Dimensions are in millimeters.



Ordering Information

Device Code	Package	Temperature
LU1X54	208-Pin SQFP	0 °C to 70 °C

Revision List

The following are revisions to the *LU1X54 Quad Transceiver* Data Sheet (DS98-354LAN) that have been incorporated into the data sheet.

1. (Table 6, Page 17), MDIO description should have an additional sentence added that says: This pin requires an external 1.5 kΩ pull-up resistor. The LSCLK (pin 87) is a CMOS input not TTL input. The use of clock oscillators with CMOS compatible outputs are necessary. The *Dale** X0-52 and X0-54 series oscillators and the SaRonix NTH/NCH oscillators are TTL and HCMOS compatible.
2. (Figure 5-7, Page 9-11), The BGREF pin is mislabeled in the March 1998 data sheet. It should be pin 25. This will be corrected in the next revision of the data sheet.
3. (Table 8, Page 18), ISET_10 (pin 42) should have a 22.1 kΩ resistor to ground. This will be corrected in the next version of the data sheet.

* *Dale* is a registered trademark of Dale Electronics, Inc.

LU1X54
QUAD Transceiver for 10Base-T

Preliminary Data Sheet
July 1998

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