QuickSwitch® Products
High-Speed CMOS
24-Bit Bus Switch

FEATURES/BENEFITS

- Enhanced N channel FET with no inherent diode to V_{CC}
- 5Ω bidirectional switches connect inputs to outputs
- Zero propagation delay, zero ground bounce
- TTL-compatible input and output levels
- Undershoot clamp diodes on all switch and control pins
- Available in 56-pin SSOP (PV) and TSSOP (PA)
- QS3162211 is 25Ω version for low noise

APPLICATIONS

- Hot-swapping, hot-docking (Application Note AN-13)
- Voltage translation (5V to 3.3V; Application Note AN-11)
- Logic replacement (data processing
- Power conservation
- Capacitance reduction and isolation
- Bus isolation
- Clock gating

DESCRIPTION

The QS316211and QS3162211 each provide a set of twenty-four high-speed CMOS TTL-compatible bus switches. The low on resistance of the QS316211 allows inputs to be connected to outputs without adding propagation delay and without generating additional ground bounce noise. The QS3162211 adds an internal 25Ω series termination resistor to each switch to reduce reflection noise in high speed applications. The device operates as a 24-bit bus switch. When 1OE is low, 1An is connected to 1Bn. When 2OE is low, 2An is connected to 2Bn.

The QS316211 is ideal for switching wide digital buses, 5V to 3.3V translation, and for hot plug buffering.

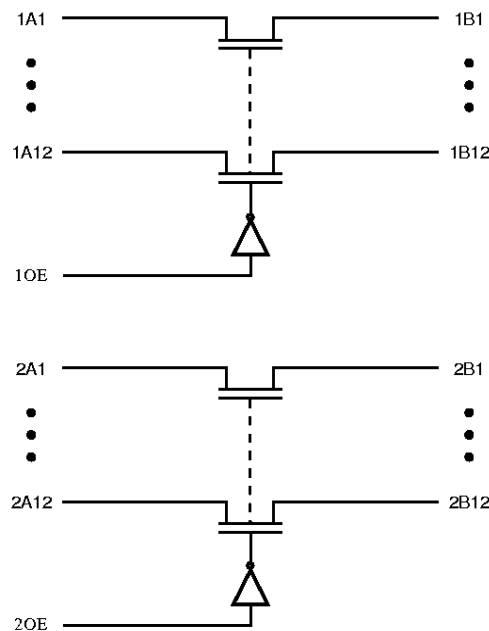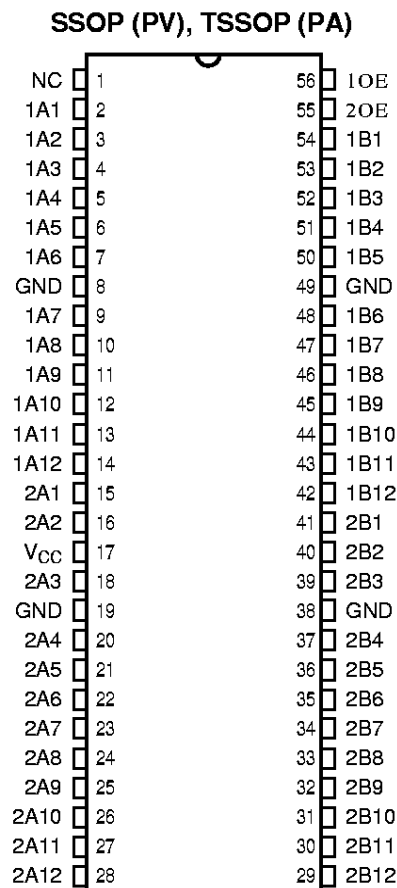## Figure 1. Functional Block Diagram

QUALITY SEMICONDUCTOR, INC.

Table 1. Pin Description

Name	I/O	Function
iA1-iA12	I/O	Bus A
iB1-iB12	I/O	Bus B
1OE-2OE	I	Data select

Table 2. Function Table

1OE	2OE	1An	2An	Function
L	L	1Bn	2Bn	1An to 1Bn, 2An to 2Bn
L	H	1Bn	Z	1An to 1Bn
H	L	Z	2Bn	2An to 2Bn
H	H	Z	Z	Disconnect

Figure 2. Pin Configuration (All Pins Top View)

SSOP (PV), TSSOP (PA)

NC	1	56	1OE
1A1	2	55	2OE
1A2	3	54	1B1
1A3	4	53	1B2
1A4	5	52	1B3
1A5	6	51	1B4
1A6	7	50	1B5
GND	8	49	GND
1A7	9	48	1B6
1A8	10	47	1B7
1A9	11	46	1B8
1A10	12	45	1B9
1A11	13	44	1B10
1A12	14	43	1B11
2A1	15	42	1B12
2A2	16	41	2B1
Vcc	17	40	2B2
2A3	18	39	2B3
GND	19	38	GND
2A4	20	37	2B4
2A5	21	36	2B5
2A6	22	35	2B6
2A7	23	34	2B7
2A8	24	33	2B8
2A9	25	32	2B9
2A10	26	31	2B10
2A11	27	30	2B11
2A12	28	29	2B12

Table 3. Absolute Maximum Ratings

Supply Voltage to Ground .... −0.5V to +7.0V

DC Switch Voltage V_S .... −0.5V to +7.0V

DC Input Voltage V_{IN} .... −0.5V to +7.0V

AC Input Voltage (for a pulse width ≤ 20 ns) .... −3.0V

DC Output Current Max. Sink Current/Pin 120mA

Maximum Power Dissipation At T_A=85°C .... 0.93 watts

T_{STG} Storage Temperature .... −65° to +150°C

Note: ABSOLUTE MAXIMUM CONTINUOUS RATINGS are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum conditions is not implied.

Table 4. Capacitance

T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins	SSOP/TSSOP Typ	Max	Unit
Control Inputs	4.5	6	pF
QuickSwitch Channels (Switch OFF)	5.5	7	pF

Note: Capacitance is characterized but not production tested. For total capacitance while switch is ON, please see Section 1 under "Input and Switch Capacitance."

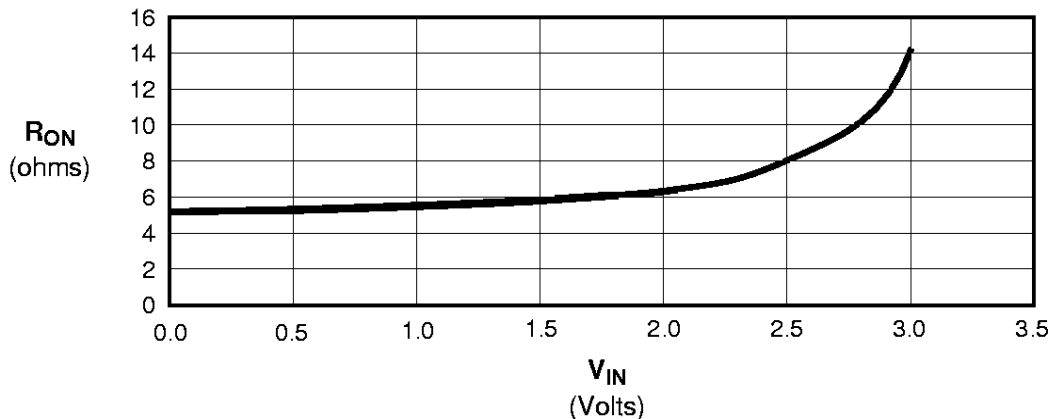## Table 5. DC Electrical Characteristics Over Operating Range

$T_A = -40°C$ to $85°C$, $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions		Min	Typ[1]	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs		2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs		—	—	0.8	V
$|I_{IN}|$	Input Leakage Current (Control Inputs)	$0 \le V_{IN} \le V_{CC}$		—	0.01	1	μA
$|I_{OZ}|$	Off-State Current (Hi-Z)	$0 \le V_{OUT} \le V_{CC}$, Switches Off		—	0.01	1	μA
R_{ON}	Switch ON Resistance[2]	V_{CC} = Min., $V_{IN} = 0.0V$ $I_{ON} = 30mA$	316211	—	4	6	Ω
			3162211	—	28	40	
R_{ON}	Switch ON Resistance[2]	V_{CC} = Min., $V_{IN} = 2.4V$ $I_{ON} = 15mA$	316211	—	8	10	Ω
			3162211	—	35	48	
V_P	Pass Voltage[3]	$V_{IN} = V_{CC} = 5V$, $I_{OUT} = -5μA$		3.7	4	4.2	V

Notes:
1. Typical values indicate $V_{CC} = 5.0V$ and $T_A = 25°C$.
2. For a diagram explaining the procedure for R_{ON} measurement, please see Section 1 under "DC Electrical Characteristics." Max. value R_{ON} guaranteed, but not production tested.
3. Pass Voltage is guaranteed, but not production tested

Figure 3. Typical ON Resistance vs. V_{IN} at $V_{CC} = 5.0V$ (QS316211)

For QS3162211, add 23Ω to R_{ON} shown.

2

Table 6. Power Supply Characteristics Over Operating Range

$T_A = -40°C$ to $85°C$, $V_{CC} = 5.0V \pm 10\%$

Symbol	Parameter	Test Conditions[1]	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}, f = 0	3.0	μA
ΔI_{CC}	Power Supply Current Per Control Input HIGH[2]	V_{CC} = Max., V_{IN} = 3.4V, f = 0	2.5	mA
Q_{CCD}	Dynamic Power Supply Current per MHz[3]	V_{CC} = Max., A and B Pins Open, Control Input Toggling @ 50% Duty Cycle	0.25	mA/ MHz

Notes:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input (V_{IN} = 3.4V). A and B pins do not contribute to ΔI_{CC}.
3. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is guaranteed, but not tested.

Table 7. Switching Characteristics Over Operating Range

$T_A = -40°C$ to $85°C$, $V_{CC} = 5.0V \pm 10\%$
$C_{LOAD} = 50pF$, $R_{LOAD} = 500\Omega$ unless otherwise noted.

Symbol	Description[1]	QS316211			QS3162211			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{PLH} t_{PHL}	Data Propagation Delay[2,3] iAn to iBn, iBn to iAn	—	—	0.25[3]	—	—	1.25[3]	ns
t_{PZL} t_{PZH}	Switch Turn-on Delay nOE to iAn, iBn	1.5	—	6.5	1.5	—	7.5	ns
t_{PLZ} t_{PHZ}	Switch Turn-off Delay[2] nOE to iAn, iBn	1.5	—	6.2	1.5	—	6.8	ns

Notes:
1. See Test Circuit and Waveforms. Minimums guaranteed but not production tested.
2. This parameter is guaranteed but not production tested.
3. The time constant for the switch alone is of the order of 0.25ns for QS316211 and 1.25ns for QS3162211 for $C_L = 50pF$. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.