Preliminary Data Sheet
August 1995

AT&T Microelectronics

ATT2X02 100VG Twisted-Pair Transceiver Chip CMOS Integrated Circuit

Features

- Supports the *IEEE** 802.12 100VG-AnyLAN specification.
- Enables 100 Mbits/s transmissions over 10Base-T wiring installations (bundled or unbundled) when used in combination with AT&T Microelectronics' ATT2MD12 MAC and PCI System Interface IC or the ATT2R02 Repeater IC.
- Provides for complete 100VG-AnyLAN control signal generation and reception supporting two levels of priority needed for bounded latency networking for multimedia and other time-sensitive applications.
- Complete implementation of the 100VG-AnyLAN Quartet Signaling physical layer function.
  - — Four transceivers provide 100 Mbits/s connectivity to one voice-grade cable consisting of four twisted pairs.
  - — Receiver circuitry with adaptive equalization phase-lock loops, automatic gain control (AGC), data justifier, and energy detectors ensure bit error rates equivalent to 10Base-T.
  - — On-chip drivers minimize component count and facilitate FCC compliance by simplifying board layout.
- Receive enable signal allows for 3-stating the receive inputs which enables transceivers for other media to be easily multiplexed.
- Fabricated in a low-power CMOS technology requiring a single 5 V supply in a 44-pin chip carrier.
- Demonstration kits are available for the ATT2MD12 (ATT2MD12-DP) and ATT2R02 (ATT2R02-DH) and all utilize the ATT2X02.

Description and Applications

The ATT2X02 is a CMOS Integrated Circuit implementing the physical layer function of the *IEEE* 802.12 standard for 100 Mbits/s data transmission in local area networks (LAN). The ATT2X02 implements the Quartet Signaling technology in a single integrated circuit, enabling reliable data transmission at 100 Mbits/s over voice-grade twisted-pair cabling.

The ATT2X02 is a versatile building block for 100VG-AnyLAN systems and is suitable for use in the following applications:

- Managed or unmanaged hubs
  - — Stackable
  - — Rack mounted
  - — Stand-alone
- Adapter cards
- Motherboards
- Workstations
- Fileservers
- Network analyzers
- LAN test equipment
- Bridges
- Routers

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Description and Applications (continued)

The ATT2X02 provides a direct synchronous interface to either the ATT2MD12 MAC and PCI System Interface or the ATT2R02 Repeater IC. A block diagram is shown in Figure 1. The ATT2X02 Transceiver Chip contains four TP transmitters and four TP receivers. The transmit control state (TCS) machine passes data from the media access controller (MAC) to the twisted-pair lines and generates control signals (CS) to indicate the current transmit control state. The receive control state (RCS) machine decodes control signals and indicates the detected control states on RCS[2:0] and RXGRANT. The control block provides the reset and test interface. The TP driver block contains four independent differential twisted-pair drivers. The twisted-pair receive block (TPREC) contains four equalizers, four PLLs, two energy detect circuits, four slicers, and a channel justifier circuit.

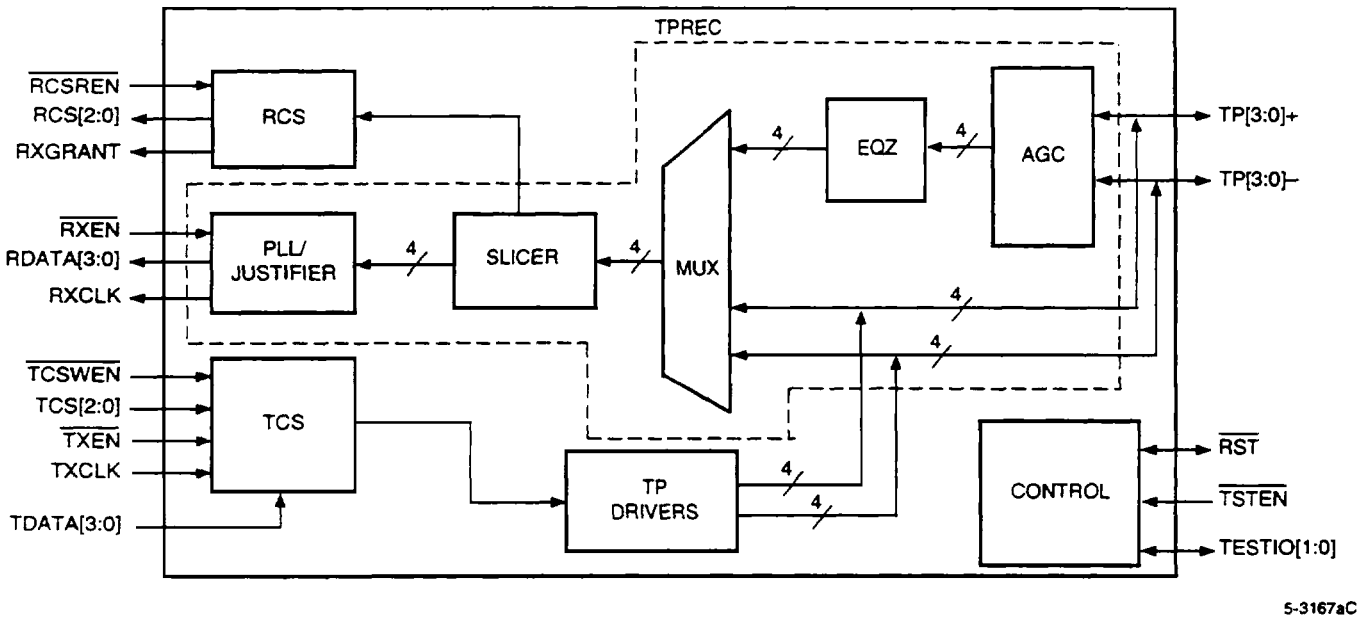

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Figure 1. Functional Block Diagram

Pin Information

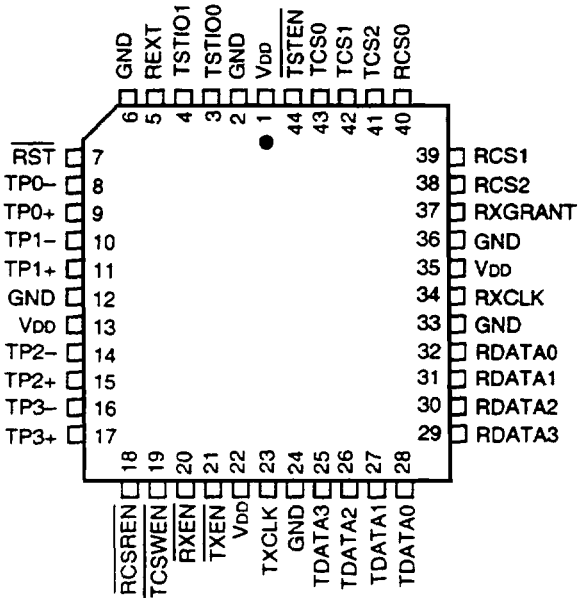

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Figure 2. Pin Diagram

Pin Information (continued)

Table 1. Pin Descriptions

Pin	Symbol	I/O	Active	Description
1, 13, 22, 35	V_{DD}	—	—	**Power.** 5 V ± 5% supply.
2, 6, 12, 24, 33, 36	GND	—	—	**Ground.**
3	TSTIO0	I/O	—	**Test Input/Output 0.** This pin is used for testing internal nodes. It should be left unconnected.
4	TSTIO1	I/O	—	**Test Input/Output 1.** This pin is used for testing internal nodes. It should be left unconnected.
5	REXT	—	—	**External Bias Resistor.** A 24.9 kΩ (±1%) resistor should be connected between this pin and ground. Parasitic loading should not exceed 15 pF.
7	$\overline{RST}$	I/O	L	**Reset.** Full chip reset. The on-chip power-on reset circuit is also connected to this pin via a small open-drain N-channel MOSFET to provide a reset output signal to external circuits if desired. $\overline{RST}$ must be asserted for >100 ns but can be asynchronous. All transceiver activity is inhibited for 1 ms after $\overline{RST}$ is deasserted. Standard CMOS levels.
8	TP0–	I/O	—	**TP Port 0–.** Twisted-pair driver/receiver negative circuit 0. Energy detect is performed on TP1 and TP0. Control signals are received on TP[1:0]. Control signals are transmitted on TP[3:2]. Data is transmitted and received on TP[3:0] (see Figure 15 for timing).
9	TP0+	I/O	—	**TP Port 0+.** Twisted-pair driver/receiver positive circuit 0.
10	TP1–	I/O	—	**TP Port 1–.** Twisted-pair driver/receiver negative circuit 1.
11	TP1+	I/O	—	**TP Port 1+.** Twisted-pair driver/receiver positive circuit 1.
14	TP2–	I/O	—	**TP Port 2–.** Twisted-pair driver/receiver negative circuit 2.
15	TP2+	I/O	—	**TP Port 2+.** Twisted-pair driver/receiver positive circuit 2.
16	TP3–	I/O	—	**TP Port 3–.** Twisted-pair driver/receiver negative circuit 3.
17	TP3+	I/O	—	**TP Port 3+.** Twisted-pair driver/receiver positive circuit 3.
18	$\overline{RCSREN}$	I	L	**Receive Control State Read Enable.** RCS[2:0] and RXGRANT lines are active when $\overline{RCSREN}$ is asserted, and they are 3-stated when $\overline{RCSREN}$ is deasserted. Standard CMOS input.
19	$\overline{TCSWEN}$	I	L	**Transmit Control State Write Enable.** TCS[2:0] lines are latched on the next rising edge of TXCLK following the assertion of $\overline{TCSWEN}$. See Figure 14 for more details. Standard CMOS input.
20	$\overline{RXEN}$	I	L	**Receive Enable.** When $\overline{RXEN}$ is asserted, the transceiver enters the receive mode, RDATA[3:0] and RXCLK are held low until all PLLs have completed acquisition, at which time RDATA[3:0] becomes active and RXCLK begins to transition as the recovered clock. See Figure 11 for more details. Standard CMOS input.
21	$\overline{TXEN}$	I	L	**Transmit Enable.** When $\overline{TXEN}$ is asserted, the transceiver enters the transmit mode and data on TDATA[3:0] is transmitted serially on the TP media synchronized to TXCLK. Actual data transmission is delayed until media dc balance is achieved with appropriate control signals. See Figure 12 for more details. Standard CMOS input.
23	TXCLK	I	—	**Transmit Clock.** 30 MHz ± 100 ppm at end of life. 40%—60% duty cycle. Clock must be present at all times during operation. Standard CMOS input.

Pin Information (continued)

Table 1. Pin Descriptions (continued)

Pin	Symbol	I/O	Active	Description
25	TDATA3	I	—	**Transmit Data 3.** Data transmitted serially on the TP media through TP0 when $\overline{\text{TXEN}}$ is asserted. See Figure 12 for more details. Standard CMOS input.
26	TDATA2	I	—	**Transmit Data 2.** Data transmitted serially on the TP media through TP1 when $\overline{\text{TXEN}}$ is asserted. Standard CMOS input.
27	TDATA1	I	—	**Transmit Data 1.** Data transmitted serially on the TP media through TP2 when $\overline{\text{TXEN}}$ is asserted. Standard CMOS input.
28	TDATA0	I	—	**Transmit Data 0.** Data transmitted serially on the TP media through TP3 when $\overline{\text{TXEN}}$ is asserted. Standard CMOS input.
29	RDATA3	O	—	**Receive Data 3.** Received serial data recovered from the TP media through TP3. It is synchronous to RXCLK. See Figure 11 for more details. Active when $\overline{\text{RXEN}}$ is asserted; 3-stated when $\overline{\text{RXEN}}$ is deasserted. 3-state output. Standard CMOS output.
30	RDATA2	O	—	**Receive Data 2.** Received serial data from TP2. Standard CMOS output.
31	RDATA1	O	—	**Receive Data 1.** Received serial data from TP1. Standard CMOS output.
32	RDATA0	O	—	**Receive Data 0.** Received serial data from TP0. Standard CMOS output.
34	RXCLK	O	—	**Receive Clock.** Recovered clock from data on TP media. RXCLK is driven when $\overline{\text{RXEN}}$ is asserted. It is held low until all four on-chip PLLs have completed acquisition. RXCLK is phase-aligned to channel 0 data. RXCLK is 3-stated when $\overline{\text{RXEN}}$ is deasserted. RXCLK has a 40%—60% duty cycle with a nominal 33.3 ns period (30 MHz). Cycle-to-cycle jitter on RXCLK is less than ±2 ns. Standard CMOS output.
37	RXGRANT	O	—	**RXGRANT.** When asserted, it indicates that a condition of silence has been detected on the link. Synchronous with the rising edge of TXCLK. Valid when $\overline{\text{RCSREN}}$ is asserted. 3-stated otherwise. Standard CMOS output.
38	RCS2	O	—	**Receive Control State Data 2.** RCS data indicates the control state of the link. RCS is synchronous with TXCLK and is valid when $\overline{\text{RCSREN}}$ is asserted. 3-stated otherwise (see Table 3). Standard CMOS output.
39	RCS1	O	—	**Receive Control State Data 1** (see Table 3). Standard CMOS output.
40	RCS0	O	—	**Receive Control State Data 0** (see Table 3). Standard CMOS output.
41	TCS2	I	—	**Transmit Control State Data 2.** TCS data is synchronous to TXCLK and loaded when $\overline{\text{TCSWEN}}$ is valid. See Table 5 for more details. TCS[2:0] indicates which control signal is to be transmitted. Standard CMOS input.
42	TCS1	I	—	**Transmit Control State Data 1.** When $\overline{\text{TCSWEN}}$ and $\overline{\text{TSTEN}}$ are both asserted, TCS1 = high signals the part to go into chip-to-board contact test mode. See Tables 6 and 7 for more details. Standard CMOS input.
43	TCS0	I	—	**Transmit Control State Data 0.** When $\overline{\text{TCSWEN}}$ and $\overline{\text{TSTEN}}$ are both asserted, setting TCS0 = 1 resets the part. Standard CMOS input.
44	$\overline{\text{TSTEN}}$	I	L	**Test Register Write Enable.** Writing to the test register is enabled when $\overline{\text{TSTEN}}$ is asserted low. For normal system operation, this signal should be pulled high through a 4.6 kΩ resistor. This test mode is for manufacturing testing only. Standard CMOS input.

Pin Information (continued)

Data transfer in the ATT2X02 is dependent on $\overline{\text{RXEN}}$ and $\overline{\text{TXEN}}$. The ATT2X02 operates in the following four primary modes as described in this table. Note crossovers shown in Figure 3.

Table 2. Data Transfer Definition

$\overline{\text{RXEN}}$ = Deasserted; $\overline{\text{TXEN}}$ = Deasserted; Mode = Control Decode	$\overline{\text{RXEN}}$ = Asserted, Preamble Not Detected; $\overline{\text{TXEN}}$ = Deasserted; Mode = Preamble Waiting	$\overline{\text{RXEN}}$ = Asserted, Preamble Detected; TXEN = Deasserted; Mode = TP Receive	$\overline{\text{RXEN}}$ = Deasserted; $\overline{\text{TXEN}}$ = Asserted; Mode = TP Transmit
Control signal > in TP[0:1] Control signal > out TP[2:3]	Control signal > in TP[0:1] Silence > out TP[2:3]	TP0 > RDATA0 TP1 > RDATA1 TP2 > RDATA2 TP3 > RDATA3	TDATA0 > TP3 TDATA1 > TP2 TDATA2 > TP1 TDATA3 > TP0

Block Description

This is a brief description of major blocks of the ATT2X02.

RCS

The receive control state (RCS) machine decodes control signal information sent by the opposite node on the two twisted pairs TP[0] and TP[1]. Table 3 defines the RCS outputs according to the control signals received on TP[0] and TP[1].

The RCS logic is clocked by TXCLK. Its purpose is to decode control states from received low-frequency control signals and then indicate the control state on RCS[2:0]. In addition, the RCS logic also detects the condition of silence on the link and asserts RXGRANT. The RCS logic implements the receive function state diagram shown in Figure 16 (located in Appendix A).

The control signals received on TP[1:0] correspond to control signals transmitted on TP[2:3] by the opposite transceiver. A crossover on the TP media is implied as shown in Figure 3.

The four output signals, RCS[2:0] and RXGRANT, are all synchronous to the rising edge of TXCLK. RCS[2:0] indicate the control signal recognized by the RCS machine. RXGRANT indicates that silence has been detected on TP[0] and TP[1]. When RXGRANT is asserted, RCS[2:0] is latched in the last known state. When $\overline{\text{TXEN}}$ is asserted, RXGRANT is deasserted and the RCS state machine enters the transmit path shown in Figure 16. If $\overline{\text{TXEN}}$ is not asserted before the fault timer times out, then RCS enters the LINK WARNING state and RCS is set to 111.

When $\overline{\text{RXEN}}$ is asserted, the RCS state machine enters the receive path, RXGRANT is deasserted, and RXCLK and RDATA [3:0] are enabled and driven low. RCS continues to decode control signals until PREAMBLE is detected. When PREAMBLE is detected, RCS[2:0] is set to 000 and the receive clock recovery circuitry is enabled. When a valid clock has been recovered, RDATA [3:0] and RXCLK are present at the transceiver pins. While $\overline{\text{RXEN}}$ is asserted, RCS monitors the transition density of the received data to ensure that the data being received appears to be valid 5B/6B encoded NRZ data. When $\overline{\text{RXEN}}$ is deasserted from either the CLOCK RECOVERY STATE or the DATA DECODE state, RCS[2:0] is set to 000. If, during DATA DECODE, the received data is not valid, e.g., the transceiver sees control signals, RCS[2:0] are set to 000 and the RCS state machine enters the NOT_DATA state. It remains in this state until $\overline{\text{RXEN}}$ is deasserted. During this time, the transceiver continues to decode and provide RDATA and RXCLK.

Block Description (continued)

RCS (continued)

Control signals are detected by counting the number of TXCLK cycles between edges on TP[0] and TP[1]. A count of 6 to 10 is interpreted as a CS2, and a count of 14 to 18 is interpreted as CS1. Other counts are ignored and do not alter RCS[2:0].

Table 3. Relationship of Receive Control State (RCS) Code, Control Signals, and Receive Control Names

RCS[2:0]	TP1	TP0	Received Control State Interpretation*
000	X†	X†	Mode Transition
001	CS1	CS1	Idle Down or Idle Up
010	CS1	CS2	Incoming or Request Normal
011	CS2	CS1	Enable High Only or Request High
100	CS2	CS2	Training Down or Training Up
101	Data On Link	Data On Link	Data On Link
110	Reserved	Reserved	Reserved
111	X†	X†	Link Warning

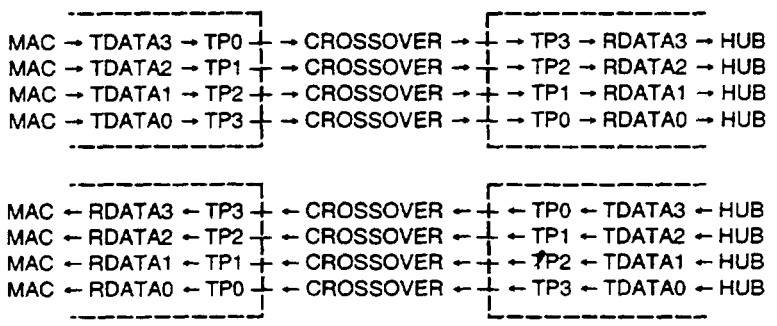
* The interpretation of the RCS information depends upon whether the transceiver is an end-node or a repeater. The interpretation in this table is provided for information purposes only.

† X indicates that this RCS code depends on factors other than the received control signal pairs; refer to Figure 16 for details.

Block Description (continued)

RCS Notes

- Grant: The control state that indicates that the repeater has granted the end node permission to send a packet. Grant is a separate code used in conjunction with the receiver control state.
- Receiver Control States: Indicate either the current or previous control state, depending on the grant state.
  — If grant_state = 0, the receiver_control_state represented by the RCS code value indicates the current control state received at the MDI.
  — If grant_state = 1, the receiver_control_state represented by the RCS code value indicates the control state received at the MDI prior to grant being decoded.
- Mode Transition: The receiver control state used by the PMD to indicate that the signals on the link are in transition between data and control modes.
- Idle_Down: Indicates that the repeater currently has no packet that is destined for the end node.
- Idle_Up: Indicates that the end node is in the idle state and is not requesting to send a packet. Its presence enables the receiver to determine that the line is connected.
- Incoming: The control state used by a repeater to alert the end node that a packet may be incoming. A node receiving incoming will release control of its control signals when incoming is detected.
- Request_High and Request_Normal: The transmit control states used by the end node to inform the repeater that it wishes to send a packet.
  — Request_High indicates that a high-priority packet needs to be sent.
  — Request_Normal indicates that a normal-priority packet needs to be sent.
- Enable High Only: A link control signal from an upper repeater to a lower repeater preempting a lower repeater's normal priority round-robin cycle.
- Training_Up: Indicates that link training is desired or is continuing.
- Data_On_Link: The receiver control state used by the PMD to indicate that data streams (rather than control signals) are being received from the link.
- The reserved state is an illegal condition.
- Link_Warning: The receiver control state used by the PMD to indicate a condition that may require the link to be retrained.
- A link warning is issued when the RCS fault timer expires (between 1 ms and 2 ms).



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Note: Everything within the dashed lines is in the ATT2X02; the crossover is external.

Figure 3. Crossover

Block Description (continued)

TCS

The transmit control state (TCS) state machine generates the low-frequency control signals which are transmitted on TP[2] and TP[3] to indicate the state of the link. These signals are transmitted as defined by the state of the TCS[2:0] control pins, whenever $\overline{\text{TXEN}}$ and $\overline{\text{RXEN}}$ are not asserted. This circuitry implements the transmit function state machines shown in Appendix A, Figures 16, 17, and 18. When $\overline{\text{TXEN}}$ is asserted, the data presented on TDATA[3:0] is passed through to TP[3:0] (note that there is a crossover as shown in Figure 3), after dc balance is reached by the control signals. When $\overline{\text{RXEN}}$ is asserted, all of the twisted-pair output drivers are disabled.

The TCS encodes control signals and transmits them with a combination of CS1, CS2 (control signals 1 and 2), and SILENCE. The control signals are shown in Table 4 for reference.

Table 4. Control Signal Patterns

CSn	HCSa	HCSb
CS1	1111111100000000	0000000011111111
CS2	11110000	00001111

When encoded and transmitted as NRZ data at 30 MBaud, CS1 has a fundamental frequency of 0.9375 MHz and CS2 has a fundamental frequency of 1.875 MHz.

Transitions between control signals are accomplished such that an HCSa pattern is always followed by an HCSb pattern and an HCSb pattern is always followed by an HCSa pattern and that equal numbers of 1s and 0s are always transmitted on TP[2] and TP[3]. This ensures that dc balance is maintained on the link.

Transitions from control signals to data transmissions are accomplished by discarding preamble bits until a point of dc balance is reached. No more than 20 preamble bits are discarded.

Table 5 shows the relationship between the TCS inputs and the control signals transmitted on TP[3] and TP[2].

Table 5. TCS Mapping

TCS[2:0]	TP2	TP3	Transmit Control State Interpretation*
000	X†	X†	Disable.
001	CS1	CS1	Idle up or idle down.
010	CS1	CS2	Request normal or incoming.
011	CS2	CS1	Request high or enable high only.
100	CS2	CS2	Training up or training down.
101	—	—	Reserved.‡
110	—	—	Reserved.‡
111	X†	X†	Disabled (disabled TP transmitters).

* In general, the interpretation of the TCS information depends upon whether the transceiver is an end node or a repeater. The interpretation in this table is provided for information purposes only. See RCS notes for control state definitions.

† X indicates that the twisted-pair transmitters are disabled (even if TXEN is asserted).

‡ The two reserved codes are unassigned control states. Selecting one of these codes will cause the transmission of control signal patterns that may not be properly interpreted by the receiving node.

Block Description (continued)

TCS (continued)

Table 6 shows the alternate test usage of the TCS[2:0] pins.

Table 6. Alternative Test Usage States of the TCS[2:0] Pins (activated by asserting $\overline{\text{TSTEN}}$ and $\overline{\text{TCSWEN}}$)

State TCS[2:0]	Name	Description
000	NA	Reserved, do not use.
001	Software Reset	Full reset, comparable to chip reset (RST).
010	Contact Test	Chip-to-board contact test. This test mode is not self-resetting; test mode is maintained until the chip reset ($\overline{\text{RST}}$) is asserted (see Table 7.).
011	NA	Reserved.
100	NA	Reserved.
101	NA	Reserved.
110	NA	Reserved.
111	NA	Reserved.

During pin mapping modes, the RCS[2:0], and RXGRANT signals are clocked out by the rising edge of TXCLK. When $\overline{\text{RXEN}}$ and $\overline{\text{TXEN}}$ are asserted, TP[3:0] are disabled.

Table 7. Pin Mapping During Contact Test

Input	Output
TXCLK	RXCLK
TDATA[3:0]	RDATA[3:0]
TDATA[3:0]	TP[3:0]+ and TP[3:0]–
$\overline{\text{TCSWEN}}$ XOR $\overline{\text{RCSREN}}$	TSTIO1
TCS[2:0]	RCS[2:0]
$\overline{\text{TXEN}}$	RXGRANT
$\overline{\text{RXEN}}$	REXT
$\overline{\text{TSTEN}}$	TSTIO0

Block Description (continued)

Control

The control block provides reset and the test interfaces. For more information, see Tables 6 and 7 and the $\overline{\text{RST}}$ pin description.

Control Notes

- There is an on-chip generated power-on reset signal connected internally over an open-drain N-channel transistor to the $\overline{\text{RST}}$ pin to provide a reset output signal to external circuits if desired. During a software reset, the $\overline{\text{RST}}$ pin is not activated.
- $\overline{\text{RST}}$ may be asynchronous to TXCLK.
- The transceiver inhibits transmission or reception until 1 ms after reset is deasserted.
- When $\overline{\text{TSTEN}}$ is asserted and $\overline{\text{TCSWEN}}$ is asserted, TCS[2:0] performs the functions of Table 6 on the rising edge of TXCLK.

TP Drivers

The transmit driver block contains four independent differential twisted-pair drivers. Each single-ended half of a TP output consists of a CMOS driver in series with a resistor. The resistor is connected between the output of the CMOS driver and the output pin. The value of this resistor is chosen to give a differential output impedance of 50 Ω when looking from the two output pins of the TP port into the chip. The TP CMOS drivers are 3-stated and disabled in the receive mode, and the two series resistors corresponding to one TP driver are connected in series via a transmission gate in order to form the 50 Ω differential receive input impedance (see Figure 4). When disabled, the TP driver is not receiving or transmitting; the 50 Ω differential line impedance is maintained.

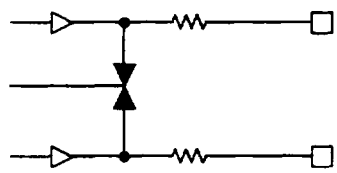

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Figure 4. TP Driver

TPREC

The twisted-pair receiver block contains four equalizers, four PLLs, two energy detect circuits, a channel justifier circuit, and a slicer.

The channel justifier aligns the four serial data streams to a single recovered clock (RXCLK), and it ensures that the data bits are always assigned to the same RXCLK window for such a packet. However, the justifier does not align bits back into their original bit cell at the transmit site.

Application

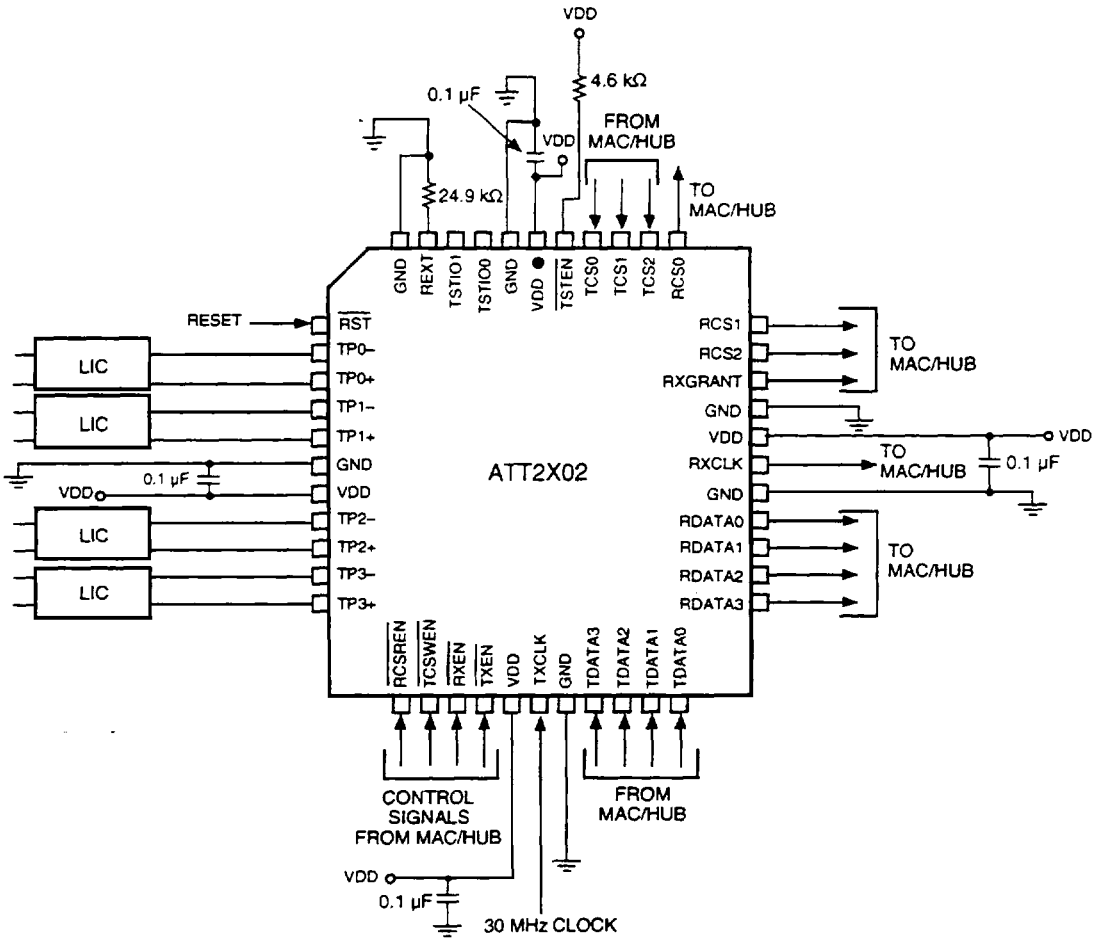

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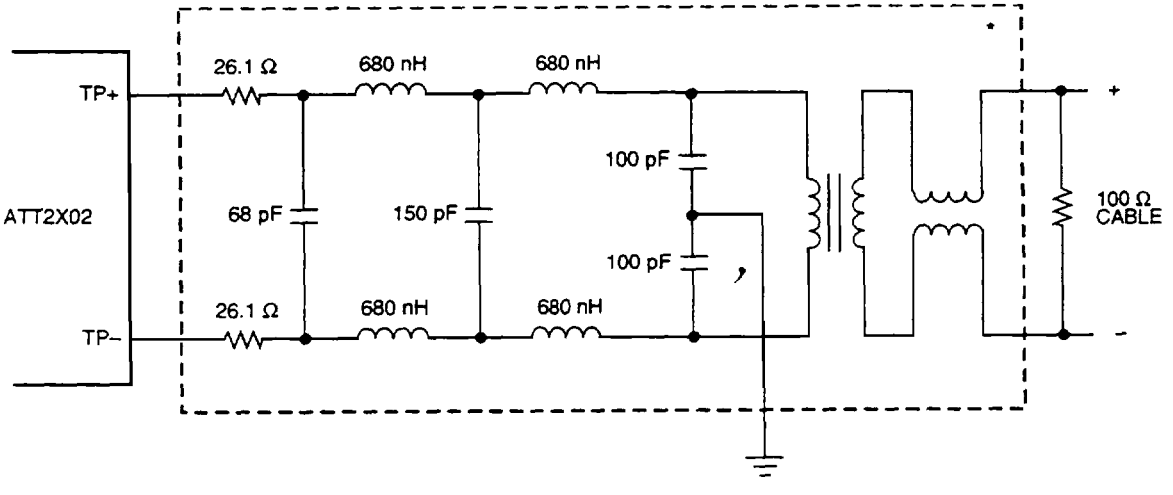
Figure 5. Typical Configuration



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*Integrated filter and magnetics modules are available from various vendors.

Figure 6. Line Interface Circuit (LIC)

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect the device reliability.

Table 8. Maximum Ratings

Parameter	Symbol	Min	Max	Units
Maximum Supply Voltage	V_{DD}	—	5.5	V
Signal Pin Voltage	—	–0.5	V_{DD} + 0.5	V
Ambient Operating Temperature with 200 FPM Airflow	T_A	0	70	°C
Ambient Storage Temperature	T_{stg}	–40	125	°C

Electrical Characteristics

The following specifications apply for V_{DD} = 5 V ± 5%.

Table 9. Twisted-Pair Input Characteristics (TP[3:0]) (See Figure 7.)

Parameter	Conditions	Min	Typ	Max	Units
Differential Input Resistance	Measured at pins	35	50	65	Ω
Differential Input Capacitance	Measured at pins	2	15	20	pF
Peak Differential Squelch Voltage	Measured at pins	185	215	245	mV

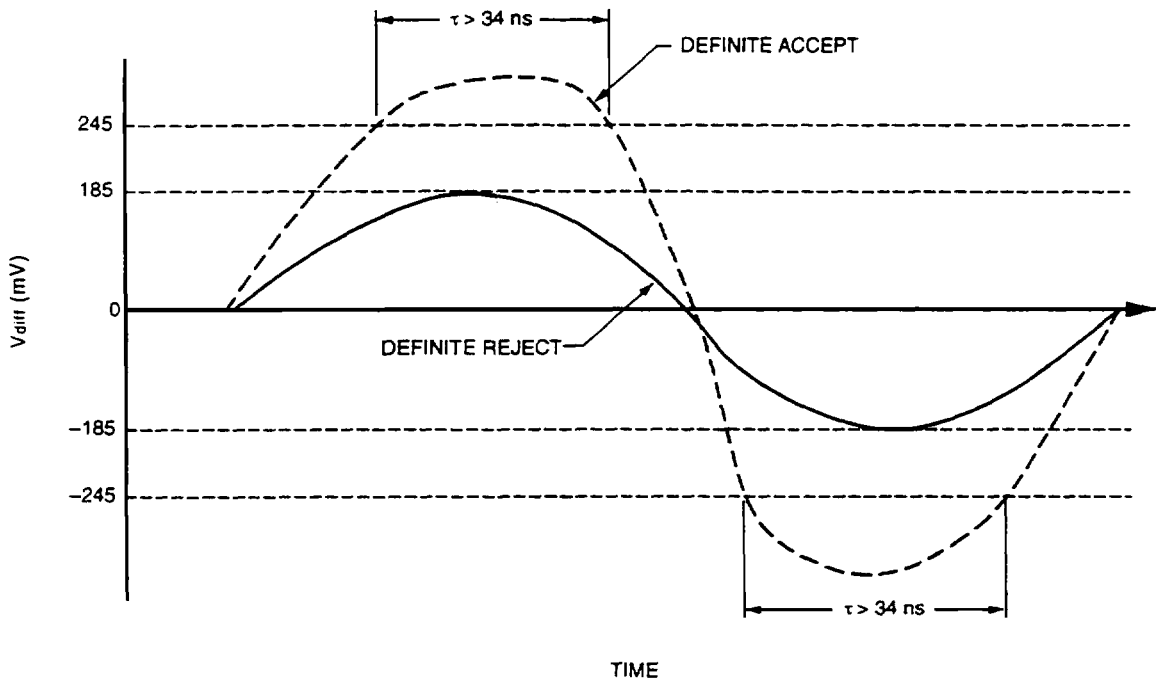

Figure 7. Squelch Levels and Timing

Electrical Characteristics (continued)

Table 10. Twisted-Pair Output Characteristics (TP[3:0]) (See Figure 8.)

Parameter	Conditions	Min	Typ	Max	Units
Output dc Source Resistance (differential)	—	40	50	60	Ω
Output dc Current (short circuit)	Load: 50 Ω external	—	—	65	mA
Output Rise/Fall Time (differential)	Load: 150 Ω/20 pF 10% to 90%	0.25	—	8.0	ns
Output Voltage	Load: 150 Ω	3.4	3.8	4.2	V
Differential Pair Skew	—	—	—	2.0	ns
Peak Common-mode Output Voltage	—	—	—	500	mV

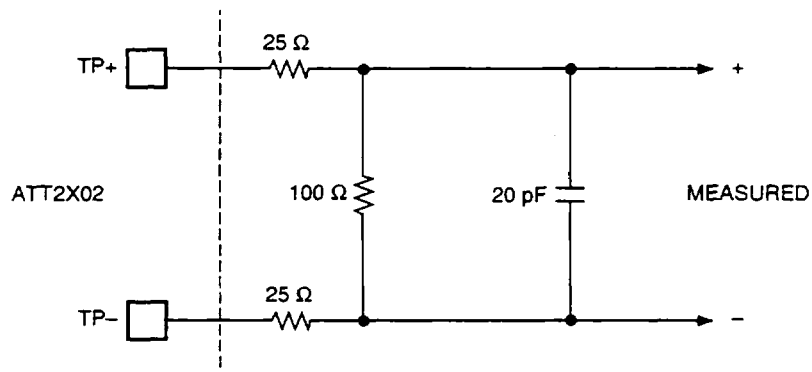

Figure 8. TP Output Test Load

Electrical Characteristics (continued)

Table 11. Digital Output Pins (RCS[2:0], RXGRANT, RData[3:0], RXCLK) (See Figure 9.)

Parameter	Conditions	Min	Typ	Max	Units
Output dc Source Resistance	—	—	33	50	Ω
Output dc Current	50 pF load	—	—	10	mA
Output Rise/Fall Time	10 pF to 50 pF load, 2 kΩ pull-up (See Figure 10.)	1	—	6	ns
V_{OH}	Sourcing 10 mA	V_{DD} – 0.5	—	—	V
V_{OL}	Sinking 10 mA	—	—	0.5	V

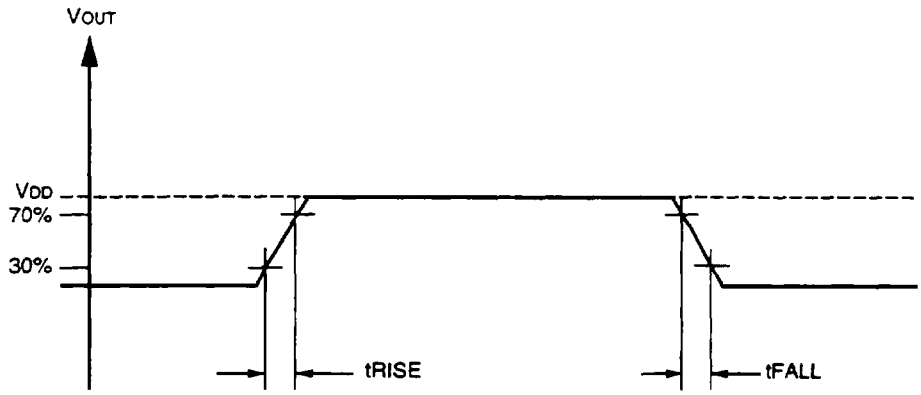

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Figure 9. Digital Rise/Fall Times

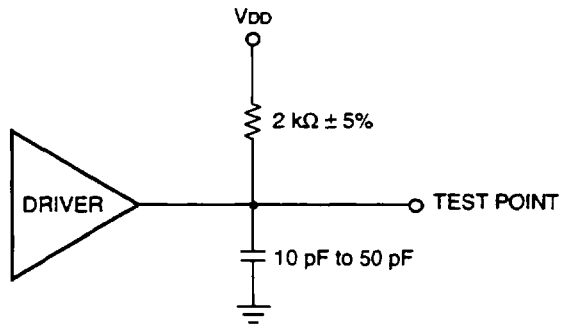

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Figure 10. MII Output Driver Test Load

Electrical Characteristics (continued)

Table 12. Regular CMOS Input

Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	—	V_{DD} – 1	—	—	V
V_{IL}	—	—	—	1	V
Input Leakage Currents	—	—	—	10	µA
Input Capacitance	—	—	—	5	pF
Input Rise/Fall Time	30%—70%	—	—	5	ns

Table 13. Open-Drain Output ($\overline{RST}$)

Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	—	V_{DD} – 1	—	—	V
V_{IL}	—	—	—	1	V
Output dc Current	—	—	—	5	mA
Output dc Source Resistance	Output shorted to positive supply	—	200	—	Ω

Table 14. dc Power Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Positive Supply Voltage	—	4.75	—	5.25	V
Transmit Mode Supply Current	—	—	—	285	mA
Receive Mode Supply Current	—	—	—	220	mA
Line Control Signals Mode Supply Current	—	—	—	210	mA
Average Power Dissipation	—	—	—	1000	mW

Timing Characteristics

Table 15. RDATA Timing (See Figure 11.)

Symbol	Parameter	Min	Max	Unit
tRNLTCH	Setup Time $\overline{\text{RXEN}}$ to Rising Edge of TXCLK	7	—	ns
tTPVRDV	Time from Preamble Until RDATA and RXCLK Are Valid	10	23	BT*
tTPVRCH	Time from Preamble Until RXCLK Is Active	10	23	BT*
tRNLRCL	Time from $\overline{\text{RXEN}}$ Until RXCLK and RDATA Driven	—	15	ns
tRCHRDV	Data Valid After RXCLK High	3	20	ns
tRNHRCZ	Time from $\overline{\text{RXEN}}$ Deasserted Until RXCLK and RDATA Are High Impedance	—	15	ns
tRNLTPV	Time Before Preamble $\overline{\text{RXEN}}$ Must Be Asserted	6	—	BT*
tRNHRNL	Minimum Time $\overline{\text{RXEN}}$ Must Be Deasserted	530	—	ns

* BT = bit times.

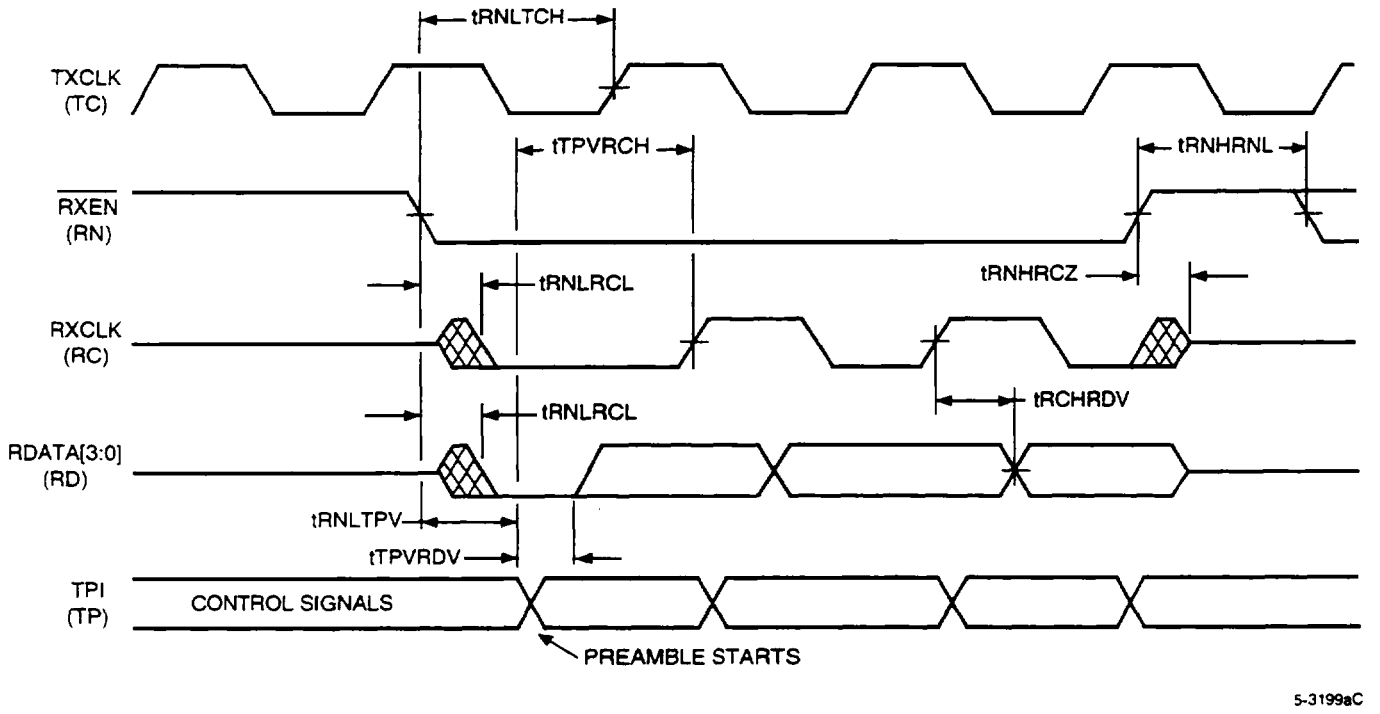


Figure 11. RDATA Timing

Timing Characteristics (continued)

Table 16. TDATA Timing (See Figure 12.)

Symbol	Parameter	Min	Max	Unit
tTNLTCH	Setup Time $\overline{\text{TXEN}}$ to Rising Edge of TXCLK	7	—	ns
tTDVTCH	Setup Time TDATA[3:0] to Rising Edge of TXCLK	7	—	ns
tTCHTNH	Hold Time for $\overline{\text{TXEN}}$ from Rising Edge of TXCLK	2	—	ns
tTCHTDV	Hold Time for TDATA[3:0] for Rising Edge of TXCLK	2	—	ns

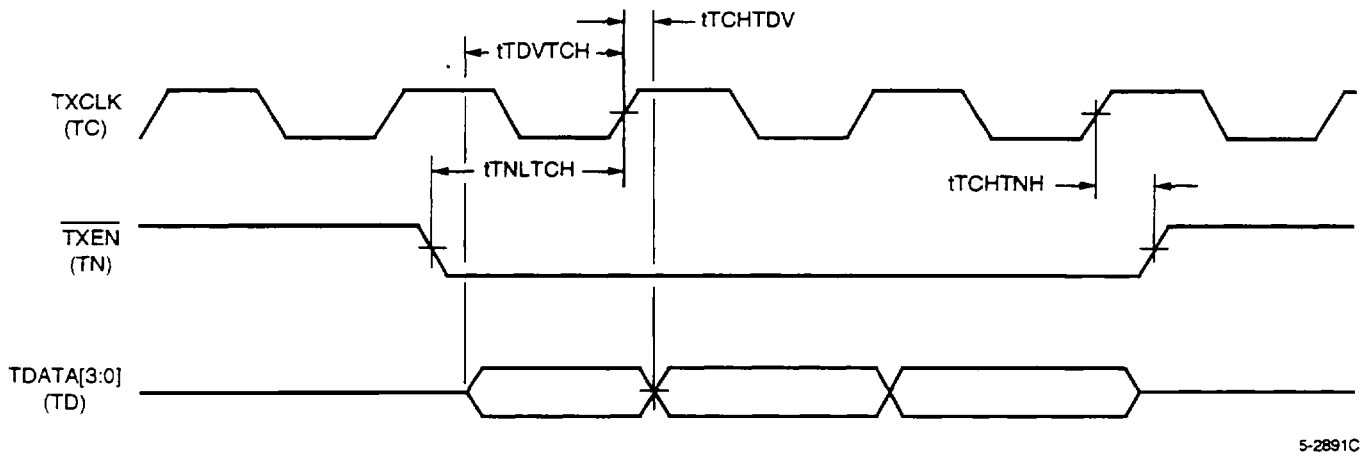


Figure 12. TDATA Timing

Table 17. RCS and RXGRANT Timing (See Figure 13.)

Symbol	Parameter	Min	Max	Unit
tRRLRLV	$\overline{\text{RCSREN}}$ Asserted to RCS[2:0] and RXGRANT Are Valid	0	15	ns
tRRHRLZ	$\overline{\text{RCSREN}}$ Deasserted Until RCS[2:0] and RXGRANT Are High Impedance	0	15	ns
tTCHRLX	Rising Edge of TXCLK Until RCS[2:0] and RXGRANT Are Valid	3	20	ns

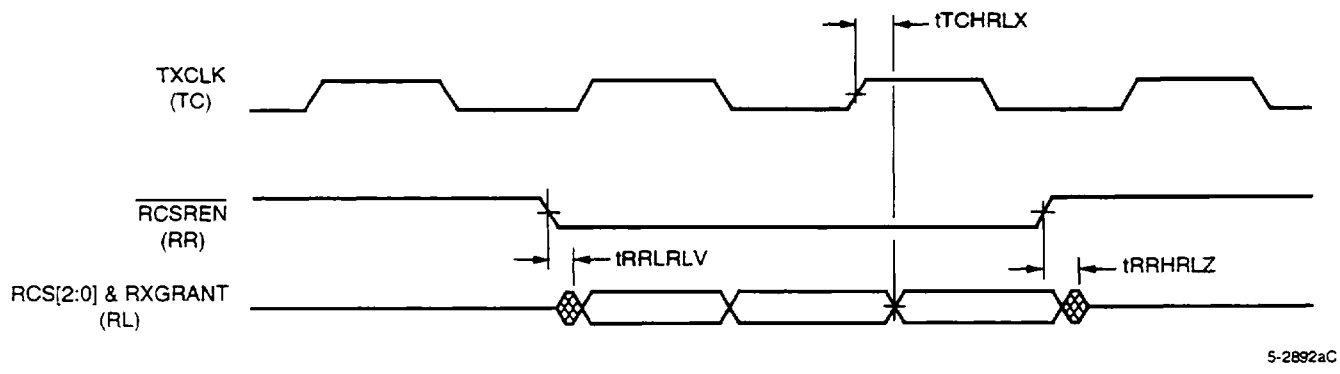


Figure 13. RCS and RXGRANT Timing

Timing Characteristics (continued)

Table 18. TCS Timing (See Figure 14.)

Symbol	Parameter	Min	Max	Unit
tTWLTCH	$\overline{\text{TCSWEN}}$ Asserted Prior to Rising Edge of TXCLK	7	—	ns
tTLVTCH	TCS[2:0] Valid Prior to Rising Edge of TXCLK	7	—	ns
tTCHTWH	TCSWEN Hold Time After Rising Edge of TXCLK	2	—	ns
tTCHTLZ	TCS[2:0] Hold Time After Rising Edge of TXCLK	2	—	ns

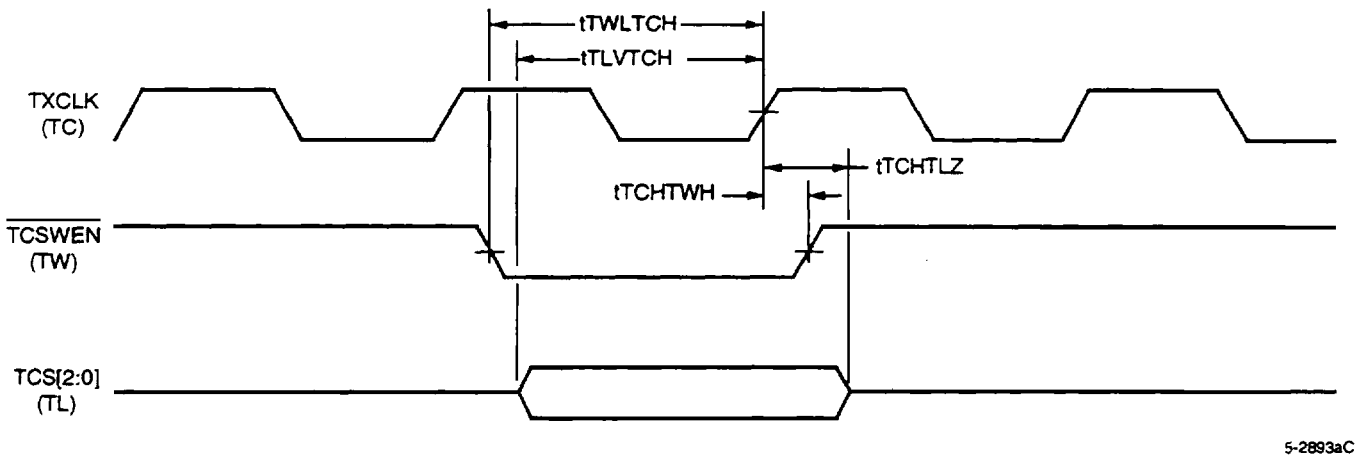


Figure 14. TCS Timing

Table 19. TP Timing (See Figure 15.)

Symbol	Parameter	Min	Max	Unit
tTDVTPV	TDATA to TP	66	267	ns
tTPVRDV	TP to RDATA	65	333	ns
—	Timing Skew Between Data Inputs During Start of Preamble	—	66	ns

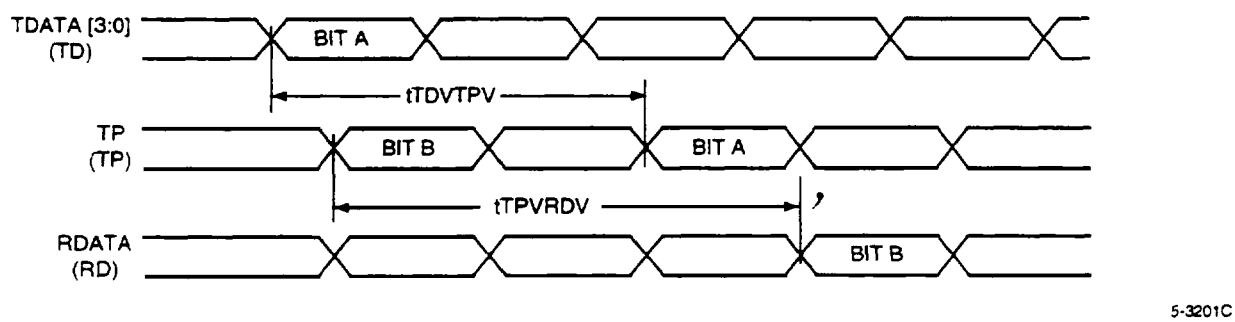
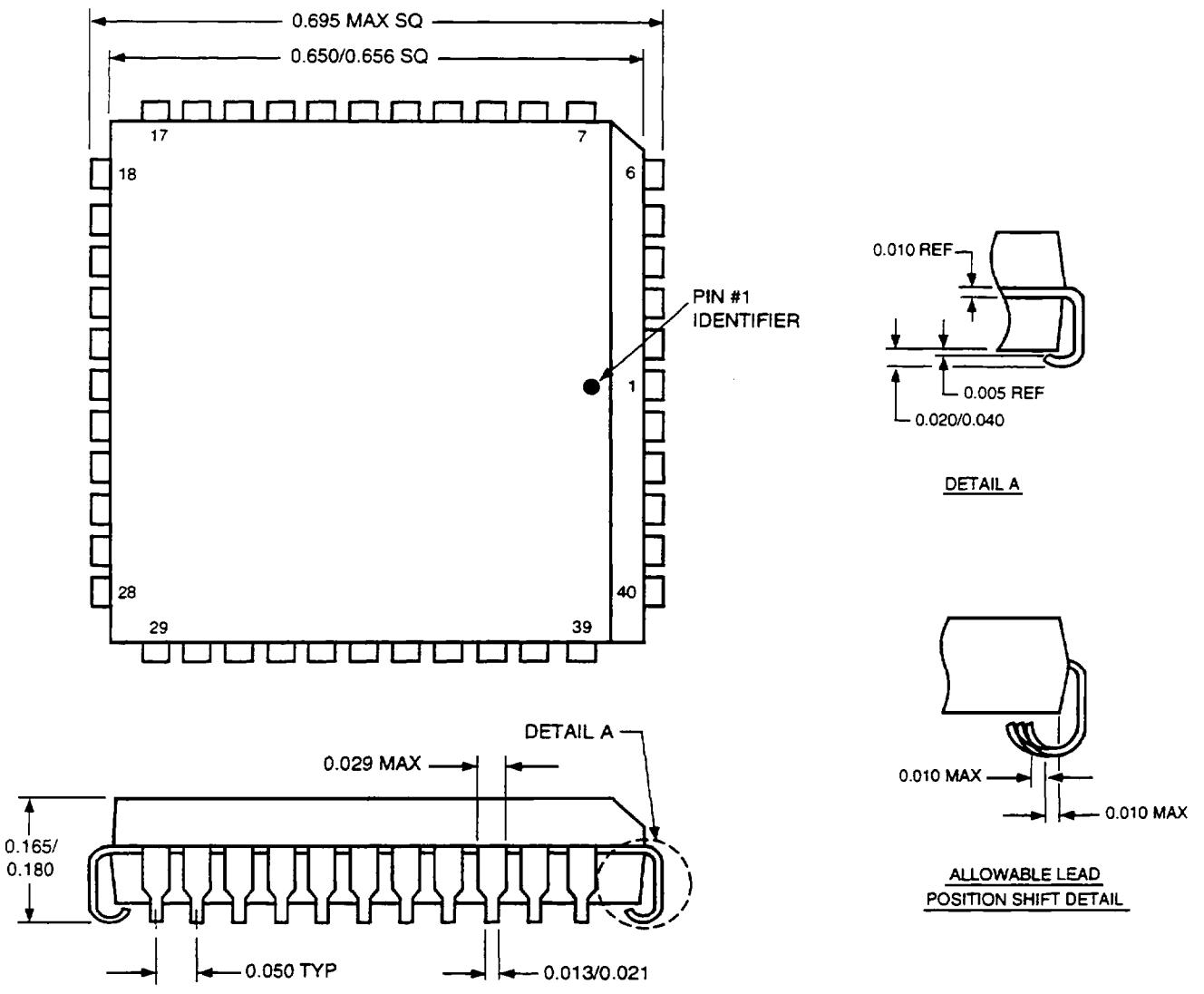


Figure 15. TP Timing

Outline Diagram

44-Pin PLCC Package

All dimensions are in inches.



Ordering Information

Code	Package	Temperature
ATT2X02-MC	44-Pin PLCC	0 °C to 70 °C

Appendix A

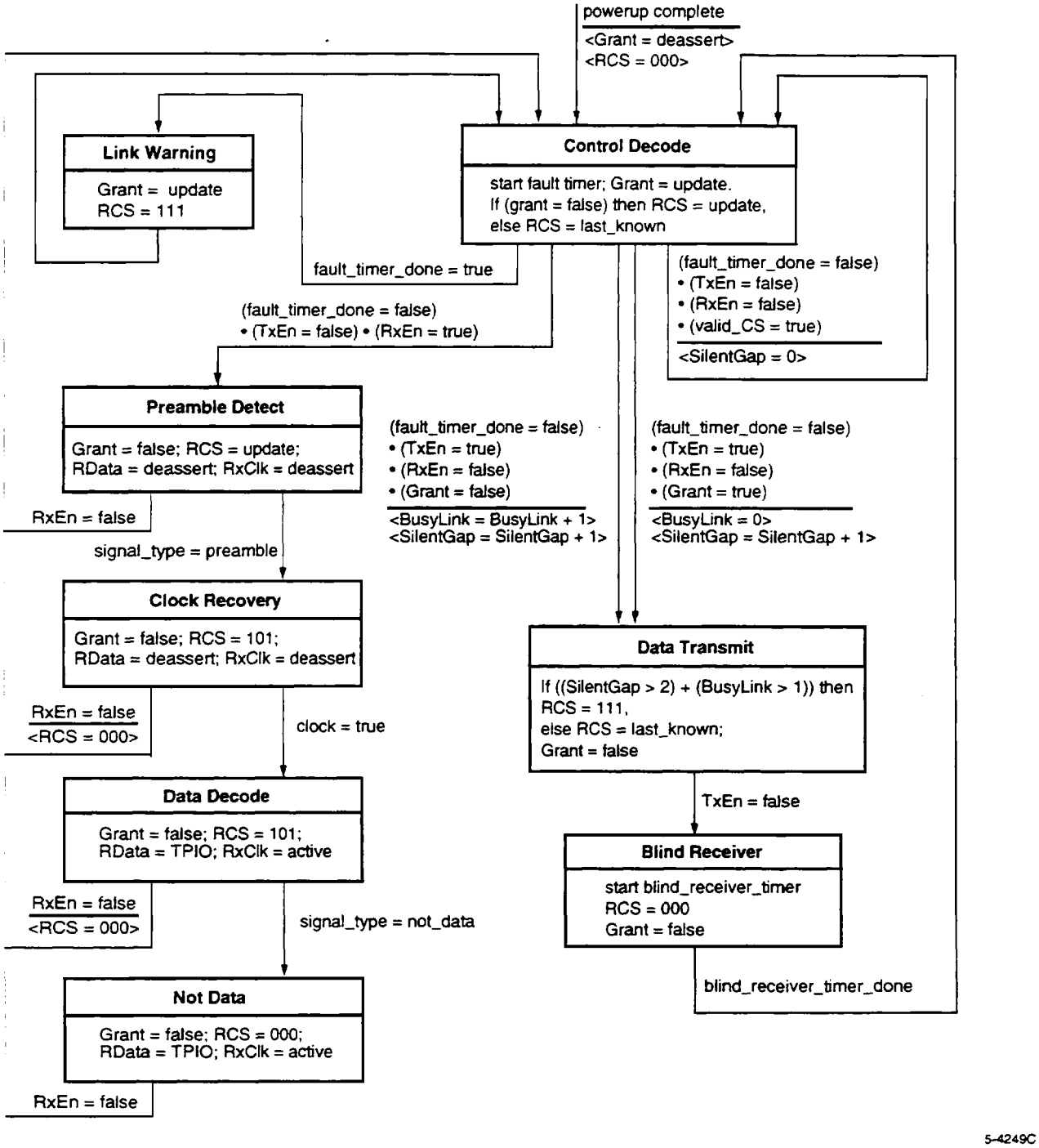


Figure A-1. State Diagram for Receive Functions

Appendix A (continued)

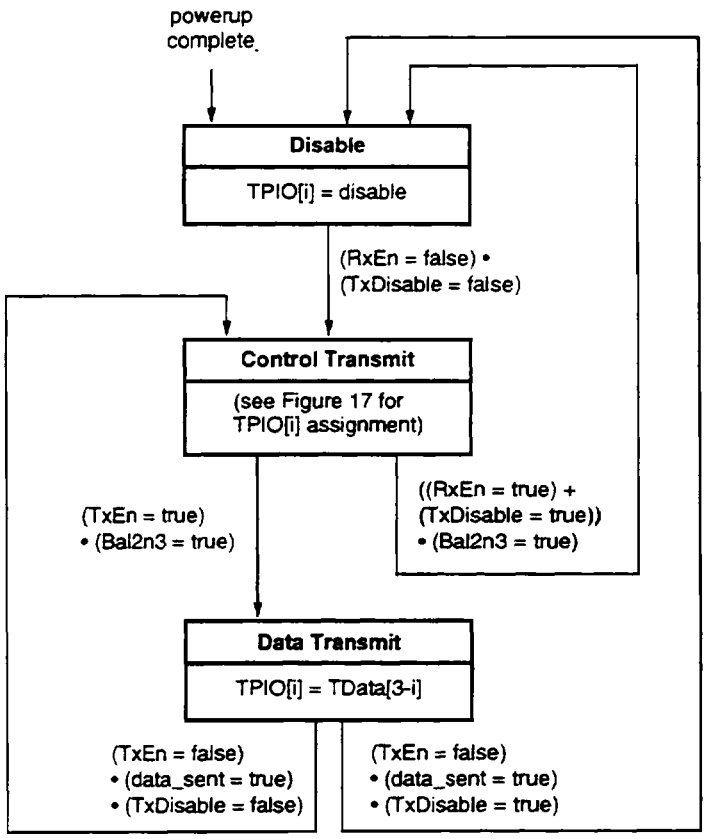


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Figure A-2. State Diagram for Transmit Functions on TPIO:2 and TPIO:3

Appendix A (continued)

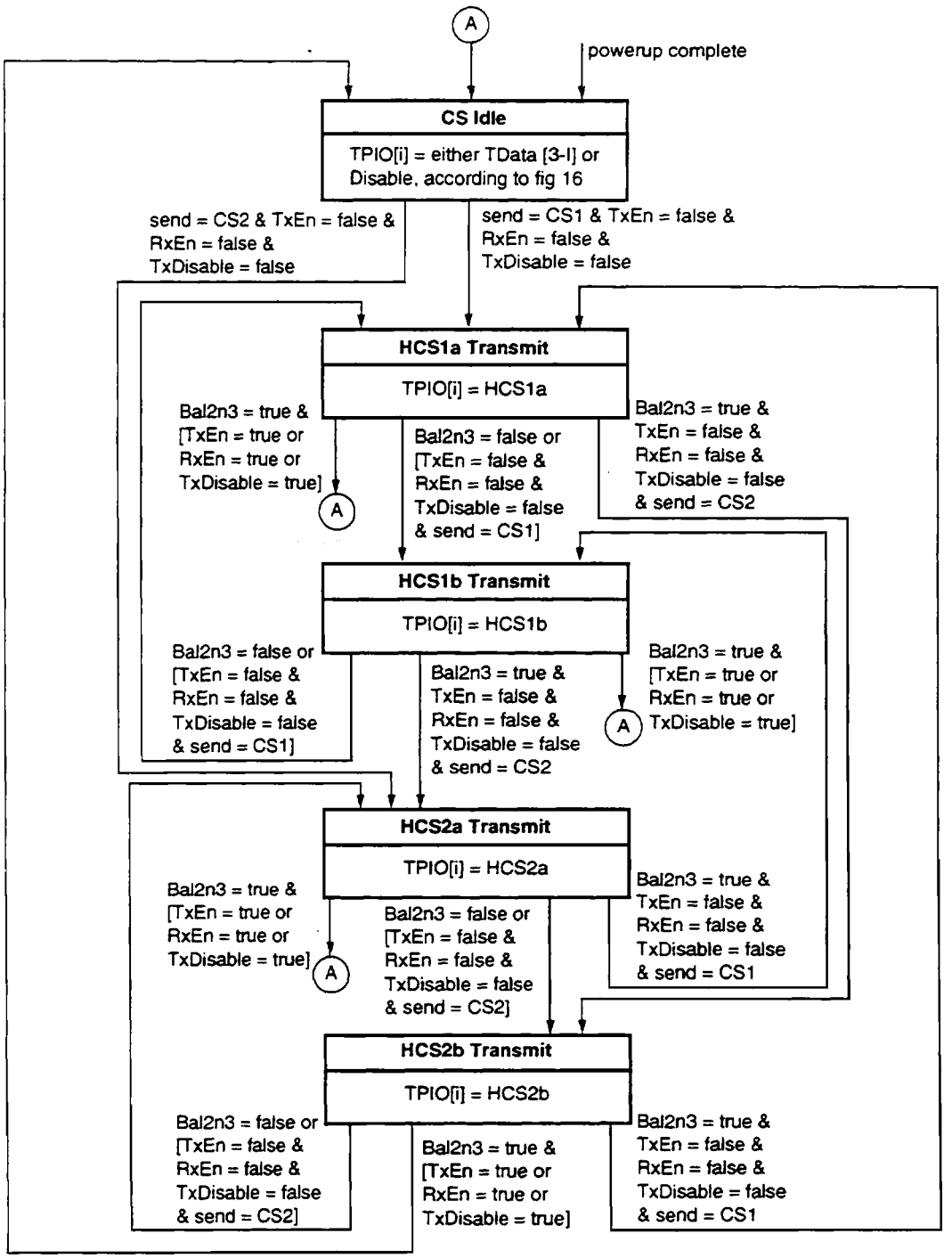

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Figure A-3. State Diagram for Control Signaling on TPIO:2 and TPIO:3

Appendix A (continued)

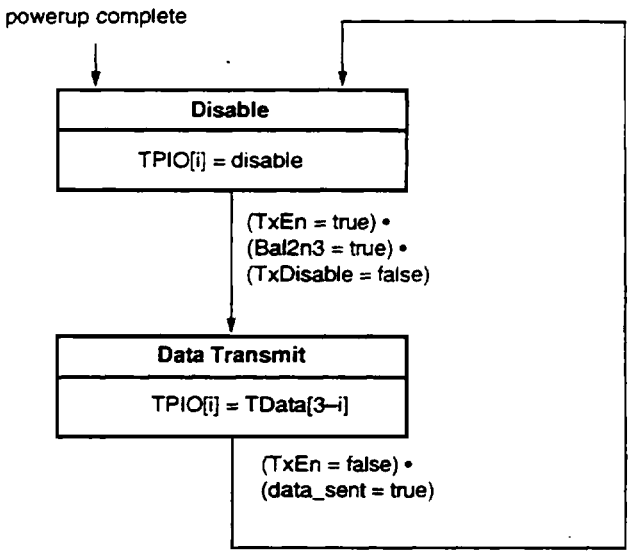

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Figure A-4. State Diagram for Transmit Functions on TPIO:0 and TPIO:1

For additional information, contact your AT&T Account Manager or the following:
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