SG1525A/27A
SG2525A-3525A/27A

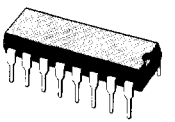
REGULATING PULSE WIDTH MODULATORS

TO 35 V OPERATION
.1 V REFERENCE TRIMMED TO ± 1 %
00 Hz TO 500 KHz OSCILLATOR RANGE
EPARATE OSCILLATOR SYNC TERMINAL
DJUSTABLE DEADTIME CONTROL
ITERNAL SOFT-START
ULSE-BY-PULSE SHUTDOWN
IPUT UNDERVOLTAGE LOCKOUT WITH YSTERESIS
ATCHING PWM TO PREVENT MULTIPLE ULSES
UAL SOURCE/SINK OUTPUT DRIVERS

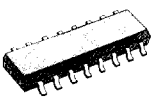
CRIPTION

3G1525A/1527A series of pulse width modula- tegrated circuits are designed to offer impro- erformance and lowered external parts count i used in designing all types of switching power lies. The on-chip + 5.1 V reference is trimmed l % and the input common-mode range of the amplifier includes the reference voltage elimi- g external resistors. A sync input to the oscilla- lows multiple units to be slaved or a single unit synchronized to an external system clock. A e resistor between the C_T and the discharge nals provide a wide range of dead time ad- ient. These devices also feature built-in soft- circuitry with only an external timing capacitor red. A shutdown terminal controls both the soft- circuity and the output stages, providing instan- us turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. This lockout circuitry includes approximately 500 mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulses has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200 mA. The SG1525A output stage features NOR logic, giving a LOW output for an OFF state. The SG1527A utilizes OR logic which results in a HIGH output level when OFF.

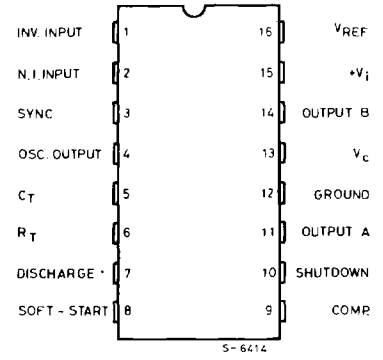
DIP-16
(Plastic -0.25 and Ceramic)



SO16J



CONNECTION DIAGRAM AND ORDERING NUMBERS (top view)



Type	Plastic DIP	Ceramic DIP	SO16J
SG1525A	–	SG1525AJ	–
SG1527A	–	SG1527AJ	–
SG2525A	SG2525AN	SG2525AJ	SG2525AP
SG2527A	SG2527AN	SG2527AJ	SG2527AP
SG3525A	SG3525AN	SG3525AJ	SG3525AP
SG3527A	SG3527AN	SG3527AJ	SG3527AP

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	Supply Voltage	40	V
V_C	Collector Supply Voltage	40	V
I_{OSC}	Oscillator Charging Current	5	mA
I_o	Output Current, Source or Sink	500	mA
I_R	Reference Output Current	50	mA
I_T	Current through C_T Terminal Logic Inputs Analog Inputs	5 – 0.3 to + 5.5 – 0.3 to V_i	mA V V
P_{tot}	Total Power Dissipation at T_{amb} = 70 °C	1000	mW
T_j	Junction Temperature Range	– 55 to 150	°C
T_{stg}	Storage Temperature Range	– 65 to 150	°C
T_{op}	Operating Ambient Temperature : **SG1525A/27A** **SG2525A/27A** **SG3525A/27A**	– 55 to 125 – 25 to 85 0 to 70	°C °C °C

THERMAL DATA (DIP-16)

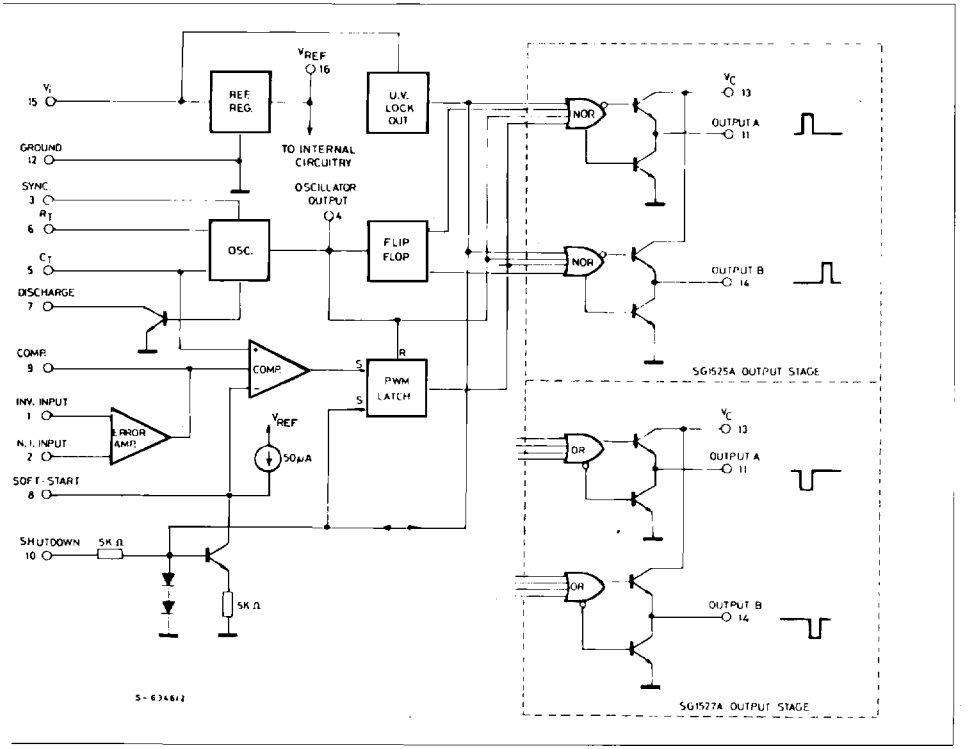
			Ceramic	Plastic
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max	–	50 °C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	150 °C/W	80 °C/W

THERMAL DATA (SO16J)

$R_{th\ j\text{-}alumina}$*	Thermal Resistance Junction-alumina	Max	50	°C/W

* Thermal resistance junction-alumina with the device soldered on the middle of an alumina supporting substrate measuring 15 × 20 mm ; 0 thickness with infinite heatsink.

OCK DIAGRAM



:CTRICAL CHARACTERISTICS

= 20 V, and over operating temperature, unless otherwise specified)

mbol	Parameter	Test Conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
FERENCE SECTION									
V_{REF}	Output Voltage	T_j = 25 °C	5.05	5.1	5.15	5	5.1	5.2	V
ΔV_{REF}	Line Regulation	V_i = 8 to 35 V		10	20		10	20	mV
ΔV_{REF}	Load Regulation	I_L = 0 to 20 mA		20	50		20	50	mV
$_{REF}/\Delta T^*$	Temp. Stability	Over Operating Range		20	50		20	50	mV
*	Total Output Variation	Line, Load and Temperature	5		5.2	4.95		5.25	V
	Short Circuit Current	V_{REF} = 0 T_j = 25 °C		80	100		80	100	mA
*	Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz, T_j = 25 °C		40	200		40	200	μVrms
$/_{REF}$*	Long Term Stability	T_j = 125 °C, 1000 hrs		20	50		20	50	mV

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Ui
			Min.	Typ.	Max.	Min.	Typ.	Max.	
OSCILLATOR SECTION**									
*, •	Initial Accuracy	T_j = 25 °C		± 2	± 6		± 2	± 6	
*, •	Voltage Stability	V_i = 8 to 35 V		± 0.3	± 1		± 1	± 2	
$\Delta f/\Delta T$*	Temperature Stability	Over Operating Range		± 3	± 6		± 3	± 6	
f_{MIN}	Minimum Frequency	R_T = 200 KΩ C_T = 0.1 µF			120			120	H
f_{MAX}	Maximum Frequency	R_T = 2 KΩ C_T = 470 pF	400			400			K
	Current Mirror	I_{RT} = 2 mA	1.7	2	2.2	1.7	2	2.2	n
*, •	Clock Amplitude		3	3.5		3	3.5		
*, •	Clock Width	T_j = 25 °C	0.3	0.5	1	0.3	0.5	1	µ
	Sync Threshold		1.2	2	2.8	1.2	2	2.8	
	Sync Input Current	Sync Voltage = 3.5 V		1	2.5		1	2.5	r
ERROR AMPLIFIER SECTION (V_{CM} = 5.1 V)									
V_{OS}	Input Offset Voltage			0.5	5		2	10	r
I_b	Input Bias Current			1	10		1	10	µ
I_{os}	Input Offset Current				1			1	µ
	DC Open Loop Gain	$R_L \geq 10$ MΩ	60	75		60	75		
*	Gain Bandwidth Product	G_v = 0 dB T_j = 25 °C	1	2		1	2		M
*, z	DC Transconduct.	30 KΩ ≤ R_L ≤ 1 MΩ T_j = 25 °C	1.1	1.5		1.1	1.5		
	Output Low Level			0.2	0.5		0.2	0.5	
	Output High Level		3.8	5.6		3.8	5.6		
CMR	Comm. Mode Reject.	V_{CM} = 1.5 to 5.2 V	60	75		60	75		
PSR	Supply Voltage Rejection	V_i = 8 to 35 V	50	60		50	60		
PWM COMPARATOR									
	Minimum Duty-cycle				0			0	
	Maximum Duty-cycle		45	49		45	49		
•	Input Threshold	Zero Duty-cycle	0.7	0.9		0.7	0.9		
		Maximum Duty-cycle		3.3	3.6		3.3	3.6	
*	Input Bias Current			0.05	1		0.05	1	

:CTRICAL CHARACTERISTICS (continued)

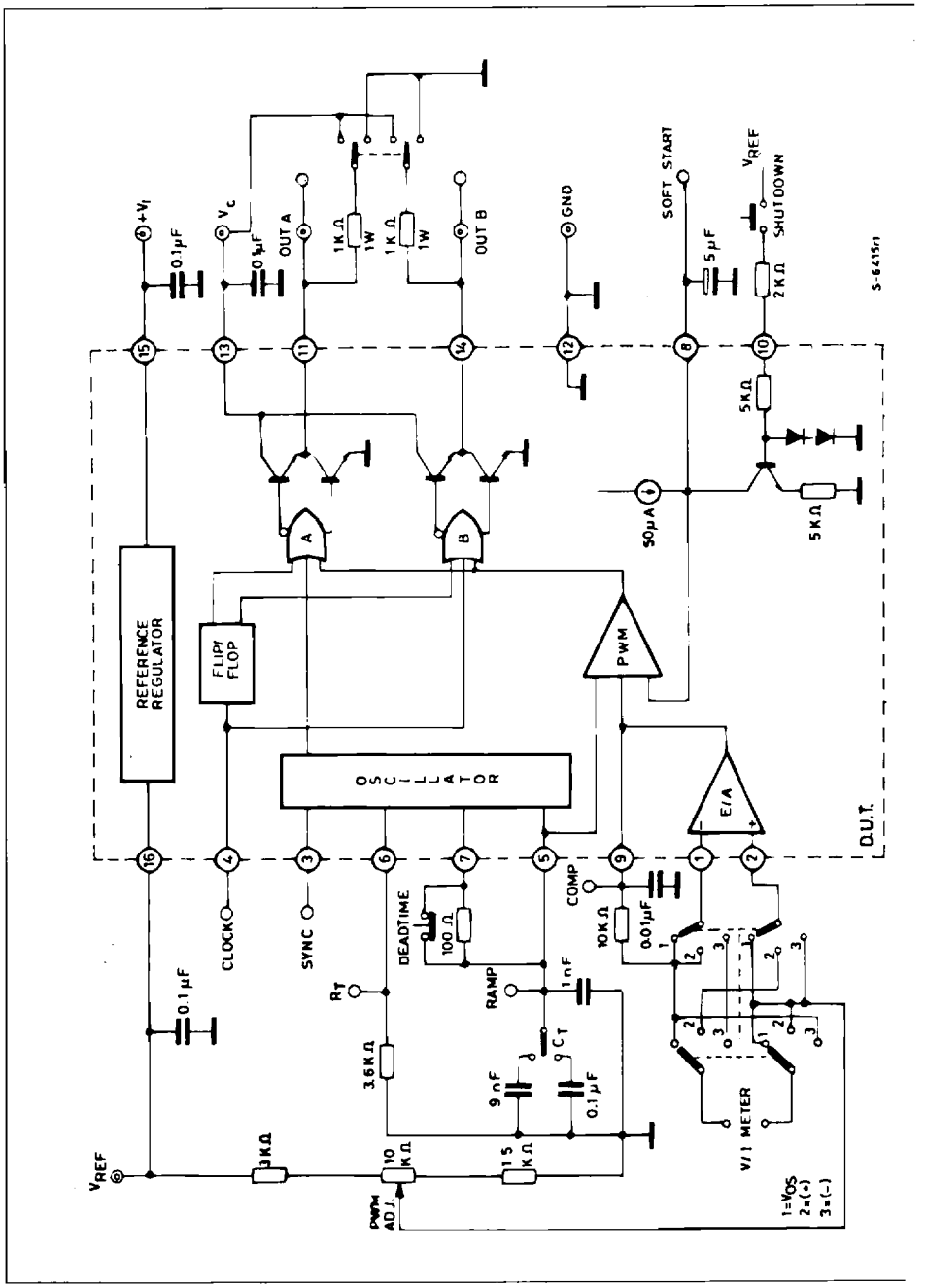
mbol	Parameter	Test Conditions	SG1525A/2525A SG1527A/2527A			SG3525A SG3527A			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
TDOWN SECTION									
	Soft Start Current	V_{SD} = 0 V, V_{SS} = 0 V	25	50	80	25	50	80	µA
	Soft Start Low Level	V_{SD} = 2.5 V		0.4	0.7		0.4	0.7	V
	Shutdown Threshold	To outputs, V_{SS} = 5.1 V T_j = 25 °C	0.6	0.8	1	0.6	0.8	1	V
	Shutdown Input Current	V_{SD} = 2.5 V		0.4	1		0.4	1	mA
*	Shutdown Delay	V_{SD} = 2.5 V T_j = 25 °C		0.2	0.5		0.2	0.5	µs
PUT DRIVERS (each output) (V_C = 20 V)									
	Output Low Level	I_{sink} = 20 mA		0.2	0.4		0.2	0.4	V
		I_{sink} = 100 mA		1	2		1	2	V
	Output High Level	I_{source} = 20 mA	18	19		18	19		V
		I_{source} = 100 mA	17	18		17	18		V
	Under-Voltage Lockout	V_{comp} and V_{ss} = High	6	7	8	6	7	8	V
C	Collector Leakage	V_C = 35 V			200			200	µA
r*	Rise Time	C_L = 1 nF, T_j = 25 °C		100	600		100	600	ns
f*	Fall Time	C_L = 1 nF, T_j = 25 °C		50	300		50	300	ns
\L STANDBY CURRENT									
s	Supply Current	V_i = 35 V		14	20		14	20	mA

se parameters, although guaranteed over the recommended operating conditions, are not 100 % tested in production.
ed at f_{osc} = 40 KHz (R_T = 3.6 KΩ, C_T = 0.1 µF, R_D = 0 Ω). Approximate oscillator frequency is defined by :

$$\frac{1}{C_T (0.7\ R_T + 3\ R_D)}$$

ransconductance (g_M) relates to DC open-loop voltage gain (G_V) according to the following equation : $G_V = g_M R_L$ where R_L is the resistance pin 9 to ground. The minimum g_M specification is used to calculate minimum G_V when the error amplifier output is loaded.

TEST CIRCUIT



COMMENDED OPERATING CONDITIONS (•)

Parameter	Value
put Voltage (V_i)	8 to 35 V
llector Supply Voltage (V_C)	4.5 to 35 V
nk/Source Load Current (steady state)	0 to 100 mA
nk/Source Load Current (peak)	0 to 400 mA
ference Load Current	0 to 20 mA
cillator Frequency Range	100 Hz to 400 KHz
cillator Timing Resistor	2 KΩ to 150 KΩ
cillator Timing Capacitor	0.001 µF to 0.1 µF
ad Time Resistor Range	0 to 500 Ω

ange over which the device is functional and parameter limits are guaranteed.

ure 1 : Oscillator Charge Time vs. R_T and C_T.

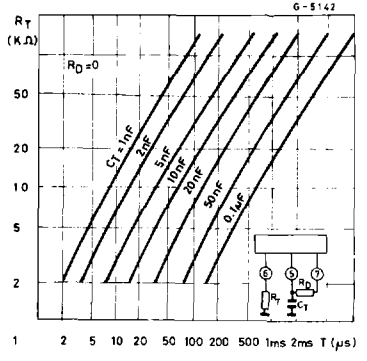
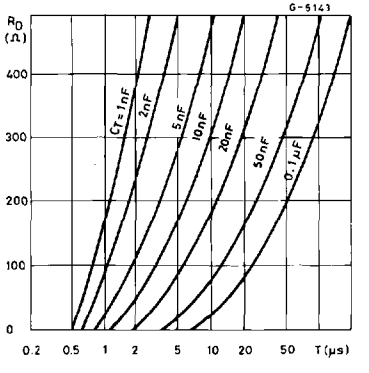


Figure 2 : Oscillator Discharge Time vs. R_D and C_T.



ure 3 : SG1525A Output Saturation Characteristics.

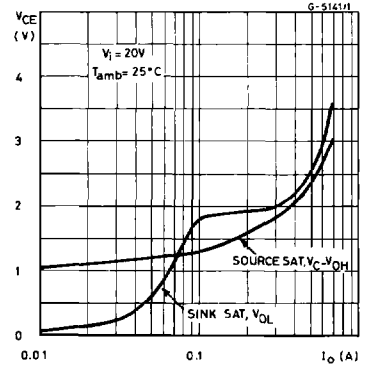


Figure 4 : Error Amplifier Voltage Gain and Phase vs. Frequency.

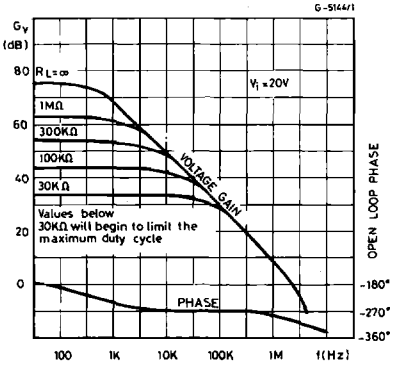
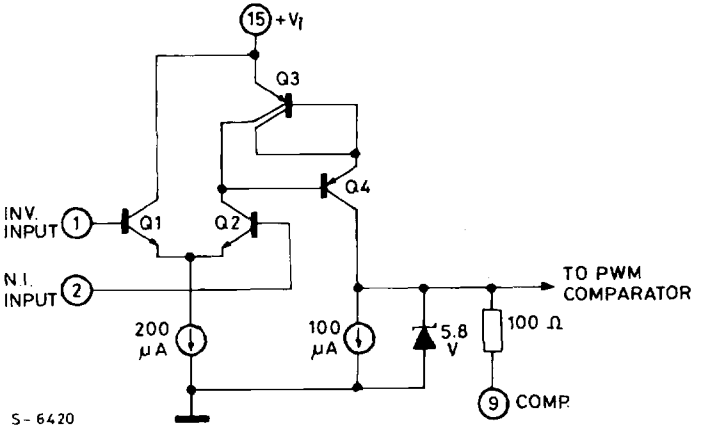


Figure 5 : SG1525A Error Amplifier.



PRINCIPLES OF OPERATION

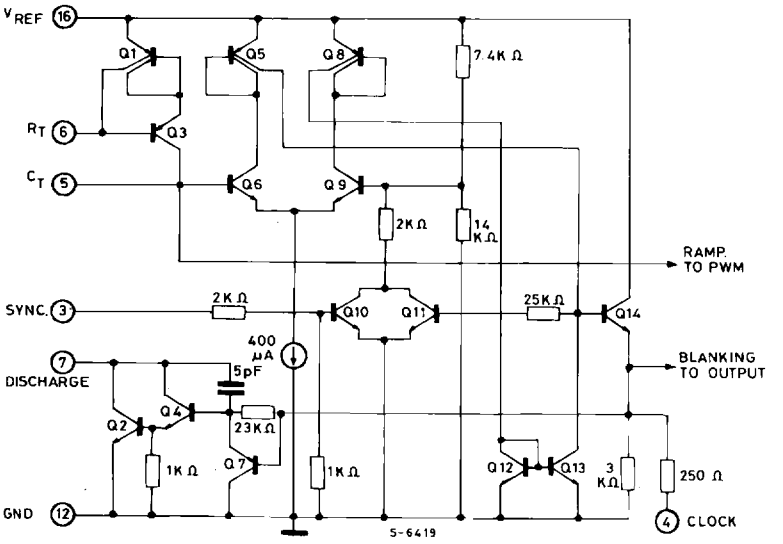
SHUTDOWN OPTIONS (see Block Diagram)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100 µA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions : the PWM latch is immediately set providing the fastest turn-off signal to outputs ; and a 150 µA current sink begins to charge the external soft-start capacitor. If the s down command is short, the PWM signal is te nated without significant discharge of the soft-s capacitor, thus, allowing, for example, a conver implementation of pulse-by-pulse current limit Holding Pin 10 high for a longer duration, howe will ultimately discharge this external capacitor cycling slow turn-on upon release.

Pin 10 should not be left floating as noise pic could conceivably interrupt normal operation.

jure 6 : SG1525A Oscillator Schematic.



ure 7 : SG1525A Output Circuit (1/2 circuit shown).

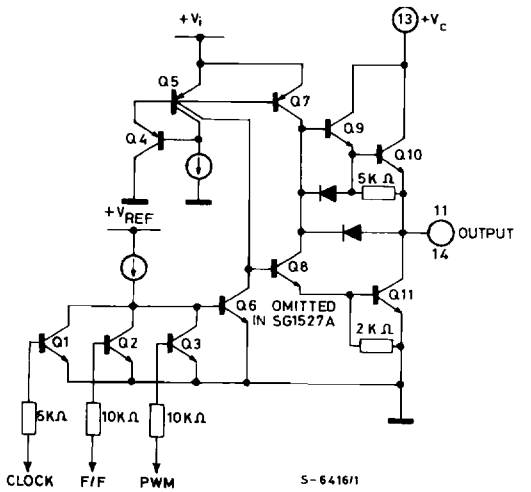
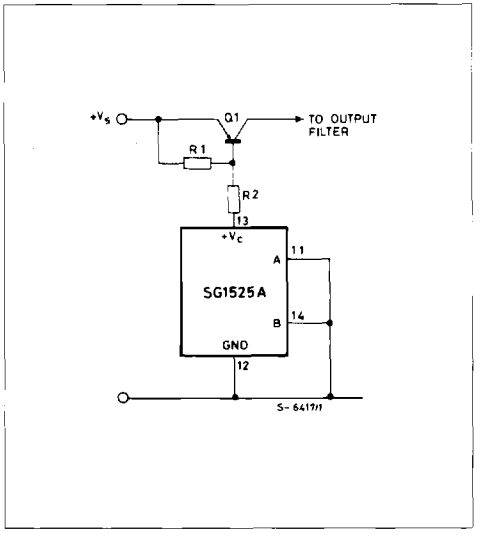
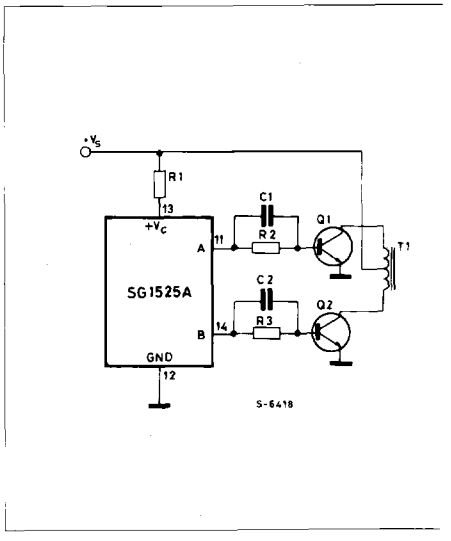


Figure 8.



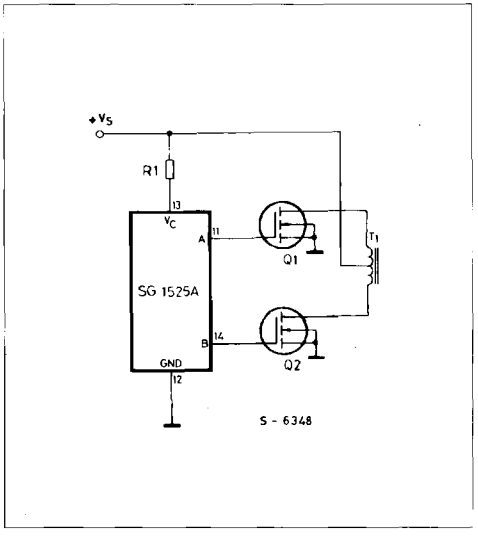
For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

Figure 9.



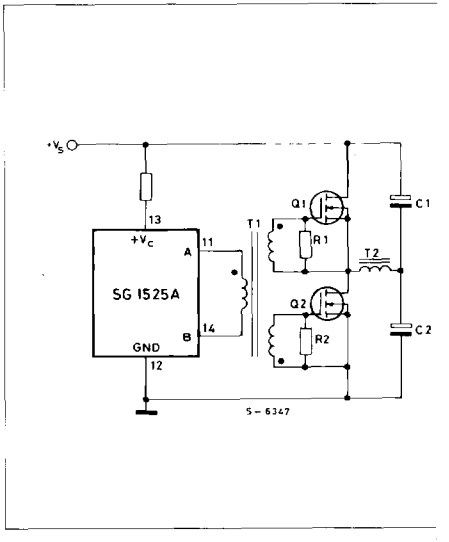
In conventional push-pull bipolar designs, forw base drive is controlled by R_1 - R_3. Rapid turr times for the power devices are achieved speed-up capacitors C_1 and C_2.

Figure 10.



The low source impedance of the output drivers provides rapid charging of Power Mos input capacitance while minimizing external components.

Figure 11.



Low power transformers can be driven directl the SG1525A. Automatic reset occurs during d time, when both ends of the primary winding switched to ground.