# Silicon N-Channel Junction FET

## Description

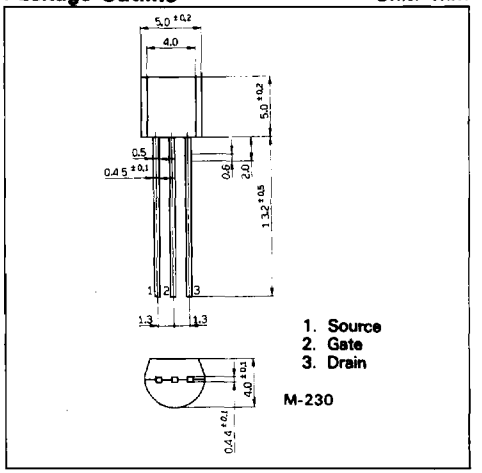
The 2SK125 is an N-Channel silicon junction type field effect transistor developed for low-noise amplification at frequencies up to UHF. It is especially suitable for when a wide dynamic range is required.

## Features

- High power gain
  12.5 dB (Typ.)
  (f = 100 MHz Gate grounded)
- Low noise figure
  1.5 dB (Typ.)
  (f = 100 MHz Gate grounded)
- Wide dynamic range
  3rd intermodulation distortion
  −52 dB (Typ.)
  (f = 100 MHz at 100 dBμ input)
- Small inverse transfer coefficient
  $|S_{12}| = 0.035$ (Typ.)
  (f = 500 MHz Gate grounded)

## Package Outline

Unit: mm




## Structure

Silicon N-Channel junction FET.

## Application

UHF band amplification, mixing, oscillation, analog switches.

## Absolute Maximum Ratings (Ta = 25°C)

| | | | |
|---|---|---|---|
| • Drain to gate voltage | $V_{DGO}$ | 35 | V |
| • Source to gate voltage | $V_{SGO}$ | 35 | V |
| • Drain current | $I_D$ | 100 | mA |
| • Gate current | $I_G$ | 10 | mA |
| • Channel temperature | Tj | 120 | °C |
| • Storage temperature | Tstg | −50 to +120 | °C |
| • Allowable power dissipation | $P_D$ | 300 | mW |

51044A-TO

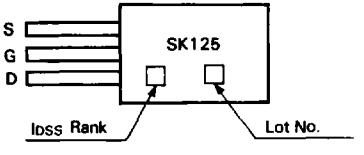
## Electrical Characteristics

Ta = 25°C

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Gate cutoff current | $I_{GSS}$ | $V_{GS} = -15V$, $V_{DS} = 0$ | | | −10 | nA |
| Gate to source voltage | $V_{GSS}$ | $I_G = 10\mu A$, $V_{DS} = 0$ | −35 | | | V |
| Drain current | $I_{DSS}$ | $V_{DS} = 10V$, $V_{GS} = 0$<br>P.W = 300μs | 40 | | 75 | mA |
| Gate to source cutoff voltage | $V_{GS(OFF)}$ | $V_{DS} = 10V$, $I_D = 100\mu A$ | −2 | | −6 | V |
| Forward transfer conductance | $\|Y_{fs}\|$ | $V_{DS} = 10V$, $I_D = 10mA$<br>f = 1 kHz | 10 | 14 | | mS |
| Reverse transfer capacitance | Crss | $V_{DG} = 10V$, $I_S = 0mA$<br>f = 1 MHz, source grounded | | 2.6 | 3 | pF |
| Power gain | PG | $V_{DG} = 10V$, $I_D = 10mA$ *1<br>f = 100 MHz, BW = 2.8 MHz | 10 | 12.5 | | dB |
| Noise figure | NF | $V_{DG} = 10V$, $I_D = 10mA$ *1<br>f = 100 MHz, BW = 2.8 MHz<br>At the NF of the amplifier<br>in the next stage is 4.2 dB | | 1.8 | 2.5 | dB |
| Intermodulation distortion | IMD | $V_{DG} = 10V$, $I_D = 10mA$, *2<br>$f_1 = 100$ MHz, $f_2 = 100.1$ MHz,<br>at 100 dBμ input | −45 | −52 | | dB |
| Junction to ambient thermal resistance | θj-a | | | | 190 | °C/W |

Note) *1. See the 100 MHz, PG, NF, test circuit.
*2. See the 100 MHz IMD test circuit.

## Mark




## Classification

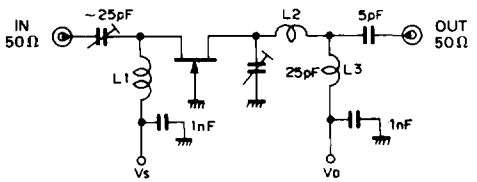
| Rank | $I_{DSS}$ (mA)<br>$V_{DS}$ = 10V<br>$V_{GS}$ = 0V |
|---|---|
| 2 | 40 to 75 |
| 3 | 40 to 52 |
| 4 | 48 to 63 |
| 5 | 57 to 75 |

## Standard Circuit Design Data

Ta = 25°C

| Item | Symbol | Condition | Typ. | Unit |
|---|---|---|---|---|
| Input resistance | $r_{ig}$ | $V_{DG}$ = 10V, $I_D$ = 10 mA<br>f = 100 MHz | 70 | Ω |
| Input capacitance | $C_{ig}$ | | 3.0 | pF |
| Output resistance | $r_{og}$ | | 5 | kΩ |
| Output capacitance | $C_{og}$ | | 3.0 | pF |
| Power gain | PG | $V_{DG}$ = 10V, $I_D$ = 10 mA<br>f = 500 MHz, BW = 12 MHz | 7.0 | dB |
| Noise figure | NF | | 4.0 | dB |
| Reverse transfer coefficient | $\lvert S_{12} \rvert$ | $V_{DG}$ = 10V, $I_D$ = 10 mA<br>f = 500 MHz | 0.035 | |
| Equivalent input noise voltage | $\overline{e}_n$ | $V_{DS}$ = 10V, $I_D$ = 10 mA<br>f = 1 kHz | 3 | $nV/\sqrt{Hz}$ |
| Drain source ON resistance | $R_{(ON)}$ | $I_D$ = 10 mA, $V_{GS}$ = 0V | 35 | Ω |
| Drain cutoff current | $I_{D(OFF)}$ | $V_{DS}$ = 10V, $V_{GS}$ = −10V | 0.1 | nA |

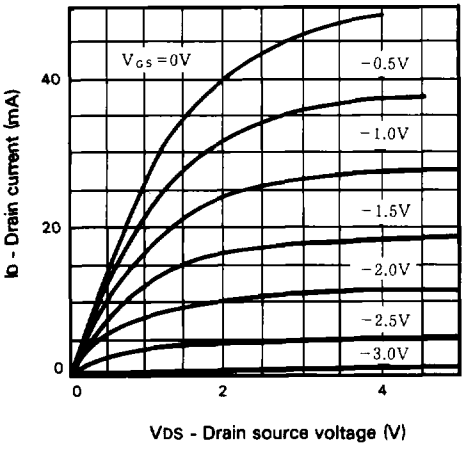
## 100 MHz PG, NF Test Circuit



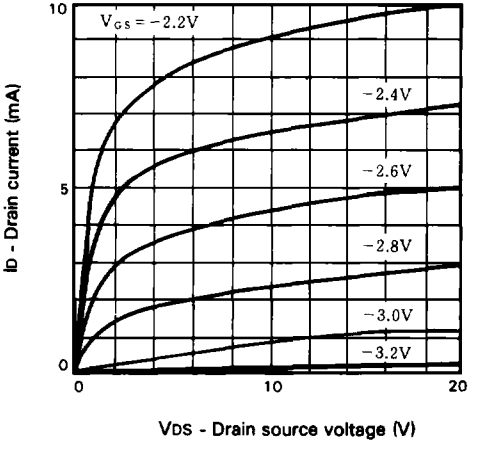

L1 : 0.45 φmm polyurethane wire φ3 mm 10.5 t
L2, L3 : 0.45 φmm polyurethane wire φ3 mm 5.5 t

## Output Characteristics

**Drain current vs. Drain source voltage**

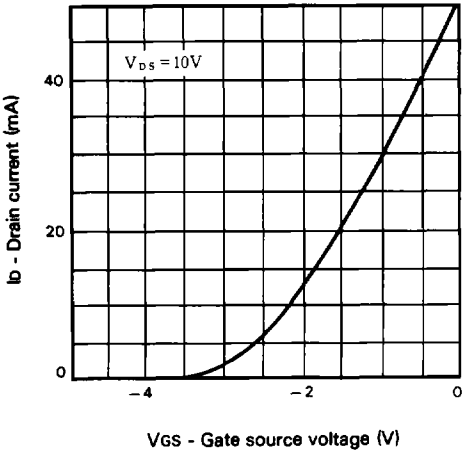



**Drain current vs. Drain source voltage**

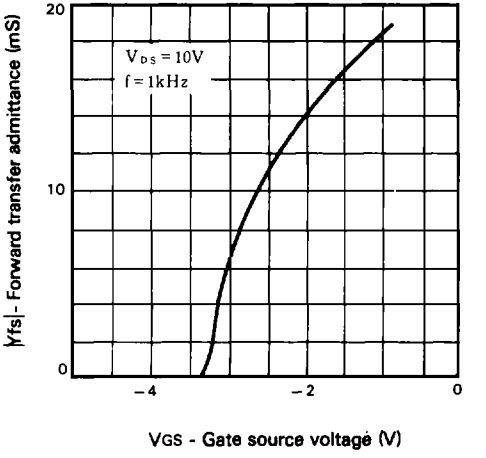



## Transfer Characteristics

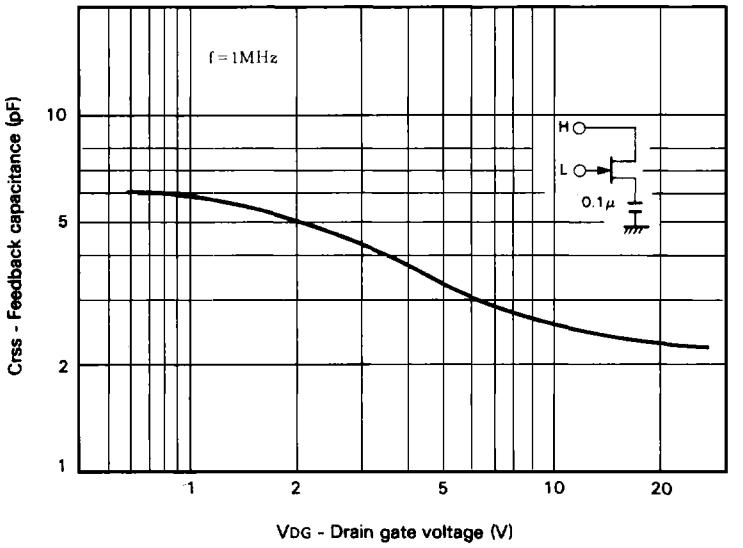
**Drain current vs. Gate source voltage**



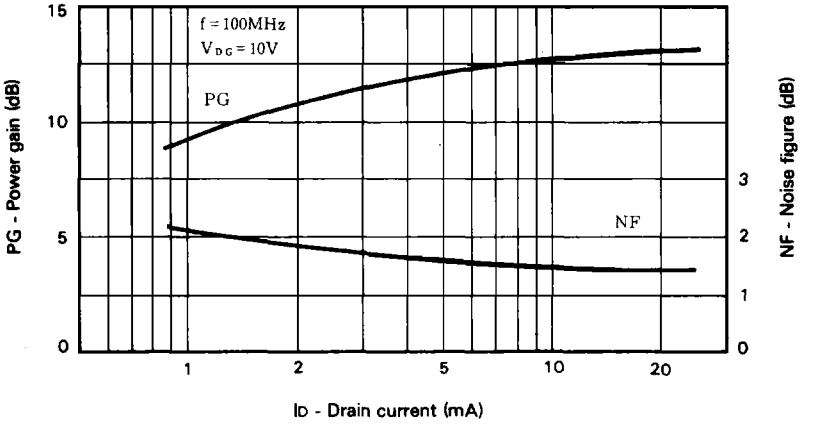

**Forward transfer admittance vs. Gate source voltage**



**Feedback capacitance vs. Drain gate voltage**



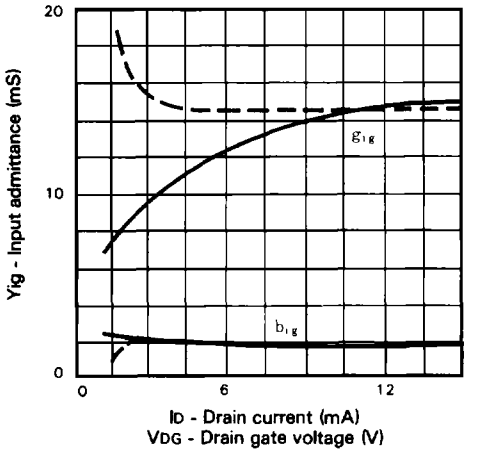

**Common-gate power gain noise figure vs. Drain current**



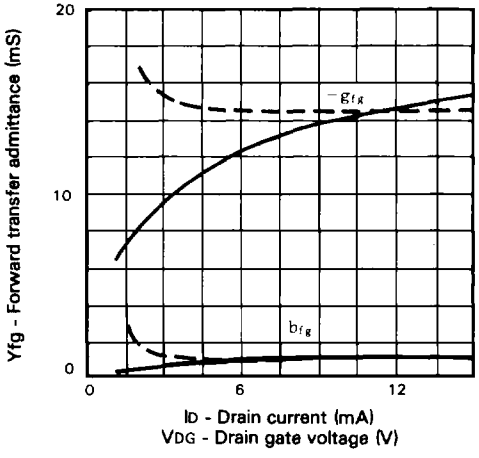
## Common Gate Y-Parameter

——— Drain current characteristics ($V_{DG}$ = 10V, f = 100 MHz)
— — — Drain gate voltage characteristics ($I_D$ = 10mA, f = 100 MHz)

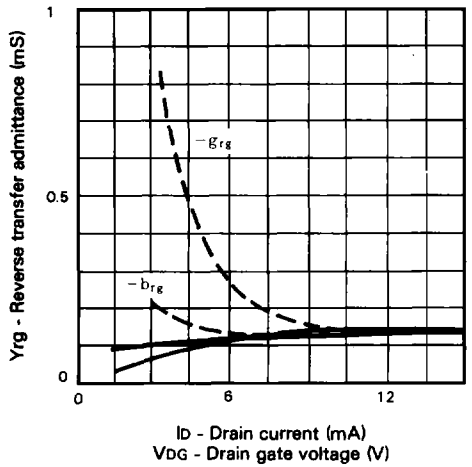
**Input admittance**



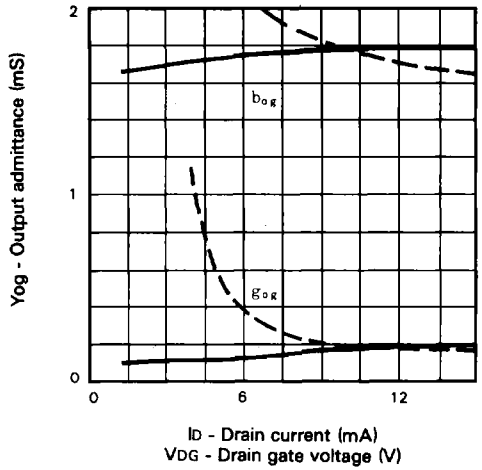

**Forward transfer admittance**




**Reverse transfer admittance**

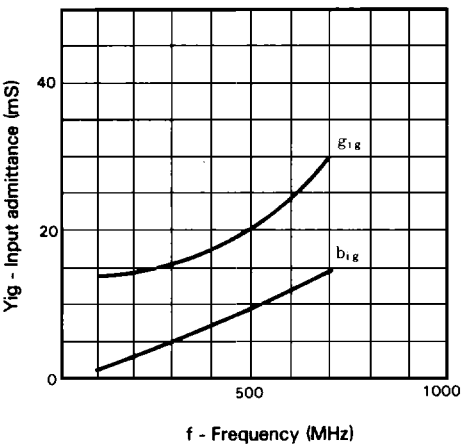



**Output admittance**

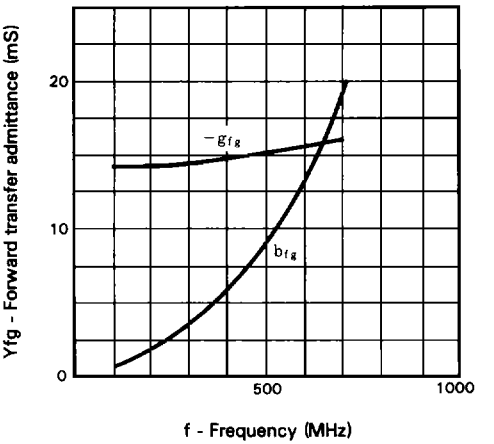


**Common Gate Y-Parameter vs. Frequency** ($V_{DG}$ = 10V, $I_D$ = 10mA)

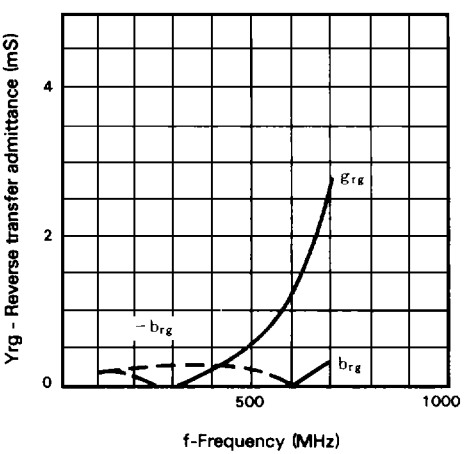
**Input admittance**



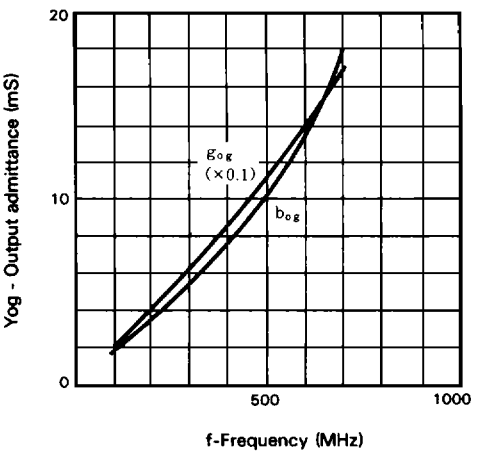

**Forward transfer admittance**



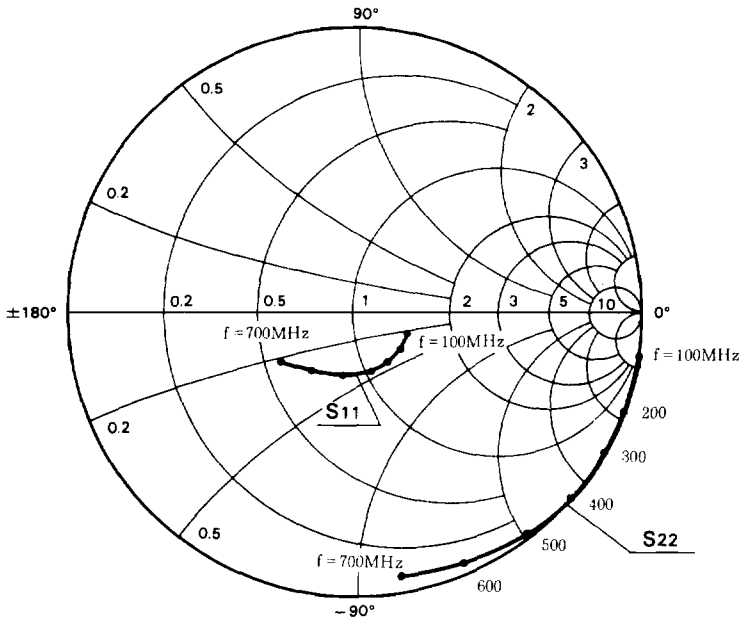

**Reverse transfer admittance**

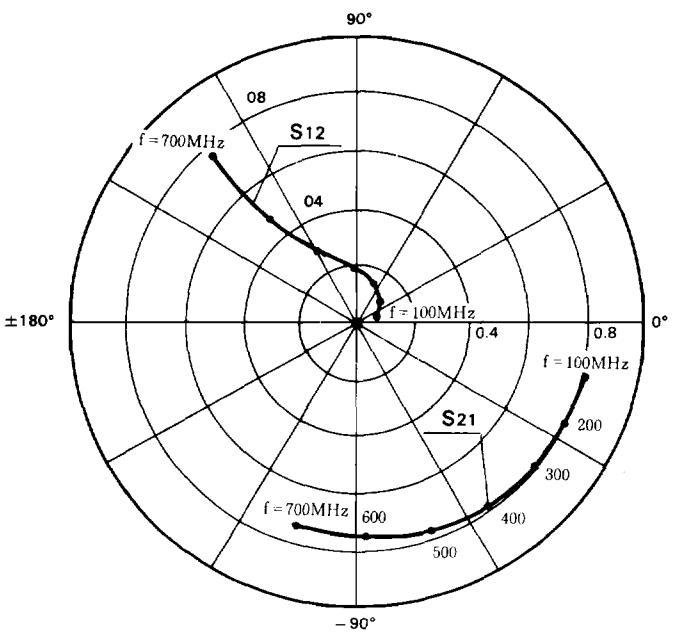



**Output admittance**

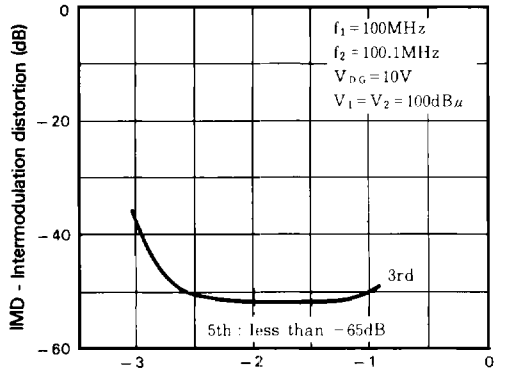


**Common Gate S-Parameter vs. Frequency** ($V_{DG}$ = 10V, $I_D$ = 10 mA)

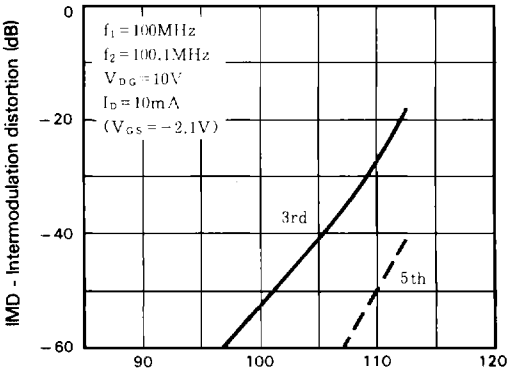


## Intermodulation distortion characteristics

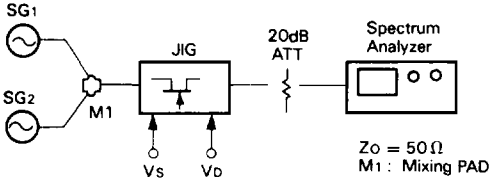


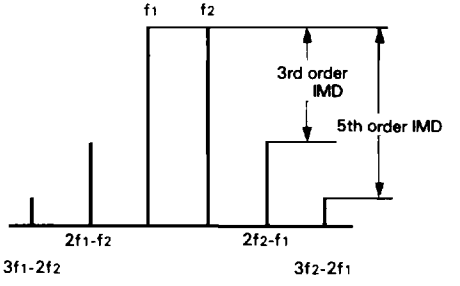

VGS - Gate source voltage (V)



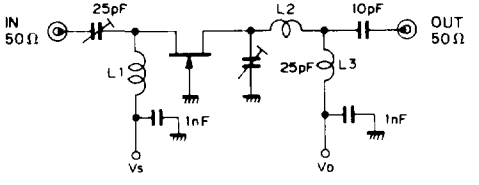

V1, V2 - Input signal level (dBμ)

## Block Diagram for IMD Measurement



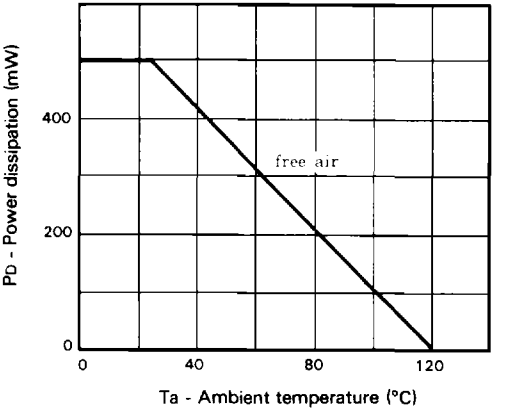




## 100 MHz IMD Test Circuit




L1 : 0.45 φmm polyurethane wire 3φ mm 10.5 t
L2, L3 : 0.45 φmm polyurethane wire 3φ mm 5.5 t

## Derating curve




Ta - Ambient temperature (°C)