Am27S31

(512 x 8) Bipolar PROM

DISTINCTIVE CHARACTERISTICS

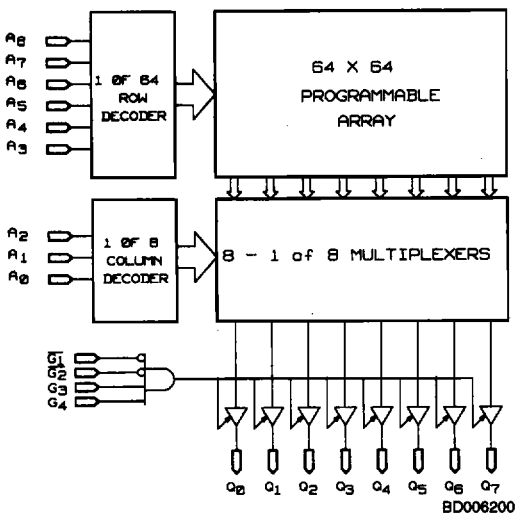
- High Speed — 35ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current and three-state outputs
- Fast chip select

GENERAL DESCRIPTION

The Am27S31 (512-words by 8-bits) is a Schottky TTL Programmable Read-Only Memory (PROM).

This device is available in three-state output version compatible with low-power Schottky bus standards capable of satisfying the requirements of a variety of microprogrammable controls, mapping functions, code conversion, or logic replacement. Easy word-depth expansion is facilitated by both active LOW ($\overline{G_1}$ and $\overline{G_2}$) and active HIGH (G_3 and G_4) output enables.

BLOCK DIAGRAM



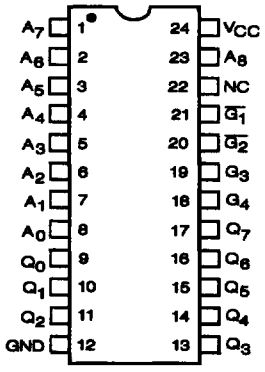
PRODUCT SELECTOR GUIDE

Part Number	27S31A		27S31	
Address Access Time	35 ns	45 ns	55 ns	70 ns
Operating Range	C	M	C	M

Publication # 03207 | Rev. C | Amendment /0
Issue Date: May 1986

CONNECTION DIAGRAM
Top View

DIP*



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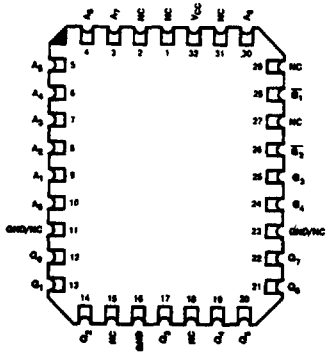

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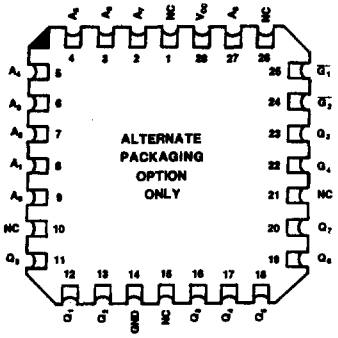

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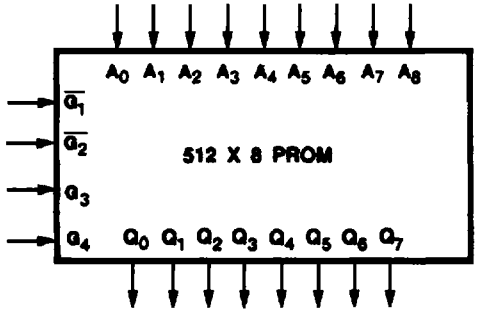
*Also available in 24-Pin Flatpack. Connections identical to DIPs.

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



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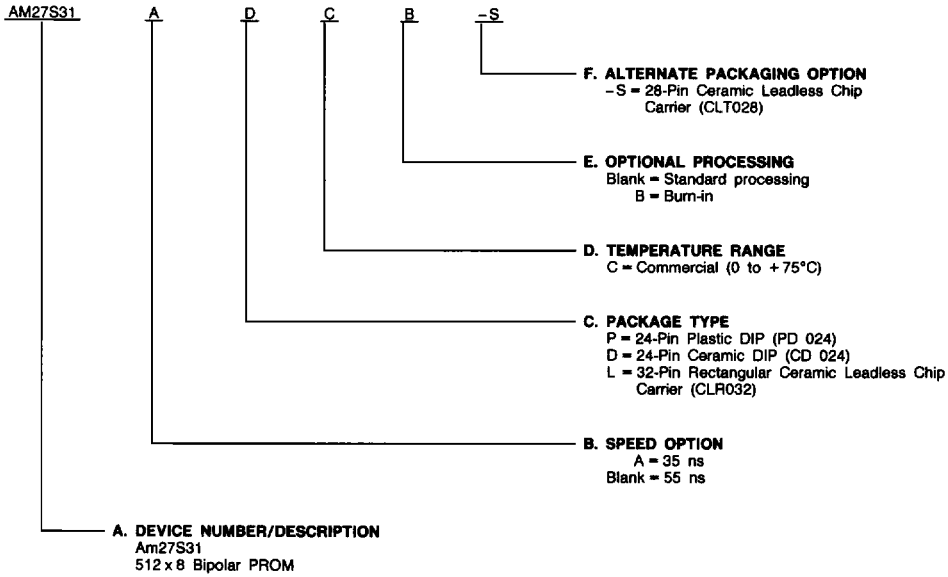
VCC/ = Power Supply
GND/ = Ground

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing
F. Alternate Packaging Option



Valid Combinations	
AM27S31	PC, PCB, DC, DCB, LC, LC-S, LCB, LCB-S
AM27S31A	

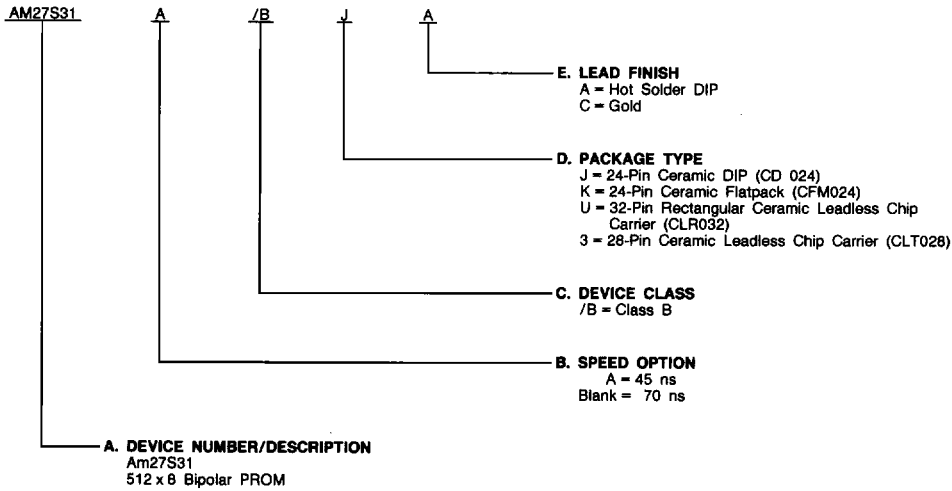
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**
B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM27S31	/BJA, /BKA, /BUC, /B3C
AM27S31A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_8$ Address Inputs
The 9-bit field presented at the address inputs selects one of 512 memory locations to be read from.

$Q_0 - Q_7$ Data Output Port
The Outputs whose state represents the data read from the selected memory locations.

$\overline{G_1}$, $\overline{G_2}$, G_3, G_4 Output Enable
Provides direct control of the Q-output buffers. Outputs disabled forces all three-state outputs to a floating or high-impedance state.

$$\text{Enable} = \overline{G_1} \cdot \overline{G_2} \cdot G_3 \cdot G_4$$

$$\text{Disable} = \overline{\overline{G_1} \cdot \overline{G_2} \cdot G_3 \cdot G_4}$$
$$= G_1 + G_2 + \overline{G_3} + \overline{G_4}$$

V_{CC} Device Power Supply Pin
The most positive of the logic power supply pins.

GND Device Power Supply Pin
The most negative of the logic power supply pins.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (See Note 1)*

No.	Parameter Symbol	Parameter Description	"A" Versions				Standard Versions				Units
			COM'L		MIL		COM'L		MIL		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	TAVPKH	Address to PK HIGH Setup Time	27		30		35		40		ns
2	TPKHAX	Address to PK HIGH Hold Time	0		0		0		0		ns
3	TPKHDQV1	Delay from PK HIGH to Output Valid, for initially active outputs (HIGH) or LOW) (Note 7)	4	12	4	17	4	15	4	20	ns
4	TPKHPKL TPKLPKH	PK Pulse Width (HIGH or LOW)	15		20		20		20		ns
5	TGLDQV	Asynchronous Output Enable LOW to Output Valid (HIGH or LOW) (See Note 3)		22		25		25		30	ns
6	TGHDQZ	Asynchronous Output Enable HIGH to Output High Z (See Note 3)		17		22		20		25	ns
7	TGSVPKH	$\overline{GS}$ to PK HIGH Setup Time (See Note 4)	12		12		15		15		ns
8	TPKHGSX	$\overline{GS}$ to PK HIGH Hold Time (See Note 4)	0		0		0		0		ns
9	TPKHDQV2	Delay from PK HIGH to Output Valid, for initially High Z outputs (See Note 4)		17		22		20		25	ns
10	TPKHDQZ	Delay from PK HIGH to Output High Z (See Notes 2 & 4)		17		22		20		25	ns
11	TILDQV	Delay from $\overline{I}$ LOW to Output Valid (HIGH or LOW) (See Note 5)		25		30		30		35	ns
12	TIHPKH	Asynchronous $\overline{I}$ Recovery to PK (HIGH) (See Note 5)	20		25		25		30		ns
13	TILIH	Asynchronous $\overline{I}$ Pulse Width (LOW) (See Note 5)	20		20		25		25		ns
14	TISVPKH	$\overline{IS}$ to PK HIGH Setup Time (See Note 6)	20		25		20		25		ns
15	TPKHISX	$\overline{IS}$ to PK HIGH Setup Time (See Note 6)	5		5		5		5		ns

Notes:
1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V, using test loads in A & B.
2. TGHDQZ and TPKHDQZ are measured to Steady State HIGH −0.5 V and Steady State LOW +0.5 V output levels, using the test load in C.
3. Applies only if the architecture is configured for Asynchronous $\overline{Enable}$.
4. Applies only if the architecture word has been programmed for a Synchronous $\overline{Enable}$ input.
5. Applies only if the architecture word has been programmed for a Asynchronous $\overline{Initialize}$ input.
6. Applies only if the architecture word has been programmed for a Synchronous $\overline{Initialize}$ input.
7. Minimum Delay times are guaranteed by design and supported by characterization data.

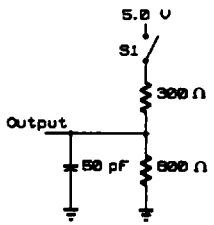
DIAGNOSTIC MODE SWITCHING CHARACTERISTICS over operating range unless otherwise specified (See Note 1)*

No.	Parameter Symbol	Parameter Description	COM'L		MIL		Units
			Min.	Max.	Min.	Max.	
16	TSDVDKH	Serial Data In to DK HIGH Setup Time	25		30		ns
17	TDKHSDX	Serial Data In to DK HIGH Hold Time	0		0		
18	TMVPKH	Mode to PK HIGH Setup Time	35		40		
19	TPKHMX	Mode to PK HIGH Hold Time	0		0		
20	TMVDKH	Mode to DK HIGH Setup Time	35		40		
21	TDKHMX	Mode to DK HIGH Hold Time	0		0		
22	TDQVDKH	Output Data In to DK HIGH Setup Time	25		30		
23	TDKHDQX	Output Data In to DK HIGH Hold Time	0		0		
24	TDKHSQV	Delay from DK HIGH to Serial Data Output (Shifting)		30		35	
25	TSDVSQV	Delay from SD Valid to SQ Valid (Mode Input HIGH)		25		30	
26	TDKHDKL TDKLDKH	DK Pulse Width (HIGH or LOW)	25		25		
27	TMHSQV TMLSQV	Delay from Mode (HIGH or LOW) to SQ Valid		25		30	

See also A-C TEST LOADS.

*See last page of this spec for Group A Subgroup Testing information.

SWITCHING TEST CIRCUITS



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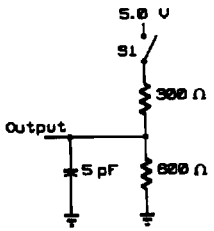

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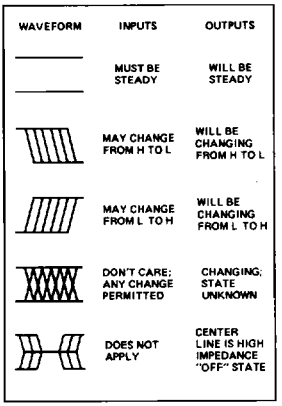
A. Output Load for all A-C tests except TGVQZ

B. Output Load for TGVQZ

KEY TO SWITCHING WAVEFORMS



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Notes: 1. All device test loads should be located within 2" of device output pin.
2. S_1 is open for Output Data HIGH to Hi-Z and Hi-Z to Output Data HIGH tests. S_1 is closed for all other AC tests.
3. Load capacitance includes all stray and fixture capacitance.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

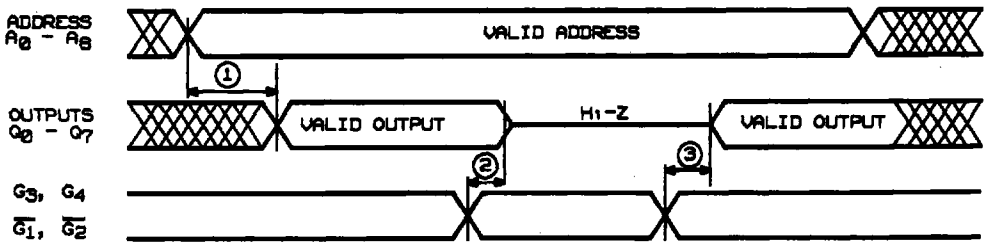
No.	Parameter Symbol	Parameter Description	"A" Version COM'L Min.	"A" Version COM'L Max.	"A" Version MIL Min.	"A" Version MIL Max.	Standard Version COM'L Min.	Standard Version COM'L Max.	Standard Version MIL Min.	Standard Version MIL Max.	Units
1	TAVQV	Address Valid to Output Valid Access Time		35		45		55		70	ns
2	TGVQZ	Delay from Output Enable Valid to Output Hi-Z		20		25		25		30	ns
3	TGVQV	Delay from Output Enable Valid to Output Valid		20		25		25		30	ns

See also Switching Test Circuits.

Notes: 1. Tests are performed with input transition time of 5 ns or less, timing reference levels of 1.5 V, and input pulse levels of 0 to 3.0 V using test load in A under Switching Test Circuits.
2. TGVQZ is measured at steady state HIGH output voltage −0.5 V and steady state LOW output voltage +0.5 V ouput levels using the test load in B under Switching Test Circuits.

*See the last page of this spec for Group A Subgroup Testing information.

SWITCHING WAVEFORMS



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SUBGROUP A TESTING INFORMATION

DC CHARACTERISTICS

Parameter Symbol	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IL}	1, 2, 3
I_{IH}	1, 2, 3
I_{SC}	1, 2, 3
I_{CC}	1, 2, 3
I_{CEX}	1, 2, 3

SWITCHING CHARACTERISTICS

Parameter Symbol	Subgroups
TAVQV	9, 10, 11
TGVQZ	9, 10, 11
TGVQV	9, 10, 11
Functional Tests	7, 8

MILITARY BURN-IN

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.