128 Megabit CMOS DDR SDRAM

DPDD16MX8RSAY5

PRELIMINARY

DESCRIPTION:

The Memory Stack™ series is a family of interchangeable memory modules. The 128 Megabit Double Data Rate Synchronous DRAM module is a member of this family which utilizes the space saving LP-Stack™ TSOP stacking technology. The devices are constructed with two 16 Meg x 4 DDR DRAMs.

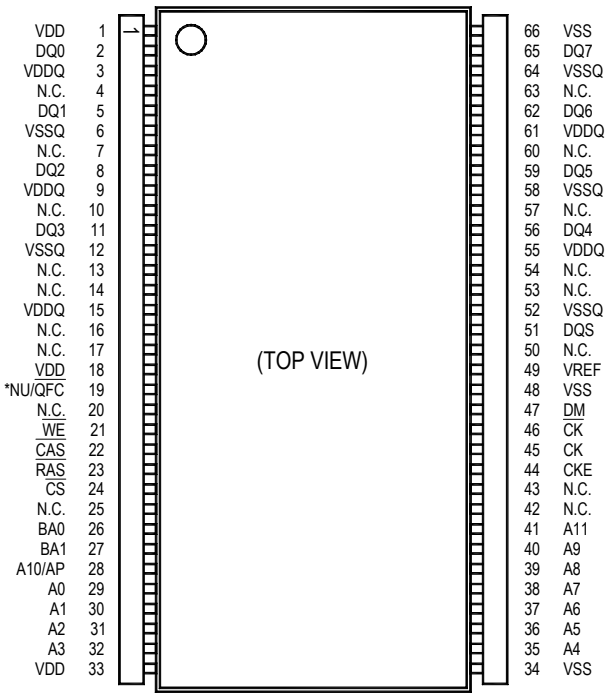
The 64 Megabit based LP-Stack™ module, DPDD16MX8RSAY5, has been designed to fit the same footprint as the 16 Meg x 4 DDR SDRAM TSOP monolithic. This allows for system upgrade without electrical or mechanical redesign, providing an immediate and low cost memory solution.

FEATURES:

- Configuration Available:
  16 Meg x 8 (2 Banks of 4 Meg x 4 bit x 4 banks)
- Clock Frequency:
  100, 125, 133, 143, 167 MHz
- 2.5 Volt DQ Supply
- JEDEC Standard SSTL_2 Interface for all Inputs/Outputs
- Four Bank Operation
- Programmable Burst Type:
  Burst Length and Read Latency
- Refresh: 4096 Cycles/64ms
- Refresh Types: Auto and Self
- JEDEC Approved Footprint and Pinout
- IPC-A-610 Manufacturing Standards
- Package: 66-Pin Leaded TSOP Stack

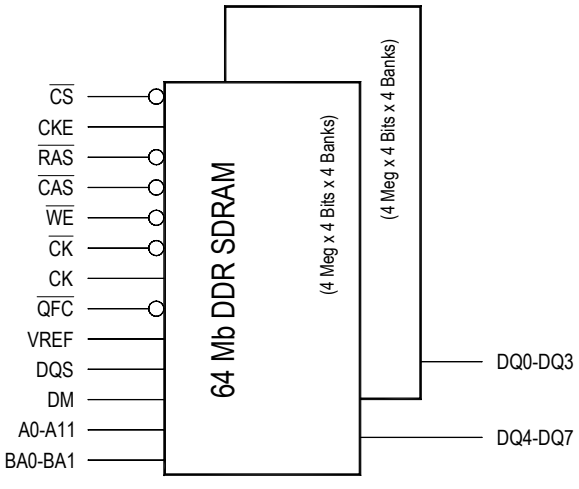
PIN NAMES	
A0-A11	Row Address: A0-A11 Column Address: A0-A8
BA0,BA1	Bank Select Address
A10/AP	Auto Precharge
DQ0-DQ7	Data In/Data Out
$\overline{CAS}$	Column Address Strobe
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe
$\overline{WE}$	Data Write Enable
CK, $\overline{CK}$	Differential Clock Inputs
CKE	Clock Enable
DQS	Data Strobe
DM	Data Mask
$\overline{QFC}$	DQ FET Switch Control
VDD	Power Supply (+2.5V)
Vss	Ground
VDDQ	DQ Power Supply (+2.5V)
VssQ	DQ Ground
VREF	Reference Voltage for inputs
N.C.	No Connect
NU	Not Used, Electrical Connect is Present

PIN-OUT DIAGRAM



* This pin is a No Connect for Some Manufacturers.

FUNCTIONAL BLOCK DIAGRAM



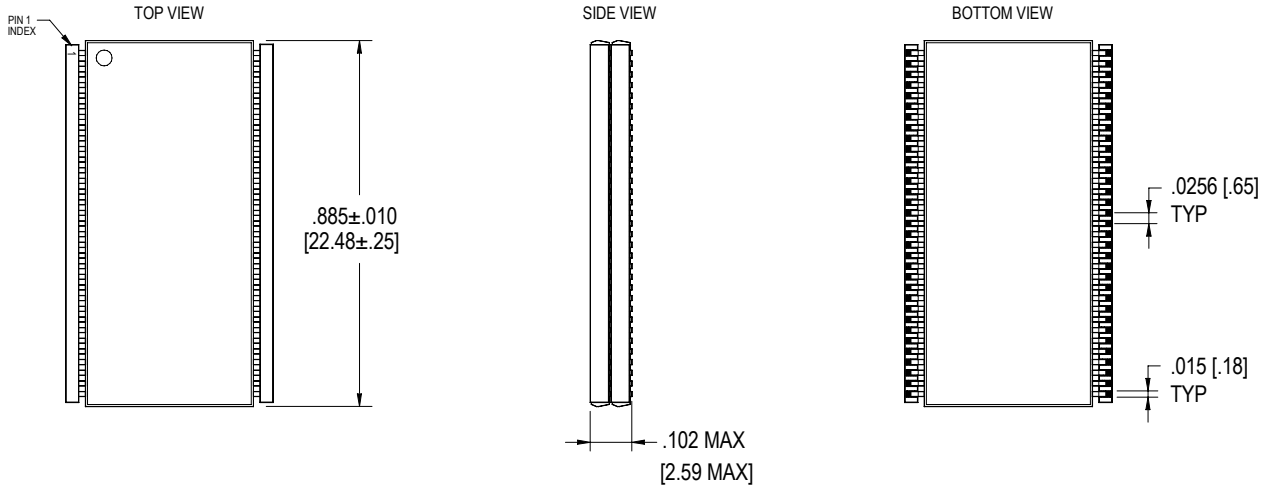
ORDERING INFORMATION

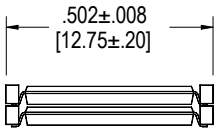
DP	DD	16M	X	8	R	S	A	Y5	-	DP	-	XX	XX	XX
PREFIX	TYPE	MEMORY DEPTH	DESIG	MEMORY WIDTH	DESIG	I/O TYPE	DEVICE WIDTH	PACKAGE		SUPPLIER		MFR ID	CYCLE TIME	CAS LATENCY

- CAS LATENCY
  - 15 CAS LATENCY 1.5
  - 20 CAS LATENCY 2.0
  - 25 CAS LATENCY 2.5
  - 30 CAS LATENCY 3.0
- CYCLE TIME
  - 60 6ns (166MHz)
  - 70 7ns (143MHz)
  - 75 7.5ns (133MHz)
  - 08 8ns (125MHz)
  - 10 10ns (100MHz)
- MFR ID: MANUFACTURER CODE*
- SUPPLIER: SUPPLIER CODE*
- PACKAGE: STACKABLE TSOP
- DEVICE WIDTH: x4 MEMORY BASED
- I/O TYPE: SSTL INPUTS/OUTPUTS
- DESIG: 64 MEGABIT BASED
- DESIG: MEMORY MODULE WITHOUT SUPPORT LOGIC
- TYPE: DOUBLE DATA RATE SYNCHRONOUS DRAM

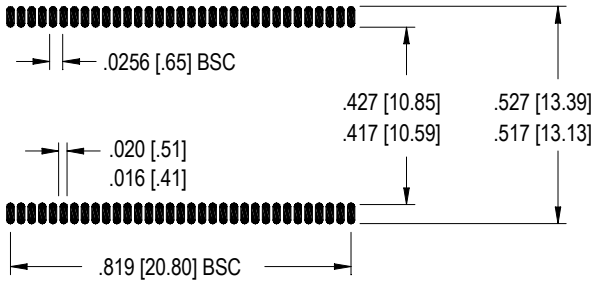
* Contact your sales representative for supplier and manufacturer codes.

MECHANICAL DRAWING





Standard TSOP pad layout is acceptable, however, when possible, the following pad layout is recommended for optimal manufacture and inspection. See Application Note 53A001-00 for further information.



PRELIMINARY

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