
Document Title

1Mx36 & 2Mx18-Bit Synchronous Burst SRAM

Revision History

<u>Rev.No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	1. Initial draft	May. 10. 2001	Preliminary
0.1	1. Add 165FBGA package	Aug. 29. 2001	Preliminary
0.2	1. Update JTAG scan order	Dec. 03. 2001	Preliminary
0.3	1. Change pin out for 165FBGA - x18/x36 ; 11B => from A to NC , 2R ==> from NC to A .	Feb. 14 . 2002	Preliminary
0.4	1. Insert pin at JTAG scan order of 165FBGA in connection with pin out change - x18/x36 ; insert Pin ID of 2R to <u>BIT</u> number of 69	Apr. 20. 2002	Preliminary
0.5	1. Add lcc, lsb, lsb1 and lsb2 values.	May. 10. 2002	Preliminary
1.0	1. Correct the pin name of 100TQFP.	Oct. 15. 2002	Final

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32Mb SB/SPB Synchronous SRAM Ordering Information

Org.	Part Number	Mode	VDD	Speed SB ; Access Time(ns) SPB ; Cycle Time(MHz)	PKG	Temp
2Mx18	K7B321825M-Q(H/F)C65/75/85	SB	3.3	6.5/7.5/8.5ns	Q: 100TQFP H: 119BGA F: 165FBGA	C (Commercial Temperature Range)
	K7A321800M-Q(H/F)C25/22/20/16/15/14	SPB(2E1D)	3.3	250/225/200/167/150/138MHz		
	K7A321801M-QC25/22/20/16/15/14	SPB(2E2D)	3.3	250/225/200/167/150/138MHz		
1Mx36	K7B323625M-Q(H/F)C65/75/85	SB	3.3	6.5/7.5/8.5ns		
	K7A323600M-Q(H/F)C25/22/20/16/15/14	SPB(2E1D)	3.3	250/225/200/167/150/138MHz		
	K7A323601M-QC25/22/20/16/15/14	SPB(2E2D)	3.3	250/225/200/167/150/138MHz		

1Mx36 & 2Mx18-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- 3.3V+0.165V/-0.165V Power Supply.
- I/O Supply Voltage 3.3V+0.165V/-0.165V for 3.3V I/O or 2.5V+0.4V/-0.125V for 2.5V I/O
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention only for TQFP.
- Asynchronous Output Enable Control.
- ADSP, ADSC, ADV Burst Control Pins.
- TTL-Level Three-State Output.
- 100-TQFP-1420A /119BGA(7x17 Ball Grid Array Package)
- 165FBGA(11x15 ball array) with body size of 15mmx17mm.

FAST ACCESS TIMES

PARAMETER	Symbol	-65	-75	-85	Unit
Cycle Time	tcyc	7.5	8.5	10	ns
Clock Access Time	tcd	6.5	7.5	8.5	ns
Output Enable Access Time	toE	3.5	3.5	4.0	ns

GENERAL DESCRIPTION

The K7B323625M and K7B321825M are 37,748,736-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 1M(2M) words of 36(18) bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; $\overline{GW}$, $\overline{BW}$, LBO, ZZ. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by $\overline{GW}$, and each byte write is performed by the combination of $\overline{WEx}$ and $\overline{BW}$ when $\overline{GW}$ is high. And with $\overline{CS}_1$ high, ADSP is blocked to control signals.

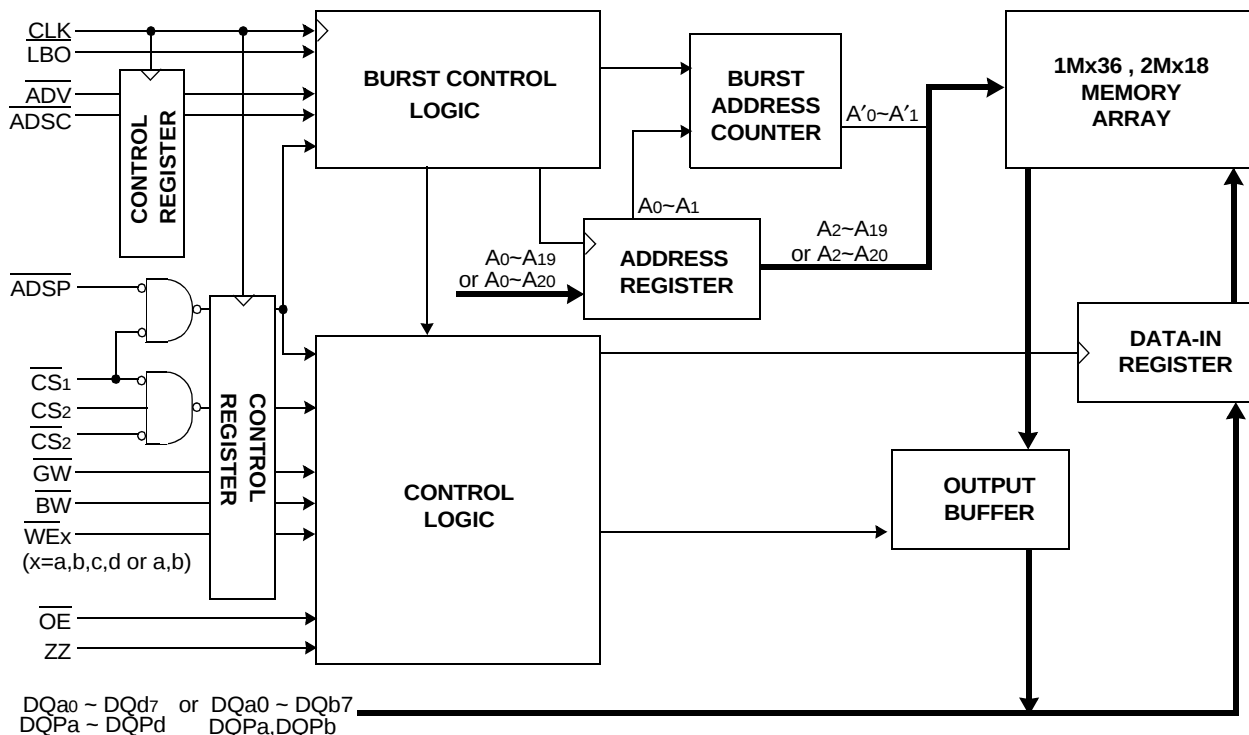
Burst cycle can be initiated with either the address status processor(ADSP) or address status cache controller(ADSC) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance(ADV) input.

LBO pin is DC operated and determines burst sequence(linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

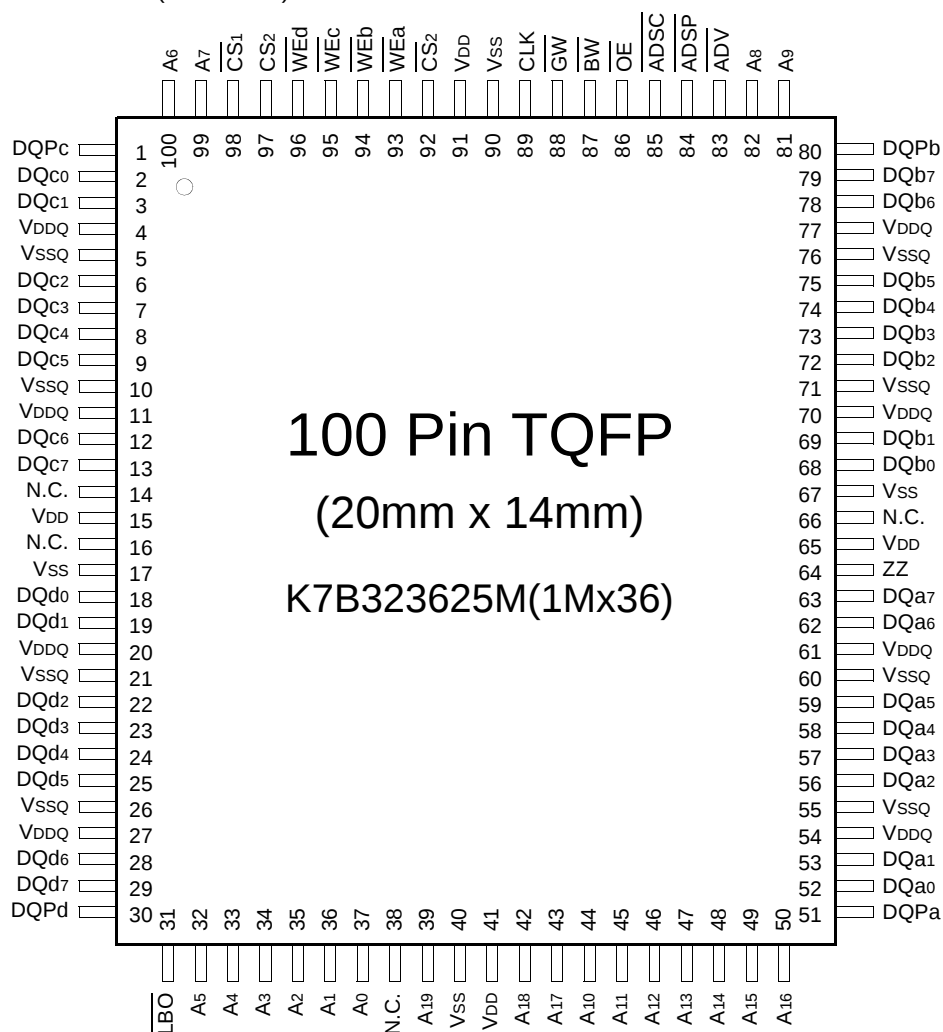
The K7B323625M and K7B321825M are fabricated using SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP, 119BGA and 165FBGA package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



1Mx36 & 2Mx18 Synchronous SRAM

PIN CONFIGURATION(TOP VIEW)

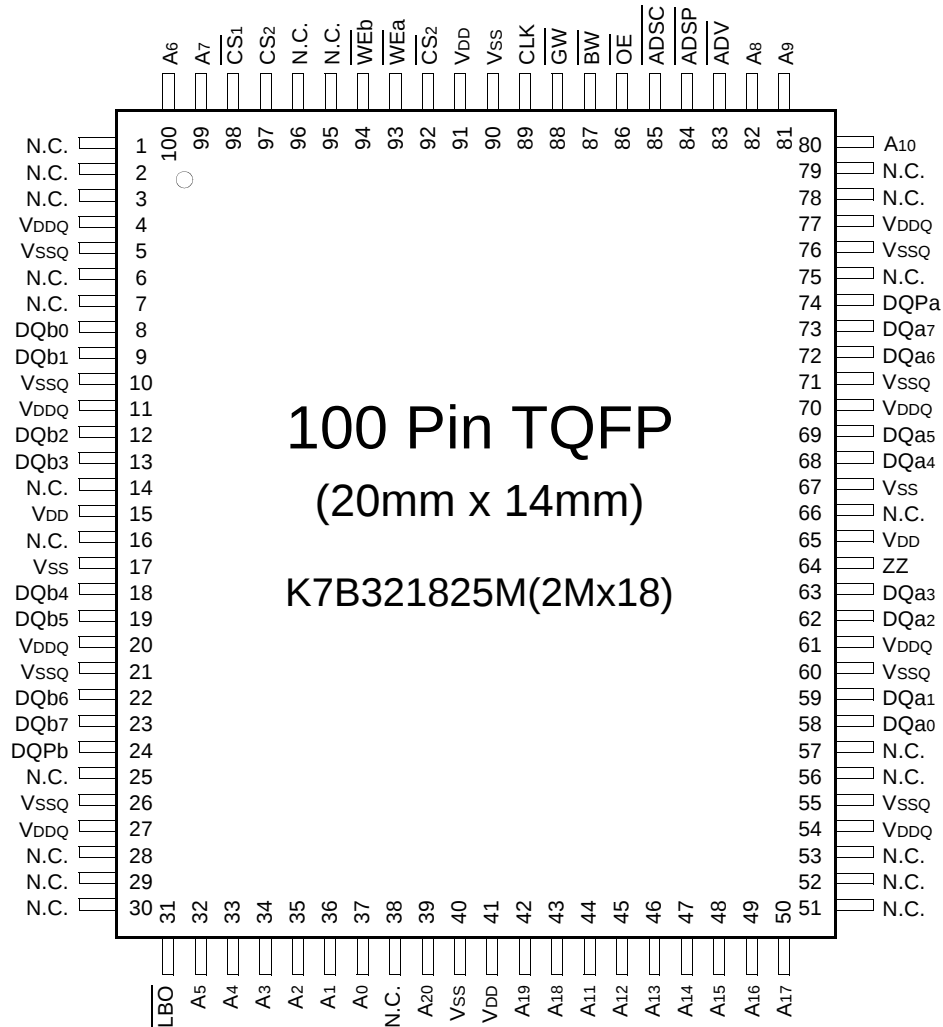


PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A19	Address Inputs	32,33,34,35,36,37,39 42,43,44,45,46,47,48, 49,50,81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
<u>ADV</u>	Burst Address Advance	83	N.C.	No Connect	14,16,38,66
<u>ADSP</u>	Address Status Processor	84			
<u>ADSC</u>	Address Status Controller	85	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
<u>CLK</u>	Clock	89	DQb0~b7		68,69,72,73,74,75,78,79
<u>CS1</u>	Chip Select	98	DQc0~c7		2,3,6,7,8,9,12,13
<u>CS2</u>	Chip Select	97	DQd0~d7		18,19,22,23,24,25,28,29
<u>CS2</u>	Chip Select	92	DQP a~Pd		51,80,1,30
<u>WEx(x=a,b,c,d)</u>	Byte Write Inputs	93,94,95,96			
<u>OE</u>	Output Enable	86	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
<u>GW</u>	Global Write Enable	88		(2.5V or 3.3V)	
<u>BW</u>	Byte Write Enable	87	VSSQ	Output Ground	5,10,21,26,55,60,71,76
<u>ZZ</u>	Power Down Input	64			
<u>LBO</u>	Burst Mode Control	31			

Notes : 1. A_0 and A_1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A20	Address Inputs	32,33,34,35,36,37,39 42,43,44,45,46,47,48, 49,50 80,81,82,99,100	VDD	Power Supply(+3.3V)	15,41,65,91
			VSS	Ground	17,40,67,90
			N.C.	No Connect	1,2,3,6,7,14,16,25,28,29, 30,38,51,52,53,56,57,66, 75,78,79,95,96
ADV	Burst Address Advance	83	DQa0 ~ a7	Data Inputs/Outputs	58,59,62,63,68,69,72,73
ADSP	Address Status Processor	84	DQb0 ~ b7		8,9,12,13,18,19,22,23
ADSC	Address Status Controller	85	DQPa, Pb		74,24
CLK	Clock	89			
CS1	Chip Select	98	VDDQ	Output Power Supply	4,11,20,27,54,61,70,77
CS2	Chip Select	97	VSSQ	(2.5V or 3.3V)	
CS2	Chip Select	92		Output Ground	5,10,21,26,55,60,71,76
WE(x=a,b)	Byte Write Inputs	93,94			
OE	Output Enable	86			
GW	Global Write Enable	88			
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

Notes : 1. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7B323625M(1Mx36)

	1	2	3	4	5	6	7
A	VDDQ	A	A	$\overline{\text{ADSP}}$	A	A	VDDQ
B	NC	A	A	$\overline{\text{ADSC}}$	A	A	NC
C	NC	A	A	VDD	A	A	NC
D	DQc	DQPc	VSS	NC	VSS	DQPb	DQb
E	DQc	DQc	VSS	$\overline{\text{CS}}_1$	VSS	DQb	DQb
F	VDDQ	DQc	VSS	$\overline{\text{OE}}$	VSS	DQb	VDDQ
G	DQc	DQc	$\overline{\text{WE}}_c$	$\overline{\text{ADV}}$	$\overline{\text{WE}}_b$	DQb	DQb
H	DQc	DQc	VSS	$\overline{\text{GW}}$	VSS	DQb	DQb
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	DQd	DQd	VSS	CLK	VSS	DQa	DQa
L	DQd	DQd	$\overline{\text{WE}}_d$	NC	$\overline{\text{WE}}_a$	DQa	DQa
M	VDDQ	DQd	VSS	$\overline{\text{BW}}$	VSS	DQa	VDDQ
N	DQd	DQd	VSS	A ₁ *	VSS	DQa	DQa
P	DQd	DQPd	VSS	A ₀ *	VSS	DQPa	DQa
R	NC	A	$\overline{\text{LBO}}$	VDD	NC	A	NC
T	NC	NC	A	A	A	A	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

Note : * A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	VDD	Power Supply(+3.3V)
A ₀ , A ₁	Burst Count Address	VSS	Ground
$\overline{\text{ADV}}$	Burst Address Advance	N.C.	No Connect
$\overline{\text{ADSP}}$	Address Status Processor		
$\overline{\text{ADSC}}$	Address Status Controller	DQa	Data Inputs/Outputs
CLK	Clock	DQb	Data Inputs/Outputs
$\overline{\text{CS}}_1$	Chip Select	DQc	Data Inputs/Outputs
$\overline{\text{WE}}_x$	Byte Write Inputs	DQd	Data Inputs/Outputs
(x=a,b,c,d)		DQPa~Pd	Data Inputs/Outputs
$\overline{\text{OE}}$	Output Enable		
$\overline{\text{GW}}$	Global Write Enable	VDDQ	Output Power Supply
$\overline{\text{BW}}$	Byte Write Enable		(2.5V or 3.3V)
$\overline{\text{ZZ}}$	Power Down Input		
$\overline{\text{LBO}}$	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7B321825M(2Mx18)

	1	2	3	4	5	6	7
A	V _{DDQ}	A	A	<u>ADSP</u>	A	A	V _{DDQ}
B	NC	A	A	<u>ADSC</u>	A	A	NC
C	NC	A	A	V _{DD}	A	A	NC
D	DQ _b	NC	V _{SS}	NC	V _{SS}	DQP _a	NC
E	NC	DQ _b	V _{SS}	<u>CS</u> ₁	V _{SS}	NC	DQ _a
F	V _{DDQ}	NC	V _{SS}	<u>OE</u>	V _{SS}	DQ _a	V _{DDQ}
G	NC	DQ _b	<u>WE</u> _b	<u>ADV</u>	V _{SS}	NC	DQ _a
H	DQ _b	NC	V _{SS}	<u>GW</u>	V _{SS}	DQ _a	NC
J	V _{DDQ}	V _{DD}	NC	V _{DD}	NC	V _{DD}	V _{DDQ}
K	NC	DQ _b	V _{SS}	CLK	V _{SS}	NC	DQ _a
L	DQ _b	NC	V _{SS}	NC	<u>WE</u> _a	DQ _a	NC
M	V _{DDQ}	DQ _b	V _{SS}	<u>BW</u>	V _{SS}	NC	V _{DDQ}
N	DQ _b	NC	V _{SS}	A ₁ *	V _{SS}	DQ _a	NC
P	NC	DQP _b	V _{SS}	A ₀ *	V _{SS}	NC	DQ _a
R	NC	A	<u>LBO</u>	V _{DD}	NC	A	NC
T	NC	A	A	A	A	A	ZZ
U	V _{DDQ}	TMS	TDI	TCK	TDO	NC	V _{DDQ}

Note : * A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	V _{DD}	Power Supply(+3.3V)
A ₀ ,A ₁	Burst Count Address	V _{SS}	Ground
<u>ADV</u>	Burst Address Advance	N.C.	No Connect
<u>ADSP</u>	Address Status Processor		
<u>ADSC</u>	Address Status Controller	DQ _a	Data Inputs/Outputs
CLK	Clock	DQ _b	Data Inputs/Outputs
<u>CS</u> ₁	Chip Select	DQP _a ~P _b	Data Inputs/Outputs
<u>WE</u> _x	Byte Write Inputs		
(x=a,b)		V _{DDQ}	Output Power Supply (2.5V or 3.3V)
<u>OE</u>	Output Enable		
<u>GW</u>	Global Write Enable		
<u>BW</u>	Byte Write Enable		
<u>ZZ</u>	Power Down Input		
<u>LBO</u>	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

165-PIN FBGA PACKAGE CONFIGURATIONS(TOP VIEW)

K7B323625M(1Mx36)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{\text{CS}}1$	$\overline{\text{WE}}c$	$\overline{\text{WE}}b$	$\overline{\text{CS}}2$	$\overline{\text{BW}}$	$\overline{\text{ADSC}}$	$\overline{\text{ADV}}$	A	NC
B	NC	A	CS2	$\overline{\text{WE}}d$	$\overline{\text{WE}}a$	CLK	$\overline{\text{GW}}$	$\overline{\text{OE}}$	$\overline{\text{ADSP}}$	A	NC
C	DQPc	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQPb
D	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
E	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
F	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
G	DQc	DQc	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQb	DQb
H	NC	VSS	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
K	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
L	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
M	DQd	DQd	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	DQa
N	DQPd	NC	VDDQ	VSS	NC	A	VSS	VSS	VDDQ	NC	DQPa
P	NC	NC	A	A	TDI	A ₁ *	TDO	A	A	A	A
R	$\overline{\text{LBO}}$	A	A	A	TMS	A ₀ *	TCK	A	A	A	A

Note : * A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	V _{DD}	Power Supply(+3.3V)
A ₀ , A ₁	Burst Count Address	V _{SS}	Ground
$\overline{\text{ADV}}$	Burst Address Advance	N.C.	No Connect
$\overline{\text{ADSP}}$	Address Status Processor		
$\overline{\text{ADSC}}$	Address Status Controller		
CLK	Clock	DQ _a	Data Inputs/Outputs
$\overline{\text{CS}}1$	Chip Select	DQ _b	Data Inputs/Outputs
$\overline{\text{WE}}x$	Byte Write Inputs	DQ _c	Data Inputs/Outputs
(x=a,b,c,d)		DQ _d	Data Inputs/Outputs
		DQPa~Pd	Data Inputs/Outputs
$\overline{\text{OE}}$	Output Enable		
$\overline{\text{GW}}$	Global Write Enable	V _{DDQ}	Output Power Supply
$\overline{\text{BW}}$	Byte Write Enable		(2.5V or 3.3V)
ZZ	Power Down Input		
$\overline{\text{LBO}}$	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

165-PIN FBGA PACKAGE CONFIGURATIONS(TOP VIEW)

K7B321825M(2Mx18)

	1	2	3	4	5	6	7	8	9	10	11
A	NC	A	$\overline{\text{CS1}}$	$\overline{\text{WEb}}$	NC	$\overline{\text{CS2}}$	$\overline{\text{BW}}$	$\overline{\text{ADSC}}$	$\overline{\text{ADV}}$	A	A
B	NC	A	CS2	NC	$\overline{\text{WEa}}$	CLK	$\overline{\text{GW}}$	$\overline{\text{OE}}$	$\overline{\text{ADSP}}$	A	NC
C	NC	NC	VDDQ	VSS	VSS	VSS	VSS	VSS	VDDQ	NC	DQPa
D	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
E	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
F	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
G	NC	DQb	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	NC	DQa
H	NC	VSS	NC	VDD	VSS	VSS	VSS	VDD	NC	NC	ZZ
J	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
K	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
L	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
M	DQb	NC	VDDQ	VDD	VSS	VSS	VSS	VDD	VDDQ	DQa	NC
N	DQPb	NC	VDDQ	VSS	NC	A	VSS	VSS	VDDQ	NC	NC
P	NC	NC	A	A	TDI	A ₁ *	TDO	A	A	A	A
R	$\overline{\text{LBO}}$	A	A	A	TMS	A ₀ *	TCK	A	A	A	A

Note : * A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	VDD	Power Supply(+3.3V)
A ₀ ,A ₁	Burst Count Address	Vss	Ground
$\overline{\text{ADV}}$	Burst Address Advance	N.C.	No Connect
$\overline{\text{ADSP}}$	Address Status Processor		
$\overline{\text{ADSC}}$	Address Status Controller	DQa	Data Inputs/Outputs
CLK	Clock	DQb	Data Inputs/Outputs
$\overline{\text{CS1}}$	Chip Select	DQPa~Pb	Data Inputs/Outputus
WEx	Byte Write Inputs		
(x=a,b)		VDDQ	Output Power Supply (2.5V or 3.3V)
$\overline{\text{OE}}$	Output Enable		
$\overline{\text{GW}}$	Global Write Enable		
$\overline{\text{BW}}$	Byte Write Enable		
$\overline{\text{ZZ}}$	Power Down Input		
LBO	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

FUNCTION DESCRIPTION

The K7B323625M and K7B321825M are synchronous SRAM designed to support the burst address accessing sequence of the Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and $\overline{ZZ}$) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$ and chip select pins.

The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with $\overline{ADV}$.

When $\overline{ZZ}$ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When $\overline{ZZ}$ returns to low, the SRAM normally operates after 2cycles of wake up time. $\overline{ZZ}$ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$ (or $\overline{ADSC}$) using the new external address clocked into the on-chip address register when both $\overline{GW}$ and $\overline{BW}$ are high or when $\overline{BW}$ is low and $\overline{WEa}$, $\overline{WEb}$, $\overline{WEc}$, and $\overline{WEd}$ are high. When $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. the data of cell array accessed by the current address are projected to the output pins.

Write cycles are also initiated with $\overline{ADSP}$ (or $\overline{ADSC}$) and are differentiated into two kinds of operations; All byte write operation and individual byte write operation.

All byte write occurs by enabling $\overline{GW}$ (independent of $\overline{BW}$ and $\overline{WEx}$), and individual byte write is performed only when $\overline{GW}$ is high and $\overline{BW}$ is low. In K7B163625M, a 512Kx36 organization, $\overline{WEa}$ controls DQa0 ~ DQa7 and DQPa, $\overline{WEb}$ controls DQb0 ~ DQb7 and DQ Pb, $\overline{WEc}$ controls DQc0 ~ DQc7 and DQ Pc and $\overline{WEd}$ controls DQd0 ~ DQd7 and DQ Pd.

$\overline{CS1}$ is used to enable the device and conditions internal use of $\overline{ADSP}$ and is sampled only when a new external address is loaded.

$\overline{ADV}$ is ignored at the clock edge when $\overline{ADSP}$ is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{ADV}$ is sampled low.

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. And this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A ₁	A ₀	A ₁	A ₀	A ₁	A ₀	A ₁	A ₀
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	0	0	1	1	1	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A ₁	A ₀	A ₁	A ₀	A ₁	A ₀	A ₁	A ₀
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	1	0	1	1	0	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	0	0	0	1	1	0

Note : 1. $\overline{LBO}$ pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS}_1$	$\overline{CS}_2$	$\overline{CS}_2$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

- Notes :** 1. X means "Don't Care". 2. The rising edge of clock is symbolized by ↑.
3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
 $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.
4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE(x36)

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	OPERATION
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTES
L	X	X	X	X	X	WRITE ALL BYTES

- Notes :** 1. X means "Don't Care".
2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

WRITE TRUTH TABLE(x18)

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	OPERATION
H	H	X	X	READ
H	L	H	H	READ
H	L	L	H	WRITE BYTE a
H	L	H	L	WRITE BYTE b
H	L	L	L	WRITE ALL BYTES
L	X	X	X	WRITE ALL BYTES

- Notes :** 1. X means "Don't Care".
2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

Operation	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on VDD Supply Relative to VSS	VDD	-0.3 to 4.6	V
Voltage on VDDQ Supply Relative to VSS	VDDQ	VDD	V
Voltage on Input Pin Relative to VSS	VIN	-0.3 to VDD+0.3	V
Voltage on I/O Pin Relative to VSS	VIO	-0.3 to VDDQ+0.3	V
Power Dissipation	PD	1.6	W
Storage Temperature	TSTG	-65 to 150	°C
Operating Temperature	TOPR	0 to 70	°C
Storage Temperature Range Under Bias	TBIAS	-10 to 85	°C

*Notes : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS at 3.3V I/O (0°C ≤ TA ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	VDD	3.135	3.3	3.465	V
	VDDQ	3.135	3.3	3.465	V
Ground	VSS	0	0	0	V

OPERATING CONDITIONS at 2.5V I/O (0°C ≤ TA ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	VDD	3.135	3.3	3.465	V
	VDDQ	2.375	2.5	2.9	V
Ground	VSS	0	0	0	V

CAPACITANCE* (TA=25°C, f=1MHz)

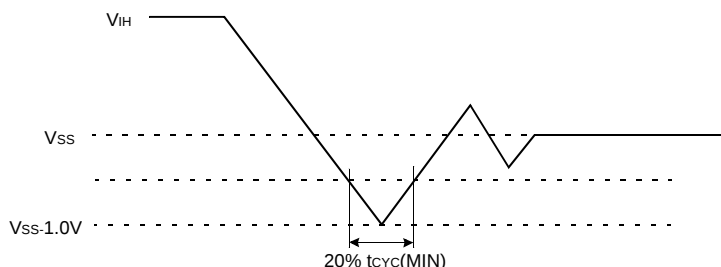
PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	CIN	VIN=0V	-	5	pF
Output Capacitance	COUT	VOU=0V	-	7	pF

*Note : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS($V_{DD}=3.3V+0.165V/-0.165V$, $T_A=0^{\circ}C$ to $+70^{\circ}C$)

Parameter	Symbol	Test Conditions	Min	Max	Unit	Notes
Input Leakage Current(except ZZ)	I_{IL}	$V_{DD}=Max$; $V_{IN}=V_{SS}$ to V_{DD}	-2	+2	μA	
Output Leakage Current	I_{OL}	Output Disabled, $V_{out}=V_{SS}$ to V_{DDQ}	-2	+2	μA	
Operating Current	I_{CC}	Device Selected, $I_{OUT}=0mA$, $ZZ \leq V_{IL}$, Cycle Time $\geq t_{CYC}$ Min	-65	-	310	mA 1,2
			-75	-	290	
			-85	-	270	
Standby Current	I_{SB}	Device deselected, $I_{OUT}=0mA$, $ZZ \leq V_{IL}$, $f=Max$, All Inputs $\leq 0.2V$ or $\geq V_{DD}-0.2V$	-65	-	100	mA
			-75	-	90	
			-85	-	80	
	I_{SB1}	Device deselected, $I_{OUT}=0mA$, $ZZ \leq 0.2V$, $f=0$, All Inputs=fixed ($V_{DD}-0.2V$ or $0.2V$)	-	70	mA	
	I_{SB2}	Device deselected, $I_{OUT}=0mA$, $ZZ \geq V_{DD}-0.2V$, $f=Max$, All Inputs $\leq V_{IL}$ or $\geq V_{IH}$	-	60	mA	
Output Low Voltage(3.3V I/O)	V_{OL}	$I_{OL}=8.0mA$	-	0.4	V	
Output High Voltage(3.3V I/O)	V_{OH}	$I_{OH}=-4.0mA$	2.4	-	V	
Output Low Voltage(2.5V I/O)	V_{OL}	$I_{OL}=1.0mA$	-	0.4	V	
Output High Voltage(2.5V I/O)	V_{OH}	$I_{OH}=-1.0mA$	2.0	-	V	
Input Low Voltage(3.3V I/O)	V_{IL}		-0.3*	0.8	V	
Input High Voltage(3.3V I/O)	V_{IH}		2.0	$V_{DD}+0.3^{**}$	V	3
Input Low Voltage(2.5V I/O)	V_{IL}		-0.3*	0.7	V	
Input High Voltage(2.5V I/O)	V_{IH}		1.7	$V_{DD}+0.3^{**}$	V	3

Notes : 1. Reference AC Operating Conditions and Characteristics for input and timing.
2. Data states are all zero.
3. In Case of I/O Pins, the Max. $V_{IH}=V_{DDQ}+0.3V$



TEST CONDITIONS

($V_{DD}=3.3V+0.165V/-0.165V$, $V_{DDQ}=3.3V+0.165V/-0.165V$ or $V_{DD}=3.3V+0.165V/-0.165V$, $V_{DDQ}=2.5V+0.4V/-0.125V$, $T_A=0$ to $70^{\circ}C$)

PARAMETER	VALUE
Input Pulse Level(for 3.3V I/O)	0 to 3.0V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80% for 3.3V I/O)	1.0V/ns
Input Rise and Fall Time(Measured at 20% to 80% for 2.5V I/O)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	$V_{DDQ}/2$
Output Load	See Fig. 1

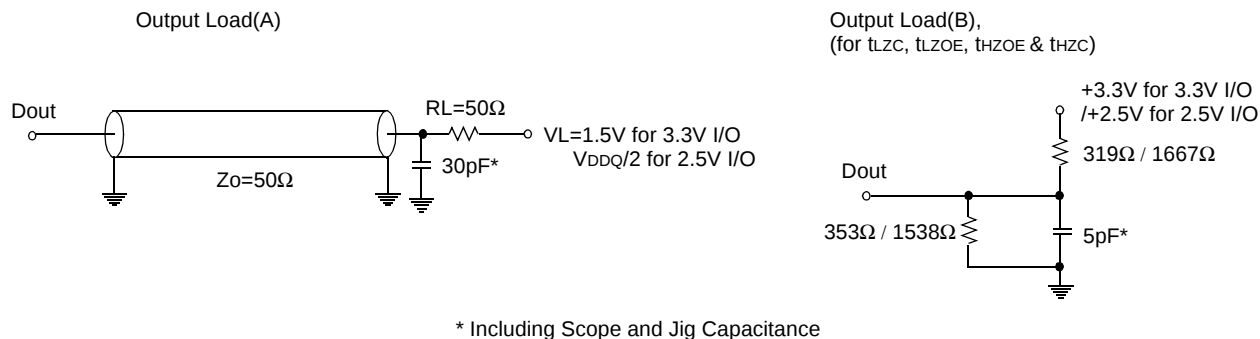


Fig. 1

AC TIMING CHARACTERISTICS($V_{DD}=3.3V+0.165V/-0.165V$, $T_A=0^{\circ}C$ to $+70^{\circ}C$)

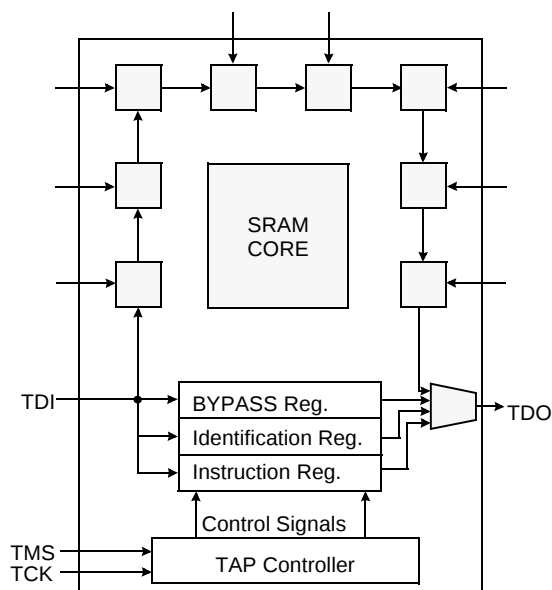
PARAMETER	SYMBOL	-65		-75		-85		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	tCYC	7.5	-	8.5	-	10	-	ns
Clock Access Time	tCD	-	6.5	-	7.5	-	8.5	ns
Output Enable to Data Valid	tOE	-	3.5	-	3.5	-	4.0	ns
Clock High to Output Low-Z	tLZC	2.5	-	2.5	-	2.5	-	ns
Output Hold from Clock High	tOH	2.5	-	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	tLZOE	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	tHZOE	-	3.5	-	3.5	-	4.0	ns
Clock High to Output High-Z	tHZC	-	3.8	-	4.0	-	5.0	ns
Clock High Pulse Width	tCH	2.2	-	2.5	-	3.0	-	ns
Clock Low Pulse Width	tCL	2.2	-	2.5	-	3.0	-	ns
Address Setup to Clock High	tAS	1.5	-	2.0	-	2.0	-	ns
Address Status Setup to Clock High	tSS	1.5	-	2.0	-	2.0	-	ns
Data Setup to Clock High	tDS	1.5	-	2.0	-	2.0	-	ns
Write Setup to Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WEx}$)	tWS	1.5	-	2.0	-	2.0	-	ns
Address Advance Setup to Clock High	tADVS	1.5	-	2.0	-	2.0	-	ns
Chip Select Setup to Clock High	tCSS	1.5	-	2.0	-	2.0	-	ns
Address Hold from Clock High	tAH	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	tSH	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	tDH	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WEx}$)	tWH	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	tADVH	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	tCSH	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	tPDS	2	-	2	-	2	-	cycle
ZZ Low to Power Up	tPUS	2	-	2	-	2	-	cycle

Notes : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.
3. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clock after leaving ZZ state.

IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to VDD through a resistor. TDO should be left unconnected.

JTAG Block Diagram



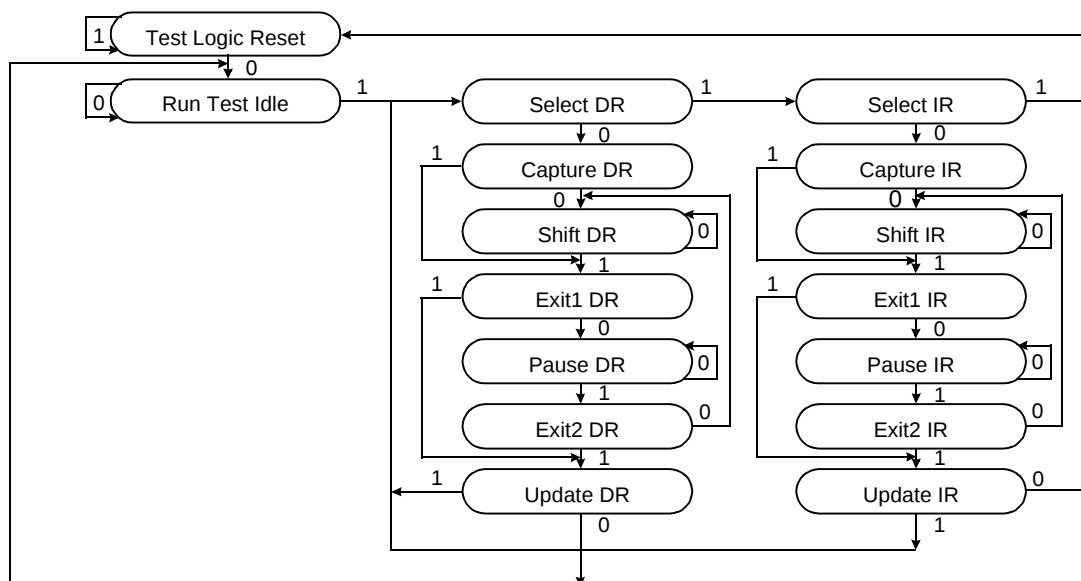
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	EXTEST	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	3
0	1	0	SAMPLE-Z	Boundary Scan Register	2
0	1	1	BYPASS	Bypass Register	4
1	0	0	SAMPLE	Boundary Scan Register	5
1	0	1	RESERVED	Do Not Use	6
1	1	0	BYPASS	Bypass Register	4
1	1	1	BYPASS	Bypass Register	4

NOTE :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs. This instruction is not IEEE 1149.1 compliant.
2. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
3. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
4. Bypass register is initiated to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
5. SAMPLE instruction dose not places DQs in Hi-Z.
6. This instruction is reserved for future use.

TAP Controller State Diagram



SCAN INFORMATION (119 BGA)

SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
1Mx36	3 bits	1 bits	32 bits	77 bits
2Mx18	3 bits	1 bits	32 bits	77 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
1Mx36	0000	01000 00100	XXXXXX	00001001110	1
2Mx18	0000	01001 00011	XXXXXX	00001001110	1

BOUNDARY SCAN EXIT ORDER

BIT	PIN ID(x18)	PIN ID(x36)
1	4H	4H
2	4T	4T
3	5T	5T
4	6T	6T
5	5L	5L
6	6R	6R
7	5R	5R
8	7R	7R
9	5J	5J
10	7T	7T
11	6P	6P
12	7N	7N
13	6M	6M
14	7L	7L
15	6K	6K
16	7P	7P
17	6N	6N
18	6L	6L
19	7K	7K
20	6H	6H
21	7G	7G
22	6F	6F
23	7E	7E
24	6D	7D
25	7H	7H
26	6G	6G
27	6E	6E
28	7D	6D
29	7B	7B
30	6C	6C
31	6A	6A
32	5C	5C
33	5B	5B
34	5G	5G
35	6B	6B
36	4F	4F
37	4M	4M
38	5A	5A
39	4K	4K

BIT	PIN ID(x18)	PIN ID(x36)
40	4B	4B
41	4E	4E
42	4G	4G
43	4A	4A
44	3G	3G
45	3C	3C
46	2B	2B
47	3B	3B
48	3A	3A
49	2C	2C
50	2A	2A
51	1B	1B
52	2D	2D
53	1E	1E
54	2F	2F
55	1G	1G
56	2H	2H
57	1D	1D
58	2E	2E
59	2G	2G
60	1H	1H
61	2K	2K
62	1L	1L
63	2M	2M
64	1N	1N
65	2P	1P
66	1K	1K
67	2L	2L
68	2N	2N
69	1P	2P
70	1T	2T
71	3R	3R
72	2T	1T
73	3L	3L
74	2R	2R
75	3T	3T
76	4N	4N
77	4P	4P

Note: 1. NC and Vss pins included in the scan exit order are read as "X" (i.e. don't care).

SCAN INFORMATION (165 FBGA)

SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
1Mx36	3 bits	1 bits	32 bits	75 bits
2Mx18	3 bits	1 bits	32 bits	75 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
1Mx36	0000	01000 00100	XXXXXX	00001001110	1
2Mx18	0000	01001 00011	XXXXXX	00001001110	1

BOUNDARY SCAN EXIT ORDER

BIT	PIN ID(x18)	PIN ID(x36)
1	6N	6N
2	8P	8P
3	8R	8R
4	9R	9R
5	9P	9P
6	10P	10P
7	10R	10R
8	11R	11R
9	11P	11P
10	11H	11H
11	11N	11N
12	11M	11M
13	11L	11L
14	11K	11K
15	11J	11J
16	10M	10M
17	10L	10L
18	10K	10K
19	10J	10J
20	11G	11G
21	11F	11F
22	11E	11E
23	11D	11D
24	11C	10G
25	10F	10F
26	10E	10E
27	10D	10D
28	10G	11C
29	11A	11A
30	11B	11B
31	10A	10A
32	10B	10B
33	9A	9A
34	9B	9B
35	8A	8A
36	8B	8B
37	7A	7A
38	7B	7B
39	6B	6B

BIT	PIN ID(x18)	PIN ID(x36)
40	6A	6A
41	5B	5B
42	5A	5A
43	4A	4A
44	4B	4B
45	3B	3B
46	3A	3A
47	2A	2A
48	2B	2B
49	1B	1B
50	1A	1A
51	1C	1C
52	1D	1D
53	1E	1E
54	1F	1F
55	1G	1G
56	2D	2D
57	2E	2E
58	2F	2F
59	2G	2G
60	1J	1J
61	1K	1K
62	1L	1L
63	1M	1M
64	1N	2J
65	2K	2K
66	2L	2L
67	2M	2M
68	2J	1N
69	2R	2R
70	1R	1R
71	3P	3P
72	3R	3R
73	4R	4R
74	4P	4P
75	6P	6P
76	6R	6R

Note: 1. NC and Vss pins included in the scan exit order are read as "X" (i.e. don't care).

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V _{DD}	3.135	3.3	3.465	V	
Input High Level (3.3V I/O / 2.5V I/O)	V _{IH}	2.0 / 1.7	-	V _{DD} +0.3	V	
Input Low Level (3.3V I/O / 2.5V I/O)	V _{IL}	-0.3	-	0.8 / 0.7	V	
Output High Voltage(3.3V I/O / 2.5V I/O)	V _{OH}	2.4 / 2.0	-	-	V	
Output Low Voltage(3.3V I/O / 2.5V I/O)	V _{OL}	-	-	0.4 / 0.4	V	

NOTE : The input level of SRAM pin is to follow the SRAM DC specification.

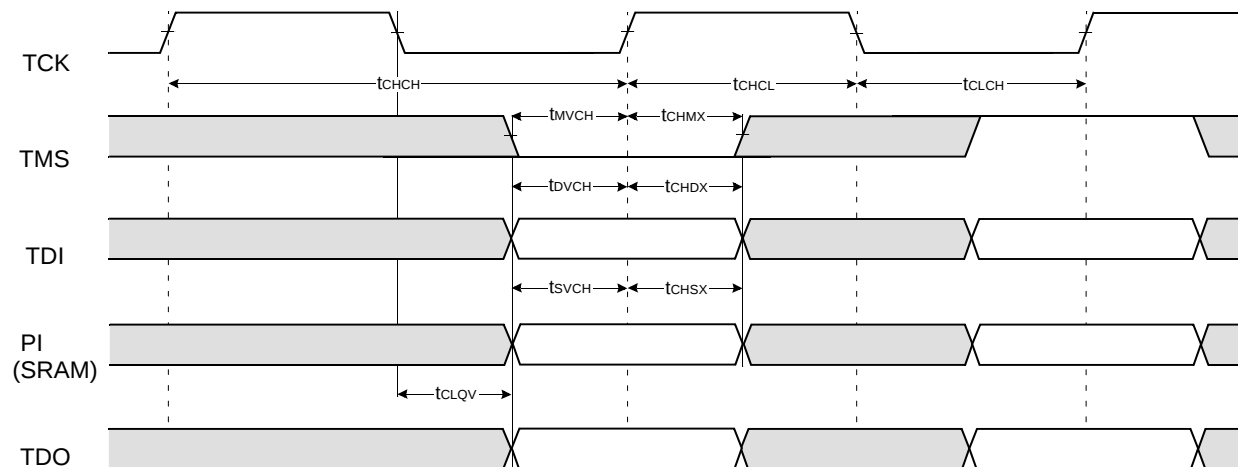
JTAG AC TEST CONDITIONS

Parameter	Symbol	Min	Unit	Note
Input High/Low Level(3.3V I/O , 2.5V I/O)	V _{IH} /V _{IL}	3.0/0 , 2.5/0	V	
Input Rise/Fall Time(3.3V I/O , 2.5V I/O)	TR/TF	1.0/1.0 , 1.0/1.0	ns	
Input and Output Timing Reference Level		V _{DDQ} /2	V	

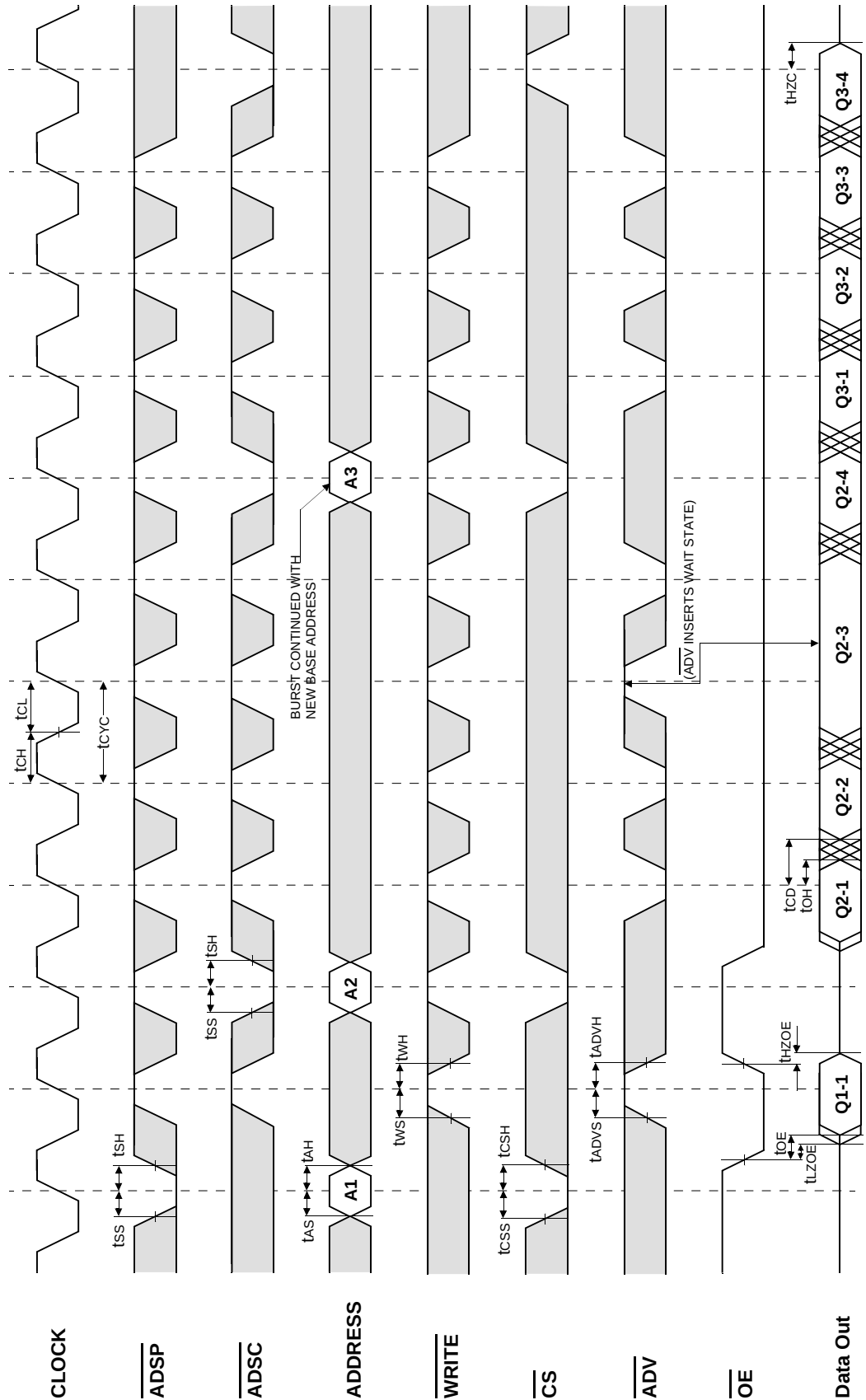
JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t _{CHCH}	50	-	ns	
TCK High Pulse Width	t _{CHCL}	20	-	ns	
TCK Low Pulse Width	t _{CLCH}	20	-	ns	
TMS Input Setup Time	t _{MVCH}	5	-	ns	
TMS Input Hold Time	t _{CHMX}	5	-	ns	
TDI Input Setup Time	t _{DVCH}	5	-	ns	
TDI Input Hold Time	t _{CHDX}	5	-	ns	
SRAM Input Setup Time	t _{SVCH}	5	-	ns	
SRAM Input Hold Time	t _{CHSX}	5	-	ns	
Clock Low to Output Valid	t _{CLQV}	0	10	ns	

JTAG TIMING DIAGRAM

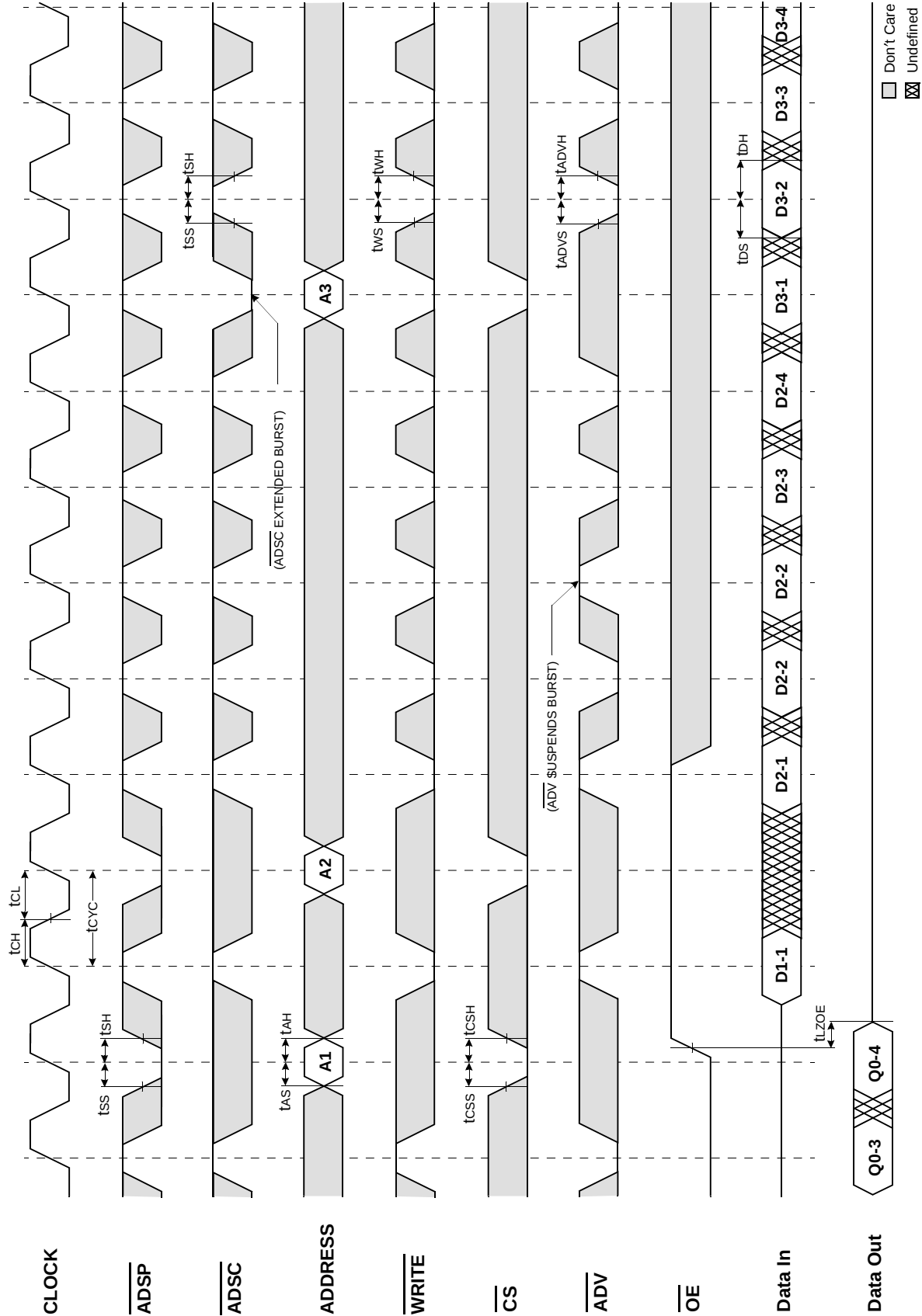


TIMING WAVEFORM OF READ CYCLE

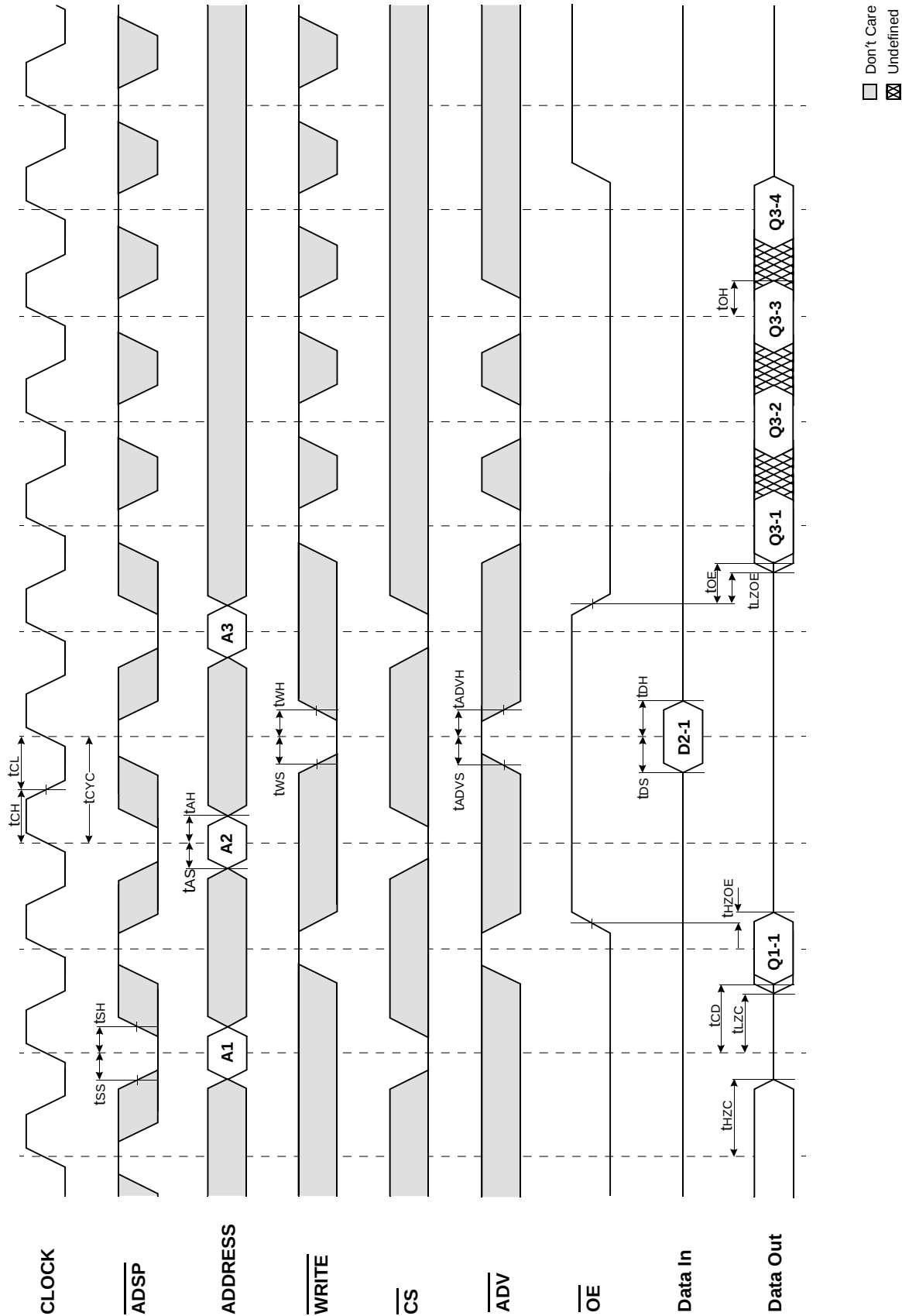


NOTES : $\overline{WRITE} = L$ means $\overline{GW} = L$, or $\overline{GW} = H$, $\overline{BW} = L$, $\overline{WE} = L$
 $\overline{CS} = L$ means $\overline{CS}_1 = L$, $\overline{CS}_2 = H$ and $\overline{CS}_2 = L$
 $\overline{CS} = H$ means $\overline{CS}_1 = H$, or $\overline{CS}_1 = L$ and $\overline{CS}_2 = H$, or $\overline{CS}_1 = L$, and $\overline{CS}_2 = L$

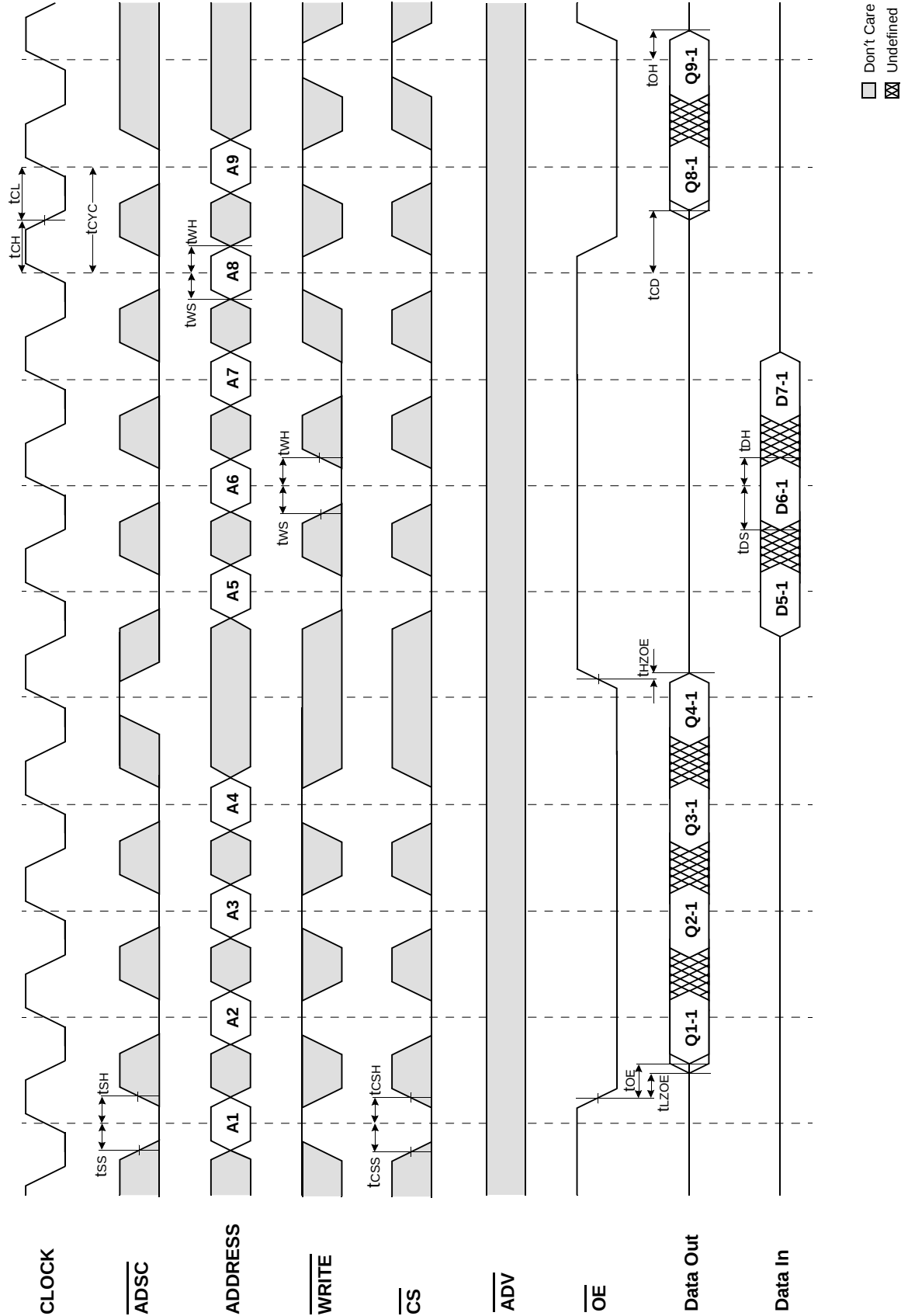
TIMING WAVEFORM OF WRTE CYCLE



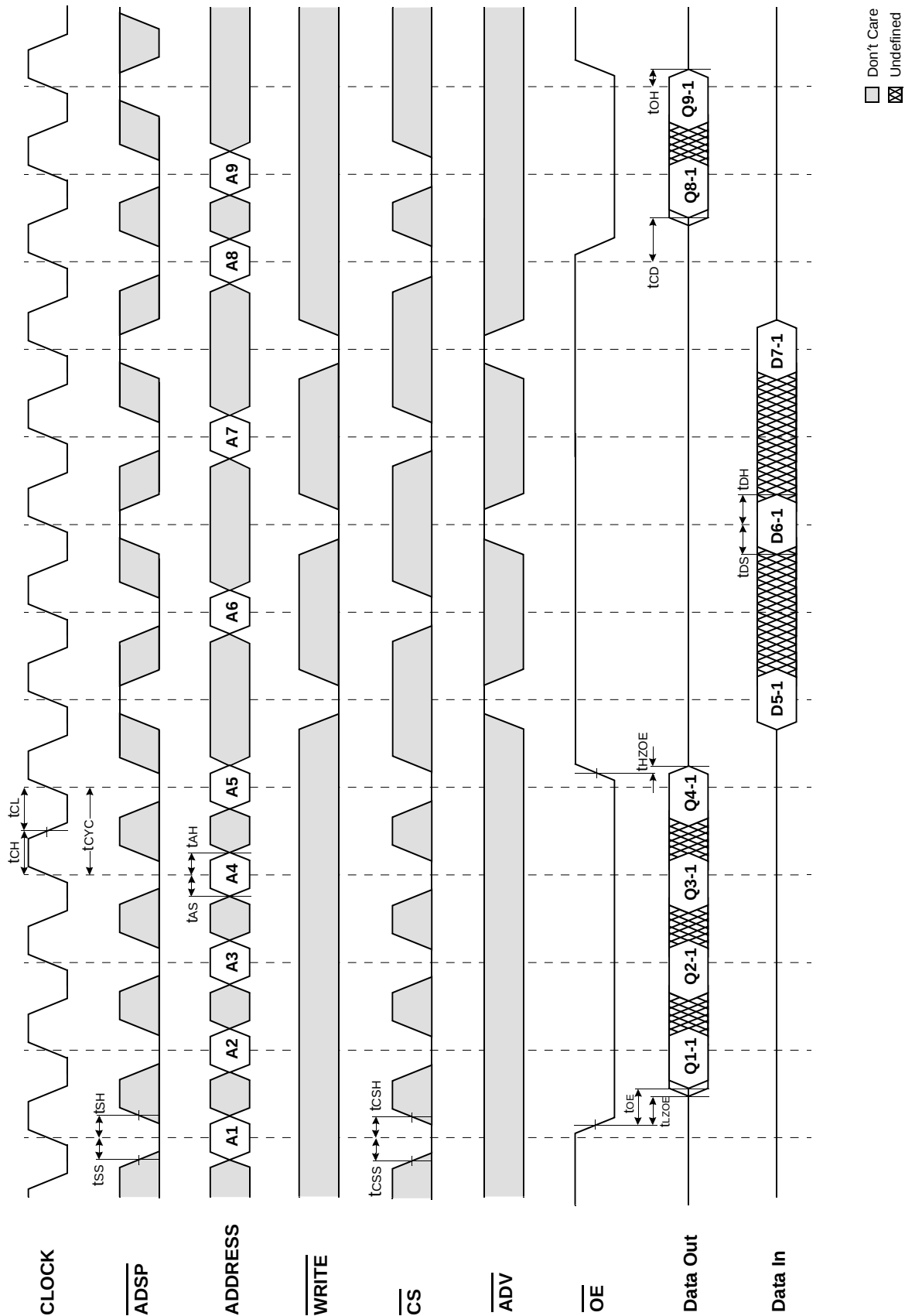
TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE(ADSP CONTROLLED, ADSC=HIGH)



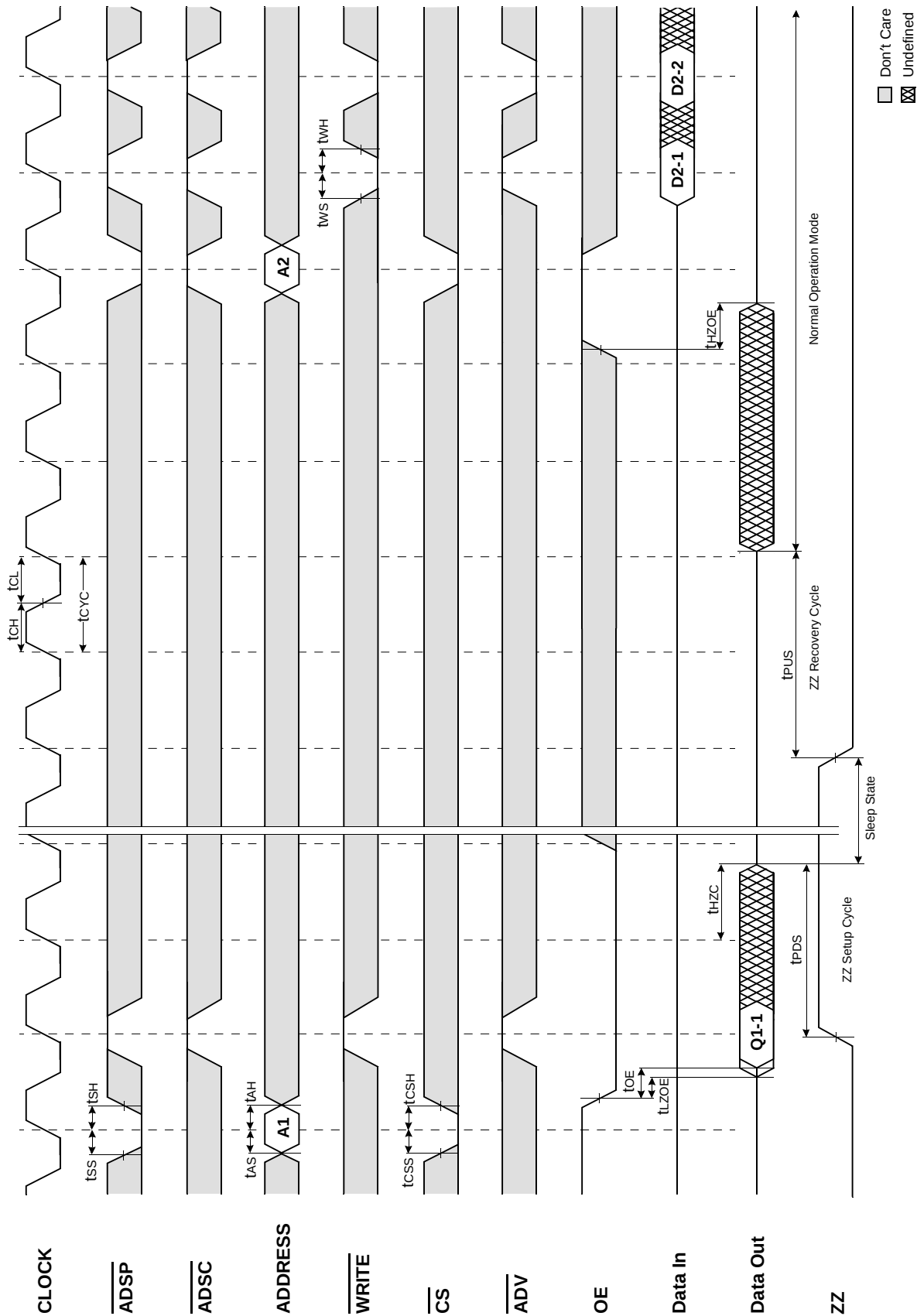
TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSC CONTROLLED, ADSP=HIGH)



TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSP CONTROLLED, ADSC=HIGH)



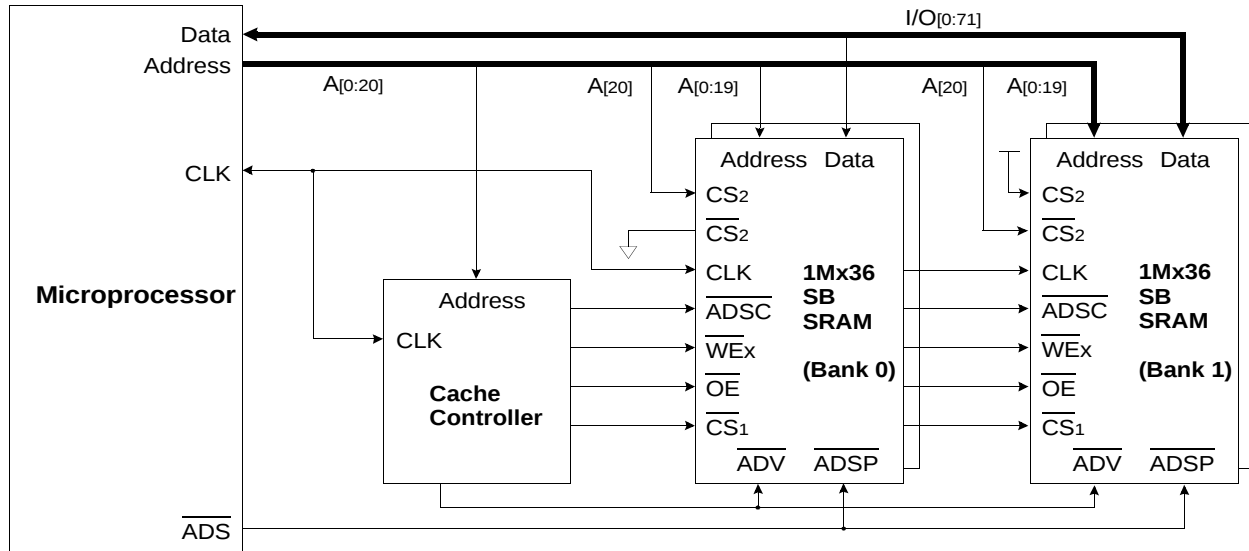
TIMING WAVEFORM OF POWER DOWN CYCLE



APPLICATION INFORMATION

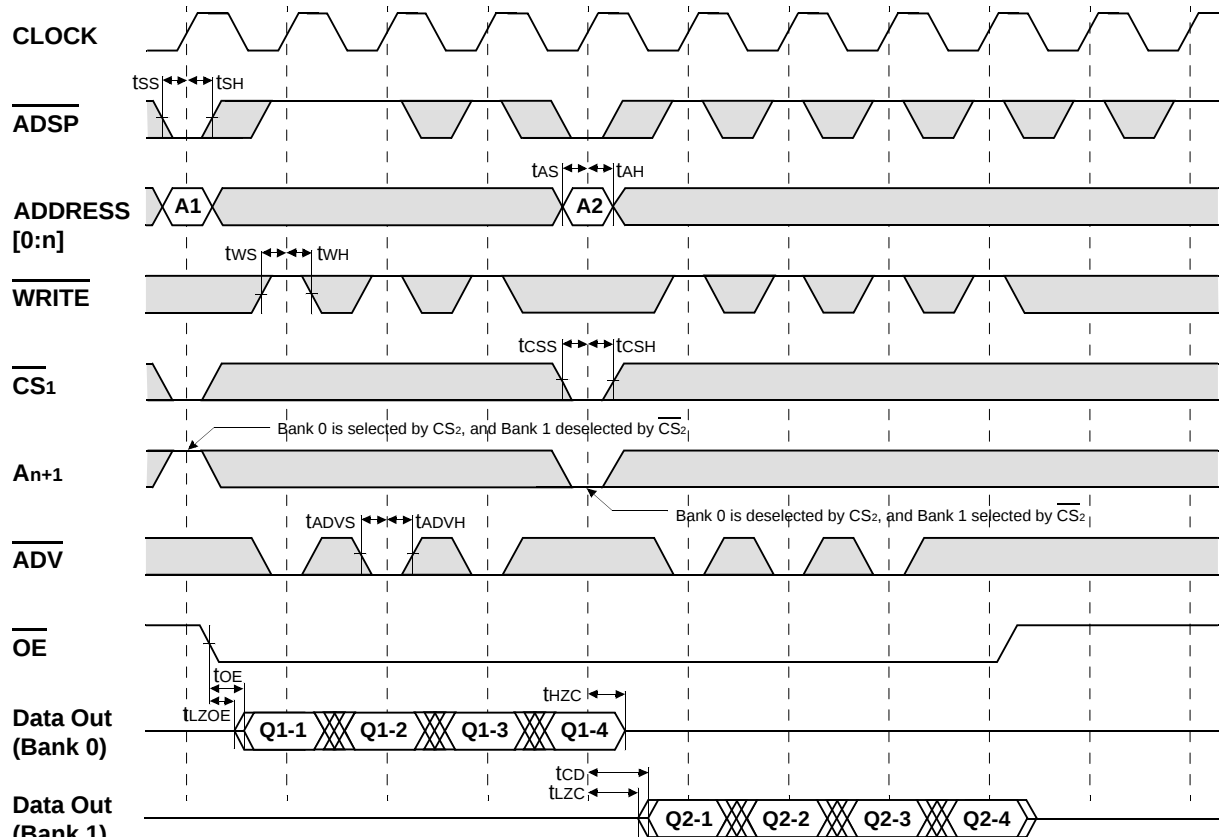
DEPTH EXPANSION

The Samsung 1Mx36 Synchronous Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 1M depth to 2M depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

(ADSP CONTROLLED , ADSC=HIGH)



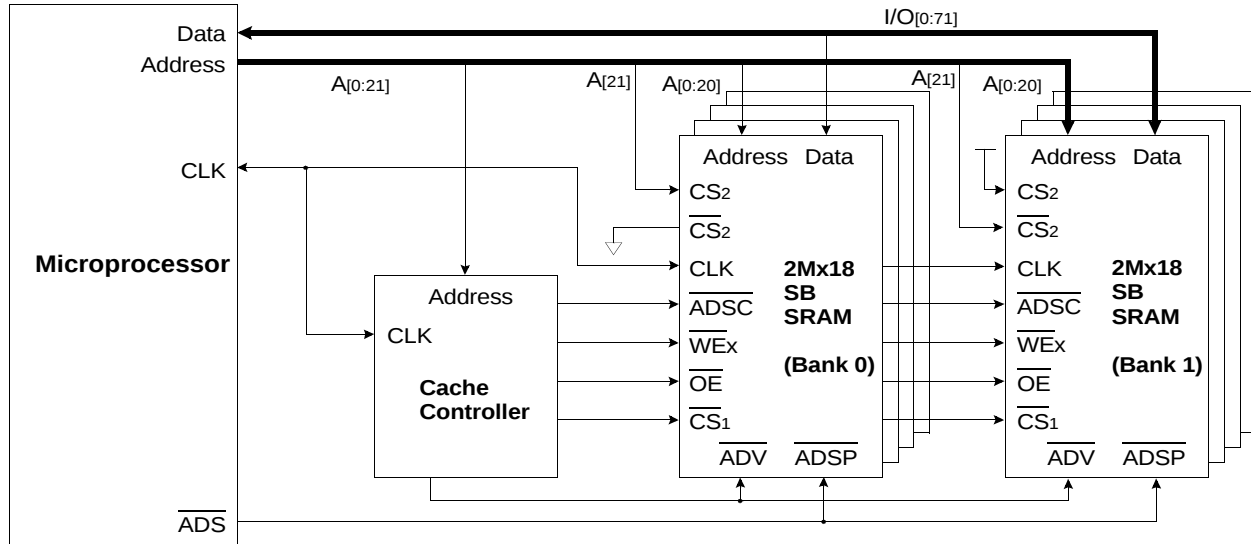
*Notes : n = 14 32K depth , 15 64K depth
16 128K depth , 17 256K depth
18 512K depth , 19 1M depth

□ Don't Care ⊗ Undefined

APPLICATION INFORMATION

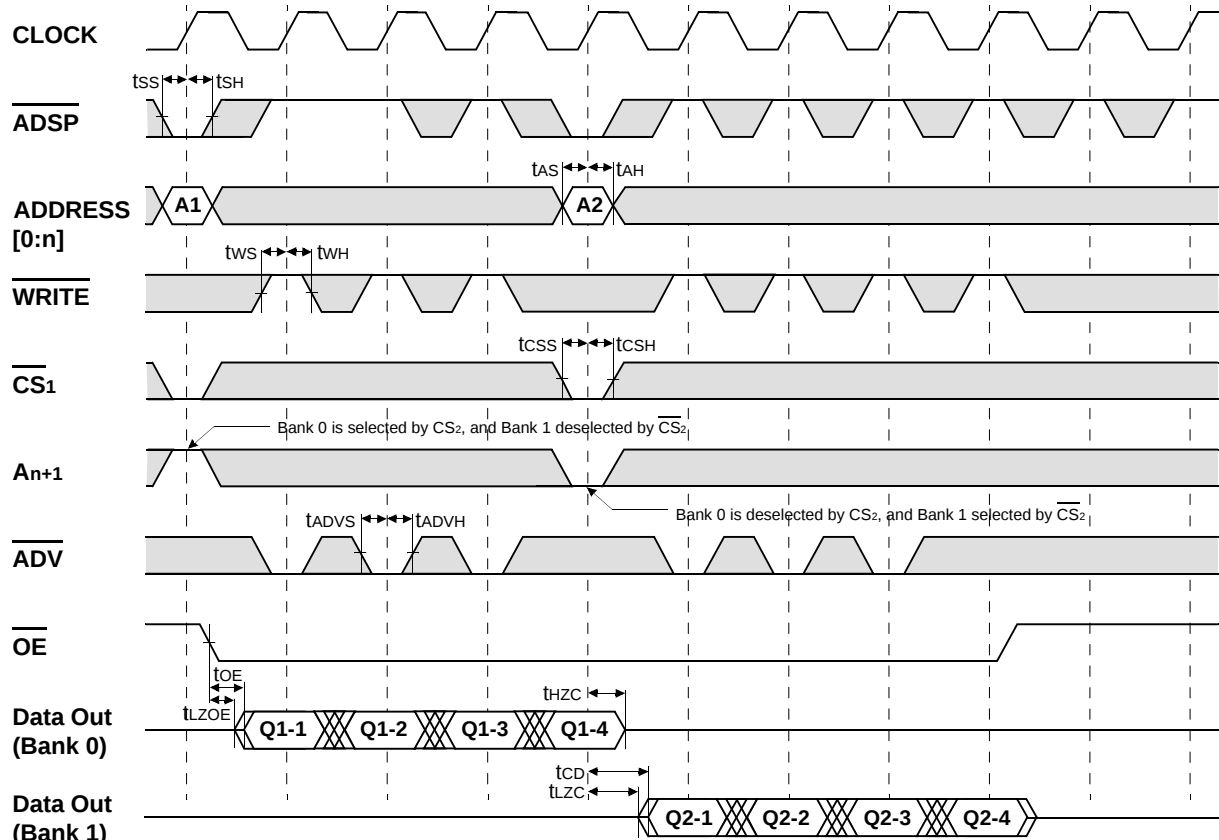
DEPTH EXPANSION

The Samsung 2Mx18 Synchronous Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 2M depth to 4M depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

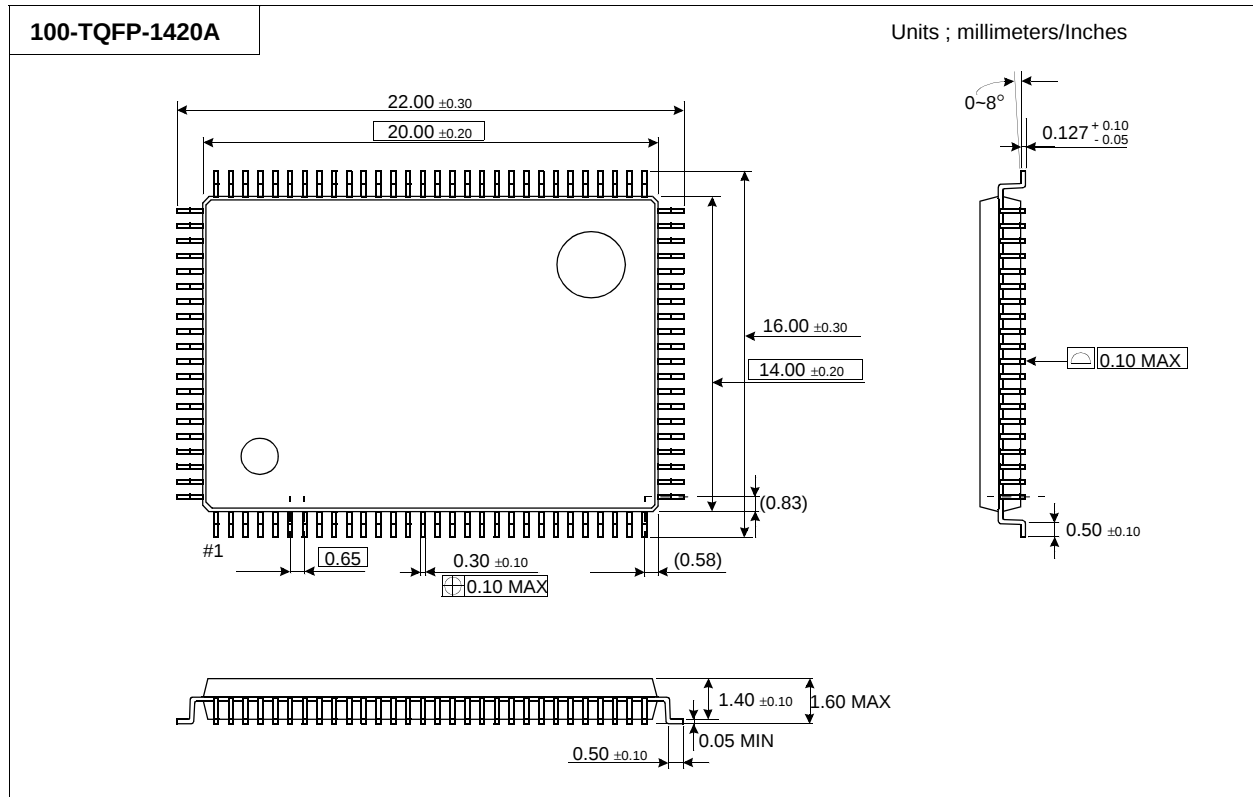
(ADSP CONTROLLED, ADSC=HIGH)



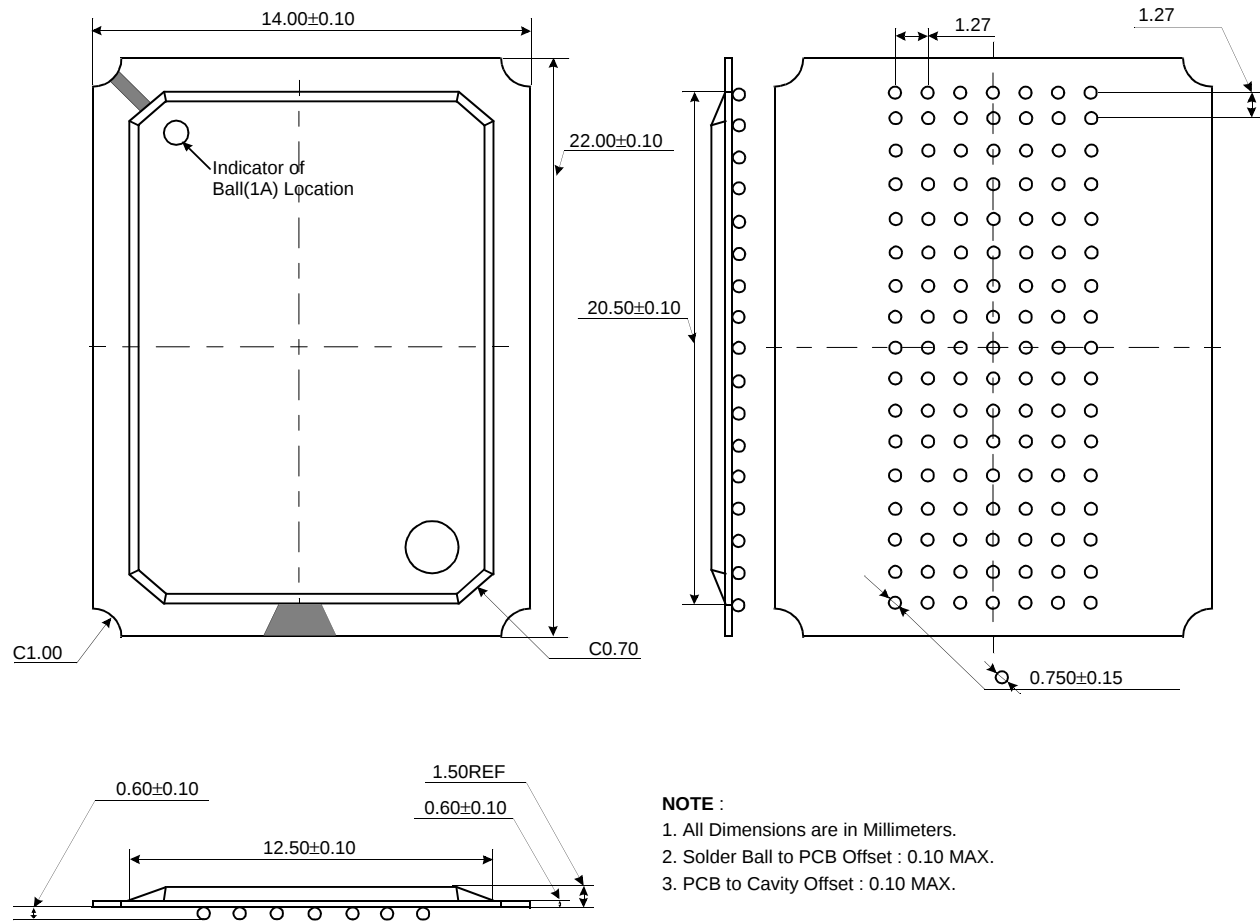
*Notes : n = 14 32K depth, 15 64K depth
 16 128K depth, 17 256K depth
 18 512K depth, 19 1M depth
 20 2M depth

□ Don't Care ⊗ Undefined

PACKAGE DIMENSIONS

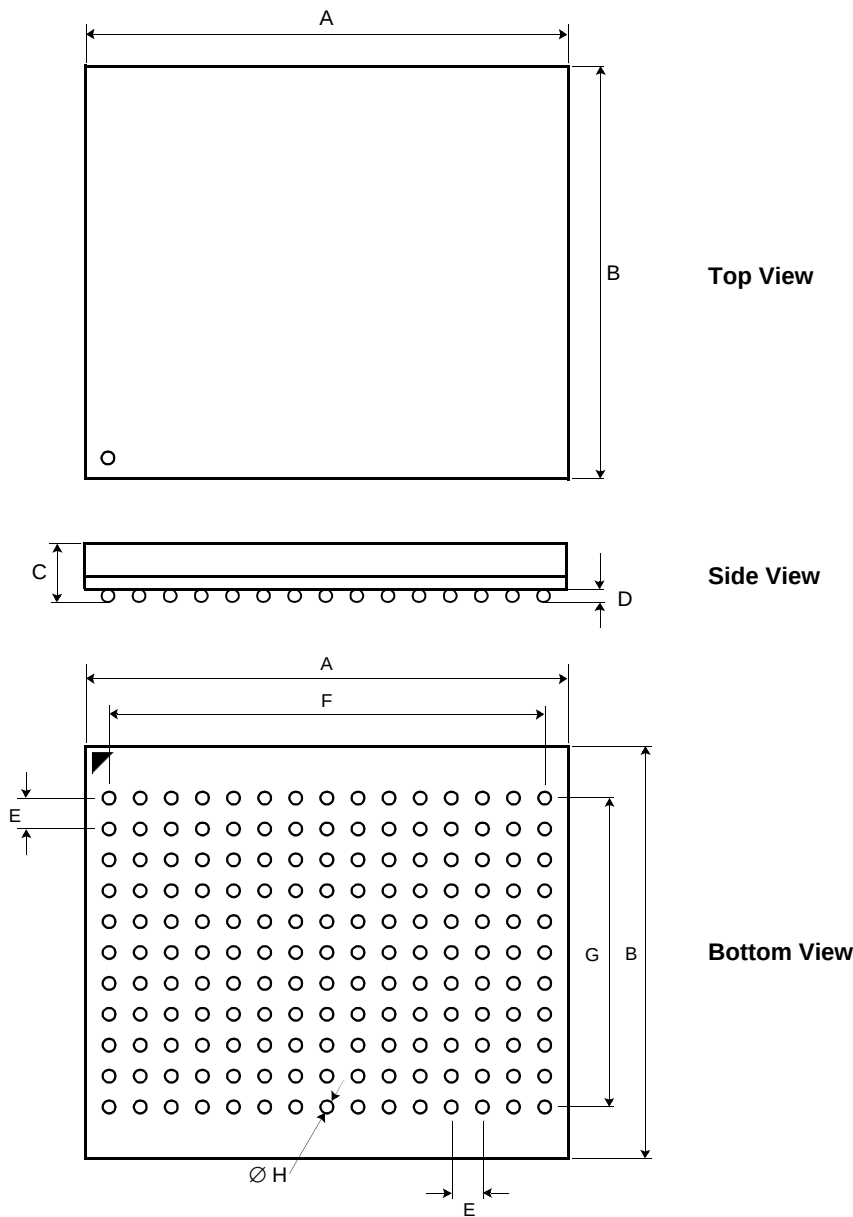


119BGA PACKAGE DIMENSIONS



165 FBGA PACKAGE DIMENSIONS

15mm x 17mm Body, 1.0mm Bump Pitch, 11x15 Ball Array



Symbol	Value	Units	Note	Symbol	Value	Units	Note
A	17 ± 0.1	mm		E	1.0	mm	
B	15 ± 0.1	mm		F	14.0	mm	
C	1.3 ± 0.1	mm		G	10.0	mm	
D	0.35 ± 0.05	mm		H	0.45 ± 0.05	mm	