



# SANYO Semiconductors

## DATA SHEET

# LC88F52H0A — CMOS LSI

FROM 512K byte, RAM 24K byte on-chip

## 16-bit 1-chip Microcontroller

### Overview

The SANYO LC88F52H0A is a 16-bit microcomputer that, centered around an Xstromy16 CPU, integrates on a single chip a number of hardware features such as 512K-byte flash ROM (onboard programmable), 24K-byte RAM, eight 16-bit timers, a base timer serving as a time-of-day clock, a real time clock, two synchronous SIO interfaces with automatic transmission capability, two single master I<sup>2</sup>C/synchronous SIO interface, a slave I<sup>2</sup>C/synchronous SIO interface, four asynchronous SIO (UART) interfaces, a 16-channel 12-bit resolution AD converter, 8bit resolution DA converter, four multifrequency 12-bit PWM modules, a watchdog timer, a system clock frequency divider, a 59-source (32 modules) 14-vector interrupt feature, and on-chip debugger feature.

### Features

#### ■Xstromy16 CPU

- 4G-byte address space
- General-purpose registers: 16 bits × 16 registers

#### ■Flash ROM

- Capable of onboard programming with a wide range of voltage levels (3.0 to 5.5V).
- Block-erasable in 512 or 1K byte units.
- Data written in 2-byte units.
- 524288 × 8 bits

#### ■RAM

- 24576 × 8 bits

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**■ Minimum instruction cycle time (tCYC)**

- 83.3 ns (12MHz)       $V_{DD} = 4.5$  to  $5.5V$
- 107 ns (9.3MHz)       $V_{DD} = 3.0$  to  $5.5V$
- 500 ns (2MHz)       $V_{DD} = 2.5$  to  $5.5V$

**■ Ports**

- Normal withstand voltage I/O ports  
Ports whose I/O direction can be designated in 1 bit units : 86 (P0n P1n, P2n, P3n, P4n, P5n, P6n, P7n, PAn PB0 to PB6, PC2, PD0 to PD5)
- Oscillation/normal withstand voltage I/O ports : 4 (PC0, PC1, PC3, PC4)
- Reset pins : 1 (RESB)
- TEST pins : 1 (TEST)
- Power pins : 8 ( $V_{SS1}$  to 4,  $V_{DD1}$  to 4)

**■ Timers**

- Timer 0: 16-bit timer that supports PWM/toggle outputs
  - 1) 5-bit prescaler
  - 2) 8-bit PWM  $\times 2$ , 8-bit timer + 8-bit PWM mode selectable
  - 3) Clock source selectable from system clock, OSC0, OSC1, and internal RC oscillator
- Timer 1: 16-bit timer with capture registers
  - 1) 5-bit prescaler
  - 2) May be divided into 2 channels of 8-bit timer
  - 3) Clock source selectable from system clock, OSC0, OSC1, and internal RC oscillator
- Timer 2: 16-bit timer with capture registers
  - 1) 4-bit prescaler
  - 2) May be divided into 2 channels of 8-bit timer
  - 3) Clock source selectable from system clock, OSC0, OSC1, and external events
- Timer 3: 16-bit timer that supports PWM/toggle outputs
  - 1) 8-bit prescaler
  - 2) 8-bit timer  $\times 2$ ch or 8-bit timer + 8-bit PWM mode selectable
  - 3) Clock source selectable from system clock, OSC0, OSC1, and external events
- Timer 4: 16-bit timer that supports toggle outputs
  - 1) Clock source selectable from system clock and prescaler 0
- Timer 5: 16-bit timer that supports toggle outputs
  - 1) Clock source selectable from system clock and prescaler 0
- Timer 6: 16-bit timer that supports toggle outputs
  - 1) Clock source selectable from system clock and prescaler 1
- Timer 7: 16-bit timer that supports toggle outputs
  - 1) Clock source selectable from system clock and prescaler 1

\* Prescaler 0 and 1 are consisted of 4 bits and can choose their clock source from OSC0 or OSC1.
- Base timer
  - 1) Clock may be selected from OSC0 (32.768kHz crystal oscillator) and frequency-divided output of system clock.
  - 2) Interrupts can be generated in 7 timing schemes.

**■ Real time clock**

- 1) Calender with Jan. 1, 2000 to Dec.31, 2799 including automatic leap year calculation function.
- 2) Consisted of Independent second- minute-hour-day-month-year-century counters.
- 3) Programmable count-clock calibration function.

**■ Serial interfaces**

- SIO0: 8-bit synchronous SIO
  - 1) LSB first/MSB first mode selectable
  - 2) Supports data communication with a data length of 8 bits or less (1 to 8 bits specifiable)
  - 3) Built-in 8-bit baudrate generator (4 tCYC to 512 tCYC transfer clocks)
  - 4) Continuous/automatic data transmission (9- to 32768-bit units specifiable)
  - 5) Interval function (intervals specifiable in 0 to 64 tSCK units)
  - 6) Wakeup function
- SIO1: 8-bit synchronous SIO
  - 1) LSB first/MSB first mode selectable
  - 2) Supports data communication with a data length of 8 bits or less (1 to 8 bits specifiable)
  - 3) Built-in 8-bit baudrate generator (4 tCYC to 512 tCYC transfer clocks)
  - 4) Continuous/automatic data transmission (9- to 32768-bit units specifiable)
  - 5) Interval function (intervals specifiable in 0 to 64 tSCK units)
  - 6) Wakeup function
- SMIIC0: Single master I<sup>2</sup>C/8-bit synchronous SIO
  - Mode 0: Single-master mode communication
  - Mode 1: Synchronous 8-bit serial I/O (MSB first)
- SMIIC1: Single master I<sup>2</sup>C/8-bit synchronous SIO
  - Mode 0: Single-master mode communication
  - Mode 1: Synchronous 8-bit serial I/O (MSB first)
- SLIIC0: Slave I<sup>2</sup>C/8-bit synchronous SIO
  - Mode 0: I<sup>2</sup>C slave mode communication
  - Mode 1: Synchronous 8-bit serial I/O (MSB first)

Note: usable only with the external clock source
- UART0
  - 1) Data length : 8 bits (LSB first)
  - 2) Start bits : 1 bit
  - 3) Stop bits : 1 bit
  - 4) Parity bits : None/even parity/odd parity
  - 5) Transfer rate : 4/8 cycle
  - 6) Baudrate source clock: P07 input signal used as a 1 cycle signal (T0PWMH can be used as a clock source) or Timer 4 cycle.
  - 7) Full duplex communication

Note: The “cycle” refers to one period of the baudrate clock source.
- UART2
  - 1) Data length : 8 bits (LSB first)
  - 2) Start bits : 1 bit
  - 3) Stop bits : 1/2 bit
  - 4) Parity bits : None/even parity/odd parity
  - 5) Transfer rate : 8 to 4096 cycle
  - 6) Baudrate source clock : System clock/OSC0/OSC1/P26 input signal
  - 7) Wakeup function
  - 8) Full duplex communication

Note: The “cycle” refers to one period of the baudrate clock source.
- UART3
  - 1) Data length : 8 bits (LSB first)
  - 2) Start bits : 1 bit
  - 3) Stop bits : 1/2 bit
  - 4) Parity bits : None/even parity/odd parity
  - 5) Transfer rate : 8 to 4096 cycle
  - 6) Baudrate source clock: System clock/OSC0/OSC1/P36 input signal
  - 7) Wakeup function
  - 8) Full duplex communication

Note: The “cycle” refers to one period of the baudrate clock source.

- **UART4**

- 1) Data length : 8 bits (LSB first)
- 2) Start bits : 1 bit
- 3) Stop bits : 1/2 bit
- 4) Parity bits : None/even parity/odd parity
- 5) Transfer rate : 8 to 4096 cycle
- 6) Baudrate source clock: System clock/OSC0/OSC1/P37 input signal
- 7) Wakeup function
- 8) Full duplex communication

Note: The “cycle” refers to one period of the baudrate clock source.

- **AD converter**

- 1) 12/8 bits resolution selectable
- 2) Analog input: 16 channels
- 3) Comparator mode
- 4) Automatic reference voltage generation

- **DA converter**

- 1) 8 bits resolution
- 2) 2 converters built-in
- 3) Able to choose output pins

- **PWM**

- **PWM0: Multifrequency 12-bit PWM × 2 channels (PWM00 and PWM01)**
  - 1) 2-channel pairs controlled independently of one another
  - 2) Clock source selectable from system clock or OSC1
  - 3) 8-bit prescaler:  $TPWMR0 = (\text{prescaler value} + 1) \times \text{clock period}$
  - 4) 8-bit fundamental wave PWM generator circuit + 4-bit additional pulse generator circuit
  - 5) Fundamental wave PWM mode
    - Fundamental wave period: 16 TPWMR0 to 256 TPWMR0
    - High pulse width : 0 to (Fundamental wave period - TPWMR0)
  - 6) Fundamental wave + additional pulse mode
    - Fundamental wave period: 16 TPWMR0 to 256 TPWMR0
    - Overall period : Fundamental wave period × 16
    - High pulse width : 0 to (Fundamental wave period - TPWMR0)
- **PWM1: Multifrequency 12-bit PWM × 2 channels (PWM10 and PWM11)**
  - 1) 2-channel pairs controlled independently of one another
  - 2) Clock source selectable from system clock or OSC1
  - 3) 8-bit prescaler:  $TPWMR1 = (\text{prescaler value} + 1) \times \text{clock period}$
  - 4) 8-bit fundamental wave PWM generator circuit + 4-bit additional pulse generator circuit
  - 5) Fundamental wave PWM mode
    - Fundamental wave period: 16 TPWMR1 to 256 TPWMR1
    - High pulse width : 0 to (Fundamental wave period - TPWMR1)
  - 6) Fundamental wave + additional pulse mode
    - Fundamental wave period: 16 TPWMR1 to 256 TPWMR1
    - Overall period : Fundamental wave period × 16
    - High pulse width : 0 to (Fundamental wave period - TPWMR1)

- **Watchdog timer**

- 1) Driven by the base timer + internal watchdog timer dedicated counter
- 2) Interrupt or reset mode selectable

**■Interrupts (peripheral function)**

- 59 sources (32 modules), 14 vector addresses

- 1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
- 2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

| No. | Vector Address | Interrupt Source                           |
|-----|----------------|--------------------------------------------|
| 1   | 08000H         | Watchdog timer (1)                         |
| 2   | 08004H         | Base timer (2)                             |
| 3   | 08008H         | Timer 0 (2)                                |
| 4   | 0800CH         | INT0 (1)                                   |
| 5   | 08014H         | INT1 (1)                                   |
| 6   | 08018H         | INT2 (1)/timer 1 (2)/UART2 (4)             |
| 7   | 0801CH         | INT3 (1)/timer 2 (4)/SMIIC0 (1)/SLIIC1 (1) |
| 8   | 08020H         | INT4 (1)/timer 3 (2)                       |
| 9   | 08024H         | INT5 (1)/timer 4 (1)/SIO1 (2)              |
| 10  | 0802CH         | PWM0 (1)/SMIIC1(1)                         |
| 11  | 08030H         | ADC (1)/timer 5 (1)                        |
| 12  | 08034H         | INT6 (1)/timer 6 (1)/UART 3 (4)            |
| 13  | 08038H         | INT7 (1)/SIO0 (2)/SIO0(2)/USRT4 (4)        |
| 14  | 0803CH         | Port 0 (3)/Port 5 (8)/RTC (1)              |

- 3 priority levels selectable.
- Of interrupts of the same level, the one with the smallest vector address takes precedence.
- A number enclosed in parentheses denotes the number of sources.

**■Subroutine Stack: 24K-byte RAM area**

- Subroutine calls that automatically save PSW, interrupt vector calls: 6 bytes
- Subroutine calls that do not automatically save PSW: 4 bytes

**■Multiplication/division instructions**

- 16 bits × 16 bits (18 tCYC execution time)
- 16 bits ÷ 16 bits (18 to 19 tCYC execution time)
- 32 bits ÷ 16 bits (18 to 19 tCYC execution time)

**■Oscillator circuits**

- RC oscillator circuit (internal): For system clock
- CF oscillator circuit (built-in Rf circuit): For system clock (OSC1)
- VCO oscillator circuit: For system clock (OSC1)
- Crystal oscillator circuit (built-in Rf circuit): For low-speed system clock (OSC0)
- SLRC oscillator circuit (internal): For system clock (In the case of exception processing)

**■System clock divider function**

- Can run on low current.
- 1/1 to 1/128 of the system clock frequency can be set.

**■Standby Function**

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  - 1) Oscillation is not halted automatically.
  - 2) Released by a system reset or occurrence of an interrupt.
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  - 1) OSC1, RC and OSC0 oscillators automatically stop.
  - 2) There are the six ways of releasing the HOLD mode.
    - (1) Setting the reset pin to the low level
    - (2) Setting at least one of the INT0, INT1, INT2, INT4, INT5, INT6, and INT7 pins to the specified level
    - (3) Having an interrupt source established at port 0
    - (4) Having an interrupt source established at port 5
    - (5) Having an interrupt established at SIO0 or SIO1
    - (6) Having an interrupt established at UART2, UART3 or UART4
- HOLDX mode: Suspends instruction execution and the operation of the peripheral circuits except those which run on OSC0.
  - 1) OSC1 and RC oscillations automatically stop.
  - 2) OSC0 maintains the state that is established when the HOLDX mode is entered.
  - 3) There are seven ways of releasing the HOLDX mode.
    - (1) Setting the reset pin to the low level
    - (2) Setting at least one of the INT0, INT1, INT2, INT4, INT5, INT6, and INT7 pins to the specified level
    - (3) Having an interrupt source established at port 0
    - (4) Having an interrupt source established at port 5
    - (5) Having an interrupt source established at the base timer circuit
    - (6) Having an interrupt established at SIO0 or SIO1
    - (7) Having an interrupt established at UART2, UART3 or UATR4

**■On-chip debugger function**

- Supports software debugging with the IC mounted on the target board.
- Supports source line debugging and tracing functions, and breakpoint setting and real time display.
- Single-wire communication

**■Package Form**

- TQFP100(14×14): Lead-free and halogen-free type

**■Development Tools**

- On-chip debugger: EOCUIF1 + LC88F52H0A

**■Programming board**

| Package           | Programming Board |
|-------------------|-------------------|
| TQFP100 (14 × 14) | W88F52TQ          |

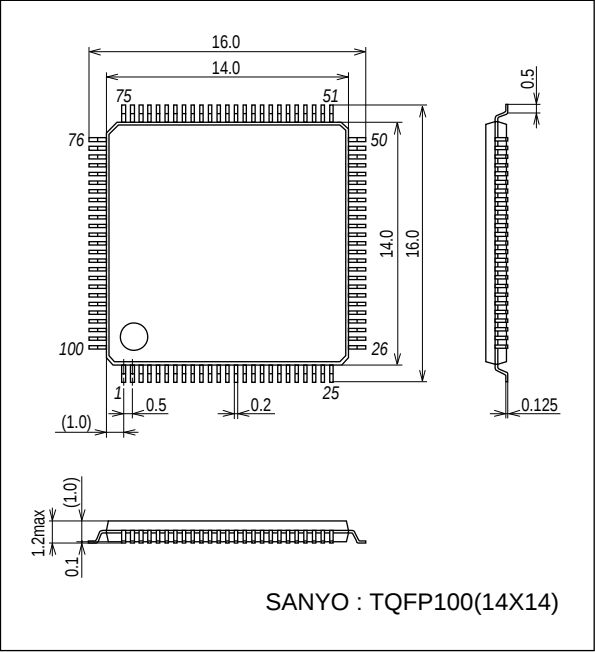
**■Flash Programming**

| Manufacturer                 | Model Name        | Supported Version                                              | Device     |
|------------------------------|-------------------|----------------------------------------------------------------|------------|
| Flash Support Group (single) | AF9708/09/09B/09C | Revision: After Rev.03.32D                                     | 88F512SN   |
| Flash Support Group (Gang)   | AF9723/23B        |                                                                |            |
|                              | AF9833            |                                                                |            |
| SANYO                        | SKK/SKK Type-B    | Application Version After 1.06<br>Chip Data Version After 2.22 | LC88F52H0A |

Package Dimensions

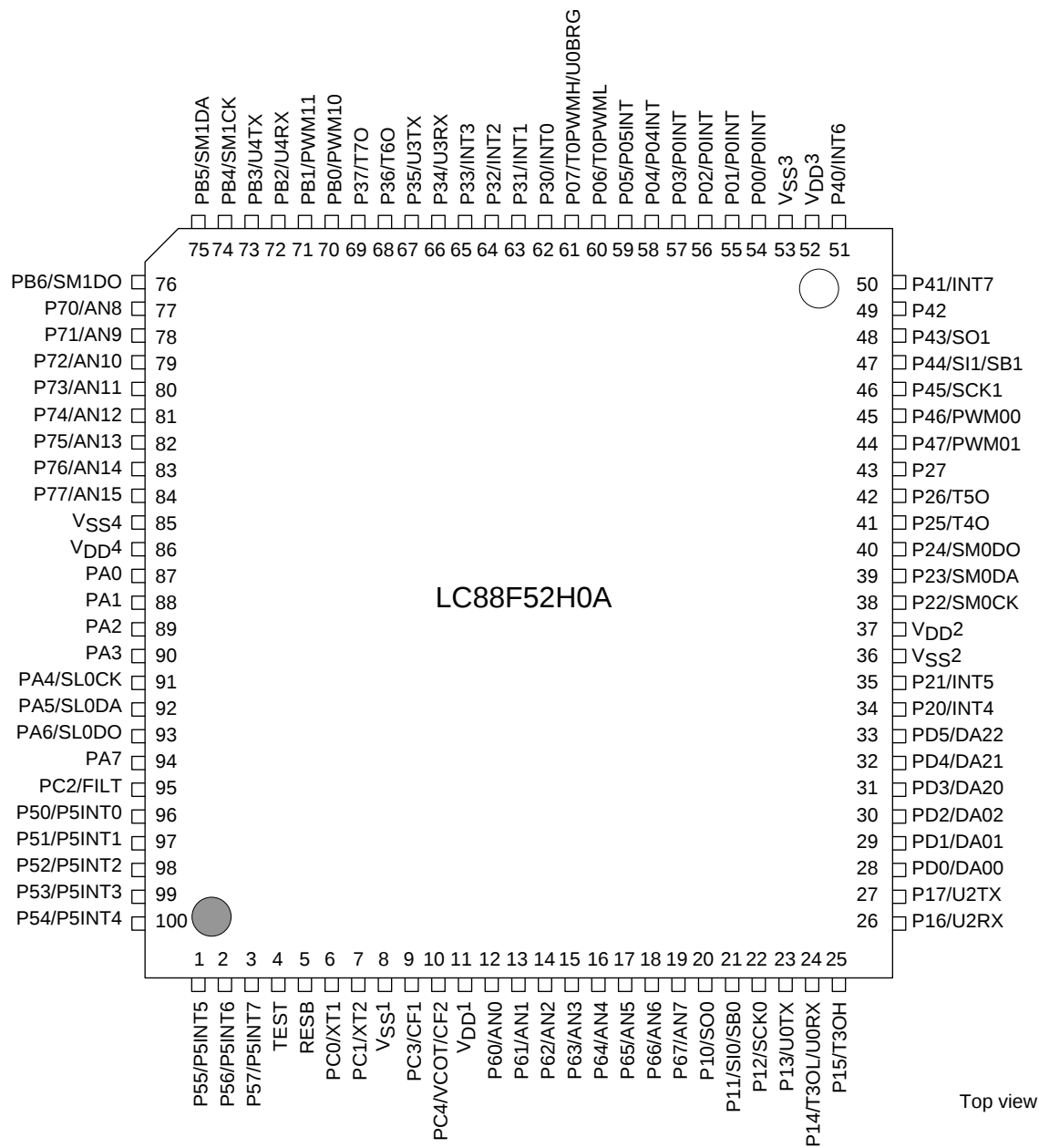
unit : mm (typ)

3274



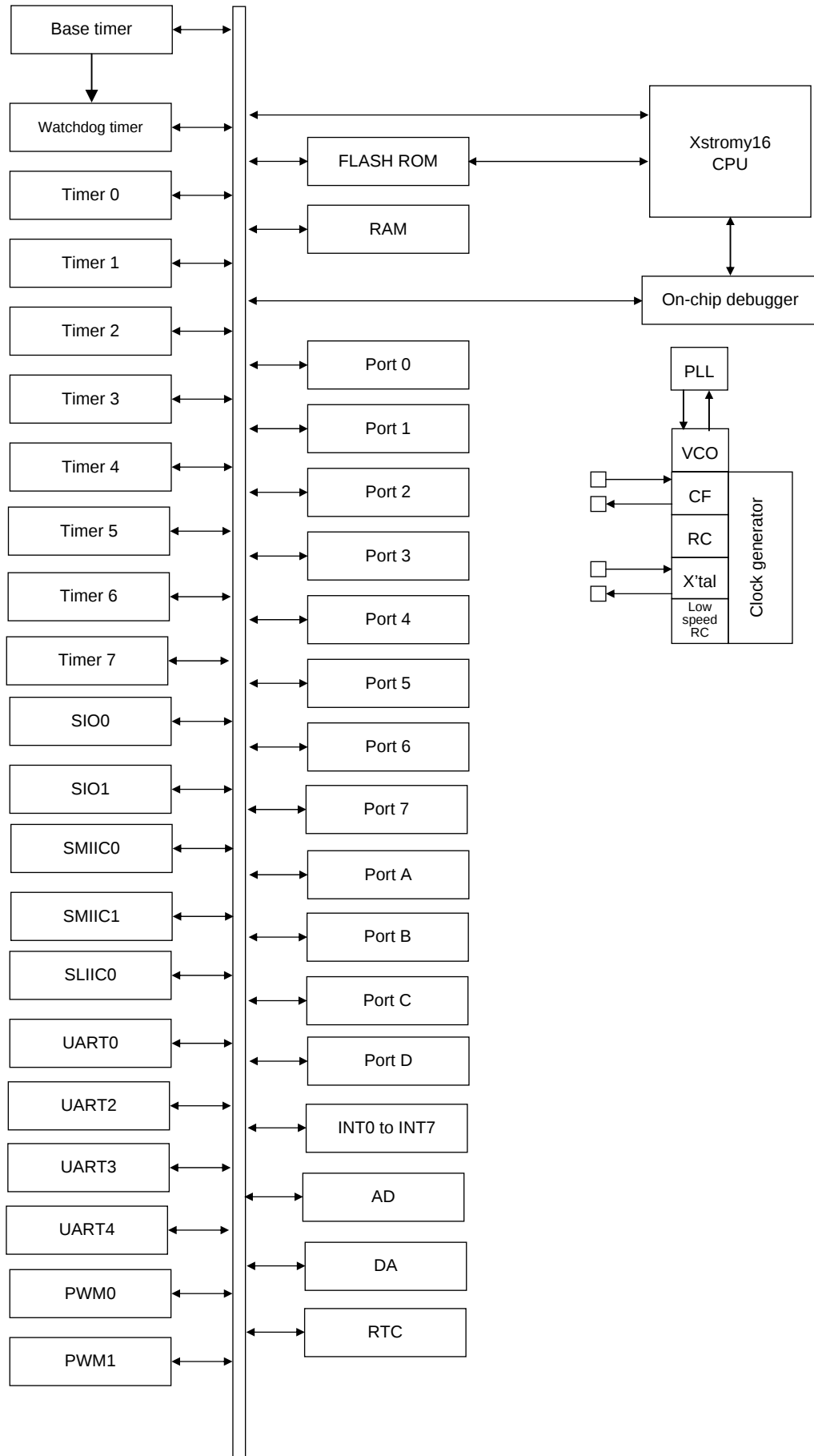
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Pin Assignment



SANYO: TQFP100 (14×14) (Lead-free and halogen-free type)

# System Block Diagram



## Pin Description

| Pin Name                                                                      | I/O | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------------------------------------------------------------------------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| V <sub>SS</sub> 1, V <sub>SS</sub> 2,<br>V <sub>SS</sub> 3, V <sub>SS</sub> 4 | -   | - Power sources                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| V <sub>DD</sub> 1, V <sub>DD</sub> 2,<br>V <sub>DD</sub> 3, V <sub>DD</sub> 4 | -   | + Power sources                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| Port 0<br>P00 to P07                                                          | I/O | <ul style="list-style-type: none"> <li>• 8-bit I/O port</li> <li>• I/O specifiable in 1-bit units</li> <li>• Pull-up resistors can be turned on and off in 1 bit units</li> <li>• HOLD release input (P00 to P03, P04, P05)</li> <li>• Port 0 interrupt input (P00 to P03, P04, P05)</li> <li>• Pin functions <ul style="list-style-type: none"> <li>P06: Timer 0L output</li> <li>P07: Timer 0L output/UART0 clock input</li> </ul> </li> </ul>                                                                                                                                                                                                                                                                                                                                                  |
| Port 1<br>P10 to P17                                                          | I/O | <ul style="list-style-type: none"> <li>• 8-bit I/O port</li> <li>• I/O specifiable in 1-bit units</li> <li>• Pull-up resistors can be turned on and off in 1 bit units</li> <li>• Pin functions <ul style="list-style-type: none"> <li>P10: SIO0 data output</li> <li>P11: SIO0 data input/pulse input/output</li> <li>P12: SIO0 clock input/output</li> <li>P13: UART0 transmit</li> <li>P14: Timer 3L output/UART0 receive</li> <li>P15: Timer 3H output</li> <li>P16: UART2 receive</li> <li>P17: UART2 transmit</li> </ul> </li> </ul>                                                                                                                                                                                                                                                        |
| Port 2<br>P20 to P27                                                          | I/O | <ul style="list-style-type: none"> <li>• 8-bit I/O port</li> <li>• I/O specifiable in 1-bit units</li> <li>• Pull-up resistors can be turned on and off in 1 bit units</li> <li>• Pin functions <ul style="list-style-type: none"> <li>P20: INT4 input/HOLD release input/timer 3 event input/timer 2L capture input/timer 2H capture input</li> <li>P21: INT5 input/HOLD release input/timer 3 event input/timer 2L capture input/timer 2H capture input</li> <li>P22: SMIC0 clock input/output</li> <li>P23: SMIC0 bus input/output/data input</li> <li>P24: SMIC0 data output (used in 3-wire SIO mode)</li> <li>P25: Timer 4 output</li> <li>P26: Timer 5 output</li> <li>Interrupt acknowledge type</li> <li>INT4, INT5: H level, L level, H edge, L edge, both edges</li> </ul> </li> </ul> |
| Port 3<br>P30 to P37                                                          | I/O | <ul style="list-style-type: none"> <li>• 8-bit I/O port</li> <li>• I/O specifiable in 1-bit units</li> <li>• Pull-up resistors can be turned on and off in 1 bit units</li> <li>• Pin functions <ul style="list-style-type: none"> <li>P30: INT0 input/HOLD release/timer 2L capture input</li> <li>P31: INT1 input/HOLD release/timer 2H capture input</li> <li>P32: INT2 input/HOLD release/timer 2 event input/timer 2L capture input</li> <li>P33: INT3 input/HOLD release/timer 2 event input/timer 2H capture input</li> <li>P34: UART3 receive</li> <li>P35: UART3 transmit</li> <li>P36: Timer 6 output</li> <li>P37: Timer 7 output</li> <li>Interrupt acknowledge type</li> <li>INT0 to INT3: H level, L level, H edge, L edge, both edges</li> </ul> </li> </ul>                       |

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| Pin Name   | I/O | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|------------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Port 4     | I/O | <ul style="list-style-type: none"> <li>• 8-bit I/O port</li> <li>• I/O specifiable in 1-bit units</li> <li>• Pull-up resistors can be turned on and off in 1 bit units</li> <li>• Pin functions</li> </ul> P40: INT6 input/HOLD release input<br>P41: INT7 input/HOLD release input<br>P43: SIO1 data output<br>P44: SIO1 data input/bus input/output<br>P45: SIO1 clock input/output<br>P46: PWM00 output<br>P47: PWM01 output<br>Interrupt acknowledge type<br>INT6, INT7: H level, L level, H edge, L edge, both edges |
| P40 to P47 |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| Port 6     | I/O | <ul style="list-style-type: none"> <li>• 8-bit I/O port</li> <li>• I/O specifiable in 1-bit units</li> <li>• Pull-up resistors can be turned on and off in 1 bit units</li> <li>• Pin functions</li> </ul> AN0 (P60) to AN7 (P67): AD converter input port                                                                                                                                                                                                                                                                |
| P60 to P67 |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| Port 7     | I/O | <ul style="list-style-type: none"> <li>• 8-bit I/O port</li> <li>• I/O specifiable in 1-bit units</li> <li>• Pull-up resistors can be turned on and off in 1 bit units</li> <li>• Pin functions</li> </ul> AN8 (P70) to AN15 (P77): AD converter input port                                                                                                                                                                                                                                                               |
| P70 to P77 |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| Port A     | I/O | <ul style="list-style-type: none"> <li>• 8-bit I/O port</li> <li>• I/O specifiable in 1-bit units</li> <li>• Pull-up resistors can be turned on and off in 1 bit units</li> <li>• Multiplexed pin functions</li> </ul> PA4: SLIIC0 clock input<br>PA5: SLIIC0 bus input/output/data input<br>PA6: SLIIC0 data output (used in 3-wire SIO mode)                                                                                                                                                                            |
| PA0 to PA7 |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| Port B     | I/O | <ul style="list-style-type: none"> <li>• 7-bit I/O port</li> <li>• I/O specifiable in 1-bit units</li> <li>• Pull-up resistors can be turned on and off in 1 bit units</li> <li>• Multiplexed pin functions</li> </ul> PB0: PWM10 output<br>PB1: PWM11 output<br>PB2: UART4 receive<br>PB3: UART4 transmit<br>PB4: SMIIC1 clock input/output<br>PB5: SMIIC1 bus input/output/data input<br>PB6: SMIIC1 data output (used in 3-wire SIO mode)                                                                              |
| PB0 to PB6 |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| Port C     | I/O | <ul style="list-style-type: none"> <li>• 5-bit I/O port</li> <li>• I/O specifiable in 1-bit units</li> <li>• Pull-up resistors can be turned on and off in 1 bit units (PC2)</li> <li>• Pin functions</li> </ul> PC0: 32.768 kHz crystal oscillator input<br>PC1: 32.768 kHz crystal oscillator output<br>PC2: FILT<br>PC3: Ceramic oscillator input<br>PC4: Ceramic oscillator output/VCO output                                                                                                                         |
| PC0 to PC4 |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| Port D     | I/O | <ul style="list-style-type: none"> <li>• 6-bit I/O port</li> <li>• I/O specifiable in 1-bit units</li> <li>• Pull-up resistors can be turned on and off in 1 bit units</li> <li>• Multiplexed pin functions</li> </ul> PD0: DA00 output<br>PD1: DA01 output<br>PD2: DA02 output<br>PD3: DA10 output<br>PD4: DA11 output<br>PD5: DA12 output                                                                                                                                                                               |
| PD0 to PD5 |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| TEST       | I/O | <ul style="list-style-type: none"> <li>• TEST pin</li> <li>• Used to communicate with on-chip debugger.</li> <li>• Connects an external 100kΩ pull-down resistor.</li> </ul>                                                                                                                                                                                                                                                                                                                                              |
| RESB       | I   | Reset pin                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

## Port Output Types

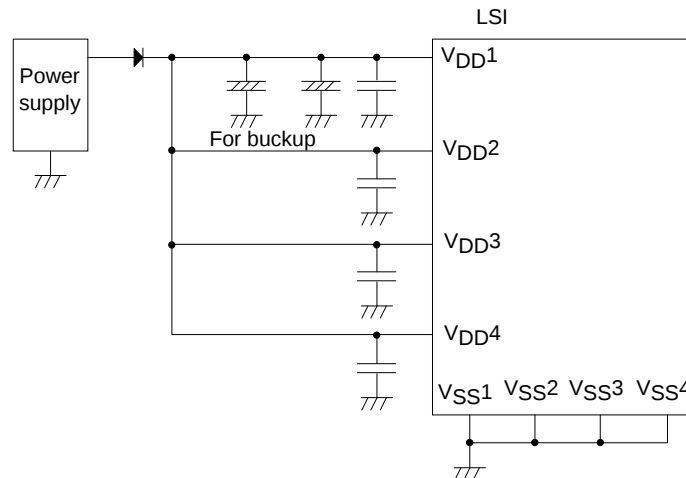
The table below lists the types of port outputs and the presence/absence of a pull-up resistor.

Data can be read into any input port even if it is in the output mode.

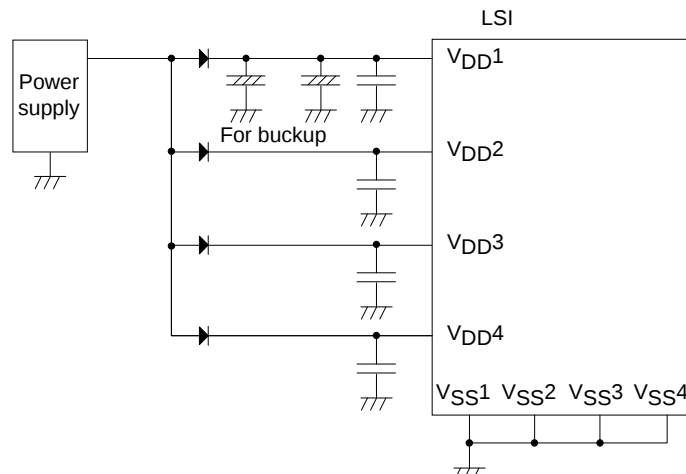
| Port Name                                                                                                                  | Option Selected in Units of | Output Type                                                                             | Pull-up Resistor |
|----------------------------------------------------------------------------------------------------------------------------|-----------------------------|-----------------------------------------------------------------------------------------|------------------|
| P00 to P07                                                                                                                 | 1 bit                       | CMOS                                                                                    | Programmable     |
| P10 to P17<br>P20 to P27<br>P30 to P37<br>P40 to P47<br>P50 to P57<br>P60 to P67<br>P70 to P77<br>PA0 to PA7<br>PB0 to PB6 |                             | Able to program special functions' output type from CMOS output or N-channel open drain |                  |
| P60 to P67<br>P70 to p77<br>PD0 to PD5<br>PC2                                                                              |                             | CMOS                                                                                    |                  |
| PC0                                                                                                                        | -                           | N-channel open drain (32.768kHz crystal oscillator input)                               | None             |
| PC1                                                                                                                        | -                           | N-channel open drain (32.768kHz crystal oscillator output)                              | None             |
| PC3                                                                                                                        | -                           | CMOS (ceramic oscillator input)                                                         | None             |
| PC4                                                                                                                        | -                           | CMOS (ceramic oscillator output)                                                        | None             |

\* Make the following connection to minimize the noise input to the V<sub>DD1</sub> pin and prolong the backup time.  
Be sure to electrically short the V<sub>SS1</sub>, V<sub>SS2</sub>, V<sub>SS3</sub> and V<sub>SS4</sub> pins.

Example 1: When data is being backed up in the HOLD mode, the H level signals to the output ports are fed by the backup capacitors.



Example 2: When data is being backed up in the HOLD mode, the H level output at any ports is not sustained and is unpredictable.



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## Absolute Maximum Ratings at Ta = 25°C, VSS1 = VSS2 = VSS3 = VSS4 = 0V

| Parameter                 | Symbol                            | Applicable Pin /Remarks                                          | Conditions                                                                  | VDD[V]                                     | Specification |     |          |      |
|---------------------------|-----------------------------------|------------------------------------------------------------------|-----------------------------------------------------------------------------|--------------------------------------------|---------------|-----|----------|------|
|                           |                                   |                                                                  |                                                                             |                                            | min           | typ | max      | unit |
| Maximum supply voltage    | VDD max                           | VDD1, VDD2, VDD3, VDD4                                           | VDD1=VDD2=VDD3=VDD4                                                         |                                            | -0.3          |     | +6.5     | V    |
| Input voltage             | VI(1)                             | RESB                                                             |                                                                             |                                            | -0.3          |     | VDD +0.3 |      |
| Input/output voltage      | VI/O(1)                           | Ports 0, 1, 2<br>Ports 3, 4, 5<br>Ports 6, 7<br>Ports A, B, C, D |                                                                             |                                            | -0.3          |     | VDD +0.3 |      |
| High level output current | Peak output current               | IOPH(1)                                                          | Ports 0, 1, 2, 3<br>P40 to P45<br>Ports 7, A, D<br>PB2 to PB6               | CMOS output selected<br>Per applicable pin | -10           |     |          |      |
|                           |                                   | IOPH(2)                                                          | P46, P47<br>PB0, PB1                                                        | Per applicable pin                         | -20           |     |          |      |
|                           |                                   | IOPH(3)                                                          | Port 5, 6<br>PC0 to PC4                                                     | Per applicable pin                         | -5            |     |          |      |
|                           | Average output current (Note 1-1) | IOMH(1)                                                          | Ports 0, 1, 2, 3<br>P40 to P45<br>Ports 5, 6, 7, A<br>PB2 to PB6<br>Ports D | CMOS output selected<br>Per applicable pin | -7.5          |     |          |      |
|                           |                                   | IOMH(2)                                                          | P46, P47<br>PB0, PB1                                                        | Per applicable pin                         | -10           |     |          |      |
|                           |                                   | IOMH(3)                                                          | Port 5, 6<br>PC0 to PC4                                                     | Per applicable pin                         | -3            |     |          |      |
|                           | Total output current              | ΣIOAH(1)                                                         | Pprts 5<br>PC0 to PC4                                                       | Total of currents at applicable pins       | -15           |     |          | mA   |
|                           |                                   | ΣIOAH(2)                                                         | Port 6                                                                      | Total of currents at applicable pins       | -15           |     |          |      |
|                           |                                   | ΣIOAH(3)                                                         | Port 5, 6<br>PC0 to PC4                                                     | Total of currents at applicable pins       | -20           |     |          |      |
|                           |                                   | ΣIOAH(4)                                                         | Ports 1,D1<br>P20 to P21                                                    | Total of currents at applicable pins       | -25           |     |          |      |
|                           |                                   | ΣIOAH(5)                                                         | P22 to P27                                                                  | Total of currents at applicable pins       | -25           |     |          |      |
|                           |                                   | ΣIOAH(6)                                                         | Ports 1, 2, D                                                               | Total of currents at applicable pins       | -45           |     |          |      |
|                           |                                   | ΣIOAH(7)                                                         | Ports 4                                                                     | Total of currents at applicable pins       | -25           |     |          |      |
|                           |                                   | ΣIOAH(8)                                                         | Ports 0, 3                                                                  | Total of currents at applicable pins       | -25           |     |          |      |
|                           |                                   | ΣIOAH(9)                                                         | Ports 0, 3, 4                                                               | Total of currents at applicable pins       | -45           |     |          |      |
|                           |                                   | ΣIOAH(10)                                                        | Ports B, 7                                                                  | Total of currents at applicable pins       | -25           |     |          |      |
|                           |                                   | ΣIOAH(11)                                                        | Ports A                                                                     | Total of currents at applicable pins       | -25           |     |          |      |
|                           |                                   | ΣIOAH(12)                                                        | Ports 7, A, B                                                               | Total of currents at applicable pins       | -45           |     |          |      |

Note 1-1: Average output current refers to the average of output currents measured for a period of 100ms.

Continued on next page.

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Continued from preceding page.

| Parameter                     | Symbol                            | Applicable Pin /Remarks | Conditions                                                                                                | V <sub>DD</sub> [V]                  | Specification |     |      |      |
|-------------------------------|-----------------------------------|-------------------------|-----------------------------------------------------------------------------------------------------------|--------------------------------------|---------------|-----|------|------|
|                               |                                   |                         |                                                                                                           |                                      | min           | typ | max  | unit |
| Low level output current      | Peak output current               | IOPL(1)                 | Ports 0, 1, 3, 4<br>Ports 7, A, B<br>P20, P21, P24 to P27<br>PA0 to PA4, PA6, PA7<br>PB0 to PB4, PB6, PB7 | Per applicable pin                   |               |     | 20   | mA   |
|                               |                                   | IOPL(2)                 | P22, P23<br>PA4, PA5<br>PB4, PB5                                                                          | Per applicable pin                   |               |     | 25   |      |
|                               |                                   | IOPL(3)                 | Ports 5, 6<br>PC0 to PC4                                                                                  | Per applicable pin                   |               |     | 10   |      |
|                               | Average output current (Note 1-1) | IOML(1)                 | Ports 0, 1, 3, 4<br>Ports 7, A, B<br>P20, P21, P24 to P27<br>PA0 to PA4, PA6, PA7<br>PB0 to PB4, PB6, PB7 | Per applicable pin                   |               |     | 15   |      |
|                               |                                   | IOML(2)                 | P22, P23<br>PA4, PA5<br>PB4, PB5                                                                          | Per applicable pin                   |               |     | 20   |      |
|                               |                                   | IOML(3)                 | Ports 5, 6<br>PC0 to PC4                                                                                  | Per applicable pin                   |               |     | 7.5  |      |
|                               | Total output current              | ΣIOAL(1)                | Ports 5<br>PC0 to PC2                                                                                     | Total of currents at applicable pins |               |     | 15   |      |
|                               |                                   | ΣIOAL(2)                | Port 6<br>PC3 to PC4                                                                                      | Total of currents at applicable pins |               |     | 15   |      |
|                               |                                   | ΣIOAL(3)                | Port 5, 6<br>PC0 to PC4                                                                                   | Total of currents at applicable pins |               |     | 20   |      |
|                               |                                   | ΣIOAL(4)                | Ports 1, D<br>P20, P21                                                                                    | Total of currents at applicable pins |               |     | 45   |      |
|                               |                                   | ΣIOAL(5)                | P22 to P27                                                                                                | Total of currents at applicable pins |               |     | 45   |      |
|                               |                                   | ΣIOAL(6)                | Ports 1, 2, D                                                                                             | Total of currents at applicable pins |               |     | 80   |      |
|                               |                                   | ΣIOAL(7)                | Port 4                                                                                                    | Total of currents at applicable pins |               |     | 45   |      |
|                               |                                   | ΣIOAL(8)                | Port 0, 3                                                                                                 | Total of currents at applicable pins |               |     | 45   |      |
|                               |                                   | ΣIOAL(9)                | Port 0, 3, 4                                                                                              | Total of currents at applicable pins |               |     | 80   |      |
|                               |                                   | ΣIOAL(10)               | Port 7, B                                                                                                 | Total of currents at applicable pins |               |     | 45   |      |
|                               |                                   | ΣIOAL(11)               | Port A                                                                                                    | Total of currents at applicable pins |               |     | 45   |      |
|                               |                                   | ΣIOAL(12)               | Port 7, A, B                                                                                              | Total of currents at applicable pins |               |     | 80   |      |
| Allowable power dissipation   | Pd max                            | TQFP100(14×14)          | Ta=-40 to +85°C                                                                                           |                                      |               |     | 250  | mW   |
| Operating ambient temperature | Topr                              |                         |                                                                                                           |                                      | -40           |     | +85  | °C   |
| Storage ambient temperature   | Tstg                              |                         |                                                                                                           |                                      | -55           |     | +125 |      |

Note 1-1: Average output current refers to the average of output currents measured for a period of 100ms.

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## Allowable Operating Conditions at Ta = -40°C to +85°C, VSS1 = VSS2 = VSS3 = VSS4 = 0V

| Parameter                              | Symbol   | Applicable Pin/Remarks                                 | Conditions                                                                                                        | Specification |                |     |                 |      |
|----------------------------------------|----------|--------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|---------------|----------------|-----|-----------------|------|
|                                        |          |                                                        |                                                                                                                   | VDD[V]        | min            | typ | max             | unit |
| Operating supply voltage<br>(Note 2-1) | VDD(1)   | VDD1=VDD2=VDD3                                         | 0.081μs≤tCYC≤66μs                                                                                                 |               | 4.0            |     | 5.5             | V    |
|                                        |          |                                                        | 0.103μs≤tCYC≤66μs                                                                                                 |               | 3.0            |     | 5.5             |      |
|                                        |          |                                                        | 0.490μs≤tCYC≤66μs                                                                                                 |               | 2.5            |     | 5.5             |      |
| Memory sustaining supply voltage       | VHD      | VDD1=VDD2=VDD3                                         | RAM and register contents sustained in HOLD mode                                                                  |               | 2.0            |     | 5.5             |      |
| High level input voltage               | VIH(1)   | Ports 0, 1, 2, 3, 4<br>Port 5, A, B                    |                                                                                                                   | 2.5 to 5.5    | 0.3VDD<br>+0.7 |     | VDD             |      |
|                                        | VIH(2)   | Ports 6, 7, PC2                                        |                                                                                                                   | 2.5 to 5.5    | 0.3VDD<br>+0.7 |     | VDD             |      |
|                                        | VIH(3)   | RESB<br>PC0, PC1, PC3, PC4                             |                                                                                                                   | 2.5 to 5.5    | 0.75VDD        |     | VDD             |      |
|                                        | VIH(4)   | P22, P23, PA4, PA5,<br>PB4, PB5 I <sup>2</sup> C side  |                                                                                                                   | 2.5 to 5.5    | 0.7VDD         |     | VDD             |      |
| Low level input voltage                | VIL(1)   | When ports 1, 2, 3, 4,<br>5, A and port B,<br>PnFSAn=0 |                                                                                                                   | 4.0 to 5.5    | VSS            |     | 0.1VDD<br>+0.4  |      |
|                                        | VIL(2)   | Ports 0, 6, 7, PC2                                     |                                                                                                                   | 2.5 to 4.0    | VSS            |     | 0.2VDD          |      |
|                                        | VIL(3)   | When ports 1, 2, 3, 4,<br>5, A and port B,<br>PnFSAn=1 |                                                                                                                   | 4.0 to 5.5    | VSS            |     | 0.15VDD<br>+0.4 |      |
|                                        | VIL(4)   |                                                        |                                                                                                                   | 2.5 to 4.0    | VSS            |     | 0.2VDD          |      |
|                                        | VIL(5)   | CF1, RESB<br>PC0, PC1, PC3, PC4                        |                                                                                                                   | 2.5 to 5.5    | VSS            |     | 0.25VDD         |      |
|                                        | VIL(6)   | P22, P23, PA4, PA5,<br>PB4, PB5 I <sup>2</sup> C side  |                                                                                                                   | 2.5 to 5.5    | VSS            |     | 0.3VDD          |      |
| Instruction cycle time<br>(Note 2-2)   | tCYC     |                                                        |                                                                                                                   | 4.5 to 5.5    | 0.081          |     | 66              | μs   |
|                                        |          |                                                        |                                                                                                                   | 2.8 to 5.5    | 0.122          |     | 66              |      |
|                                        |          |                                                        |                                                                                                                   | 2.5 to 5.5    | 0.490          |     | 66              |      |
| External system clock frequency        | FEXCF(1) | CF1                                                    | <ul style="list-style-type: none"> <li>CF2 pin open</li> <li>System clock frequency division ratio=1/1</li> </ul> | 4.5 to 5.5    | 0.1            |     | 12              | MHz  |
|                                        |          |                                                        |                                                                                                                   | 3.0 to 5.5    | 0.1            |     | 8.3             |      |
|                                        |          |                                                        | <ul style="list-style-type: none"> <li>External system clock DUTY50±5%</li> </ul>                                 | 2.5 to 5.5    | 0.1            |     | 2               |      |
|                                        |          |                                                        |                                                                                                                   | 4.5 to 5.5    | 0.2            |     | 24              |      |
|                                        |          |                                                        | <ul style="list-style-type: none"> <li>CF2 pin open</li> <li>System clock frequency division ratio=1/2</li> </ul> | 3.0 to 5.5    | 0.2            |     | 18.6            |      |
|                                        |          |                                                        |                                                                                                                   | 2.5 to 5.5    | 0.2            |     | 4               |      |

Note 2-1: VDD≥3.0V must be maintained when making onboard programming into flash ROM.

Note 2-2: Relationship between tCYC and oscillation frequency is 1/FmCF when frequency division ratio is 1/1 and 2/FmCF when the ratio is 1/2.

Continued on next page.

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| Parameter                                 | Symbol   | Applicable Pin /Remarks | Conditions                                                                                          | Specification       |     |          |     |      |
|-------------------------------------------|----------|-------------------------|-----------------------------------------------------------------------------------------------------|---------------------|-----|----------|-----|------|
|                                           |          |                         |                                                                                                     | V <sub>DD</sub> [V] | min | typ      | max | unit |
| Oscillation frequency range<br>(Note 2-3) | FmCF(1)  | PC3 (CF1),<br>PC4 (CF2) | 12MHz ceramic oscillator mode<br>See Fig. 1.                                                        | 4.5 to 5.5          |     | 12       |     | MHz  |
|                                           | FmCF(2)  | PC3(CF1),<br>PC4(CF2)   | 8MHz ceramic oscillator mode<br>See Fig. 1.                                                         | 3.0 to 5.5          |     | 8        |     |      |
|                                           | FmCF(3)  | PC3(CF1),<br>PC4(CF2)   | 4MHz ceramic oscillator mode<br>See Fig. 1.                                                         | 2.5 to 5.5          |     | 4        |     |      |
|                                           | FmRC     |                         | Internal RC oscillation                                                                             | 2.5 to 5.5          | 0.5 | 1.0      | 2.0 |      |
|                                           | FmSLRC   |                         | Internal low-speed RC oscillation                                                                   | 2.5 to 5.5          | 18  | 30       | 45  | kHz  |
|                                           | FsX'tal  | XT1, XT2                | 32.768kHz crystal oscillator mode<br>See Fig. 2.                                                    | 2.5 to 5.5          |     | 32.768   |     |      |
|                                           | FmVCO(1) |                         | VCO oscillator<br>When setting VC3=1<br>When SELDIV=0 or 1<br>See Fig. 9.                           | 2.5 to 3.8          | 5.0 |          | 9.0 | MHz  |
|                                           | FmVCO(2) |                         | VCO oscillator<br>When setting VC3=0<br>When SELDIV=2 or 3<br>See Fig. 9.                           | 2.5 to 3.8          | 5.0 |          | 12  |      |
|                                           | FmVCO(3) |                         | VCO oscillator<br>When setting VC3=1<br>When SELDIV=0 or 1<br>See Fig. 9.                           | 3.6 to 5.5          | 5.0 |          | 9.0 |      |
|                                           | FmVCO(4) |                         | VCO oscillator<br>When setting VC3=0<br>When SELDIV=2 or 3<br>See Fig. 9.                           | 3.6 to 5.5          | 9.0 |          | 12  |      |
|                                           | FmVCO(5) |                         | VCO oscillator<br>When OSC0=32.768KHz<br>SELDIV setting range=0 to 3<br>SELDLY setting range=0 to 3 | 2.5 to 5.5          |     | Note 2-4 |     |      |

Note 2-3: See Tables 1 and 2 for oscillator constant values.

Note 2-4: VCO oscillation frequency =  $0.032768 \times (56 \times (\text{SELDIV} + 3) + \text{SELDLY})$

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## Electrical Characteristics at Ta = -40 to +85°C, VSS1 = VSS2 = VSS3 = VSS4 = 0V

| Parameter                 | Symbol               | Applicable/<br>Remarks                                                   | Conditions                                                                                                                | VDD[V]     | Specification        |                    |     |      |
|---------------------------|----------------------|--------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------|------------|----------------------|--------------------|-----|------|
|                           |                      |                                                                          |                                                                                                                           |            | min                  | typ                | max | unit |
| High level input current  | I <sub>IH</sub> (1)  | Ports 0, 1, 2<br>Ports 3, 4, 5<br>Ports 6, 7<br>Ports A, B, C, D<br>RESB | Output disabled<br>Pull-up resistor off<br>V <sub>IN</sub> =V <sub>DD</sub><br>(Including output Tr. off leakage current) | 2.5 to 5.5 |                      |                    | 1   | μA   |
| Low level input current   | I <sub>IL</sub> (1)  | Ports 0, 1, 2<br>Ports 3, 4, 5<br>Ports 6, 7<br>Ports A, B, C, D<br>RESB | Output disabled<br>Pull-up resistor off<br>V <sub>IN</sub> =V <sub>SS</sub><br>(Including output Tr. off leakage current) | 2.5 to 5.5 | -1                   |                    |     |      |
| High level output voltage | V <sub>OH</sub> (1)  | Ports 0, 1, 2, 3                                                         | I <sub>OH</sub> =-1.0mA                                                                                                   | 4.5 to 5.5 | V <sub>DD</sub> -1   |                    |     | V    |
|                           | V <sub>OH</sub> (2)  | Ports 4, A, D<br>P40 to P45                                              | I <sub>OH</sub> =-0.4mA                                                                                                   | 3.0 to 5.5 | V <sub>DD</sub> -0.4 |                    |     |      |
|                           | V <sub>OH</sub> (3)  | PB2 to PB6                                                               | I <sub>OH</sub> =-0.2mA                                                                                                   | 2.5 to 5.5 | V <sub>DD</sub> -0.4 |                    |     |      |
|                           | V <sub>OH</sub> (4)  | Port 5, 6                                                                | I <sub>OH</sub> =-0.4mA                                                                                                   | 3.0 to 5.5 | V <sub>DD</sub> -0.4 |                    |     |      |
|                           | V <sub>OH</sub> (5)  | PC2                                                                      | I <sub>OH</sub> =-0.2mA                                                                                                   | 2.5 to 5.5 | V <sub>DD</sub> -0.4 |                    |     |      |
|                           | V <sub>OH</sub> (6)  | P46, P47                                                                 | I <sub>OH</sub> =-10mA                                                                                                    | 4.5 to 5.5 | V <sub>DD</sub> -1.5 |                    |     |      |
|                           | V <sub>OH</sub> (7)  | PB0, PB1                                                                 | I <sub>OH</sub> =-1.6mA                                                                                                   | 3.0 to 5.5 | V <sub>DD</sub> -0.4 |                    |     |      |
|                           | V <sub>OH</sub> (8)  |                                                                          | I <sub>OH</sub> =-1.0mA                                                                                                   | 2.5 to 5.5 | V <sub>DD</sub> -0.4 |                    |     |      |
|                           | V <sub>OH</sub> (9)  | PC0, PC1,<br>PC3, PC4,                                                   | I <sub>OH</sub> =-1.0mA                                                                                                   | 3.0 to 5.5 | V <sub>DD</sub> -0.4 |                    |     |      |
|                           | V <sub>OH</sub> (10) |                                                                          | I <sub>OH</sub> =-0.4mA                                                                                                   | 2.5 to 5.5 | V <sub>DD</sub> -0.4 |                    |     |      |
| Low level output voltage  | V <sub>OL</sub> (1)  | Ports 0, 1, 3, 4<br>Ports 7, D                                           | I <sub>OL</sub> =10mA                                                                                                     | 4.5 to 5.5 |                      |                    | 1.5 | V    |
|                           | V <sub>OL</sub> (2)  | P20 to P21,<br>P24 to P27                                                | I <sub>OL</sub> =1.6mA                                                                                                    | 3.0 to 5.5 |                      |                    | 0.4 |      |
|                           | V <sub>OL</sub> (3)  | PA0 to PA3<br>PA6 to PA7<br>PB0 to PB3, PB6                              | I <sub>OL</sub> =1.0mA                                                                                                    | 2.5 to 5.5 |                      |                    | 0.4 |      |
|                           | V <sub>OL</sub> (4)  | P22, P23,                                                                | I <sub>OL</sub> =11mA                                                                                                     | 4.5 to 5.5 |                      |                    | 1.5 |      |
|                           | V <sub>OL</sub> (5)  | PA4, PA5,<br>PB4, PB5                                                    | I <sub>OL</sub> =3.0mA                                                                                                    | 3.0 to 5.5 |                      |                    | 0.4 |      |
|                           | V <sub>OL</sub> (6)  |                                                                          | I <sub>OL</sub> =1.3mA                                                                                                    | 2.5 to 5.5 |                      |                    | 0.4 |      |
|                           | V <sub>OL</sub> (7)  | Ports 5, 6                                                               | I <sub>OL</sub> =1.6mA                                                                                                    | 3.0 to 5.5 |                      |                    | 0.4 |      |
|                           | V <sub>OL</sub> (8)  | PC2                                                                      | I <sub>OL</sub> =1.0mA                                                                                                    | 2.5 to 5.5 |                      |                    | 0.4 |      |
|                           | V <sub>OL</sub> (9)  | PC0, PC1,<br>PC3, PC4                                                    | I <sub>OL</sub> =1.0mA                                                                                                    | 3.0 to 5.5 |                      |                    | 0.4 |      |
|                           | V <sub>OL</sub> (10) |                                                                          | I <sub>OL</sub> =0.4mA                                                                                                    | 2.5 to 5.5 |                      |                    | 0.4 |      |
| Pull-up resistor          | Rpu(1)               | Ports 0, 1, 2, 3<br>Ports 4, 5, 6, 7                                     | V <sub>OH</sub> =0.9V <sub>DD</sub>                                                                                       | 4.5 to 5.5 | 15                   | 35                 | 80  | kΩ   |
|                           | Rpu(2)               | Ports A, B, D, PC2                                                       |                                                                                                                           | 2.5 to 4.5 | 18                   | 55                 | 150 |      |
| Hysteresis voltage        | VHYS                 | RESB<br>When ports 1, 2, 3,<br>4, A<br>PnFSAn=1                          |                                                                                                                           | 2.5 to 5.5 |                      | 0.1V <sub>DD</sub> |     | V    |
| Pin capacitance           | CP                   | All pins                                                                 | Pins other than that under test<br>V <sub>IN</sub> =V <sub>SS</sub><br>f=1MHz<br>Ta=25°C                                  | 2.5 to 5.5 |                      | 10                 |     | pF   |

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**Serial I/O Characteristics** at Ta = -40 to +85°C, V<sub>SS1</sub> = V<sub>SS2</sub> = V<sub>SS3</sub> = V<sub>SS4</sub> = 0V

**Serial I/O Characteristics (Wakeup Function Disabled) (Note 4-1-1)**

| Parameter     |                 |                        | Symbol       | Applicable Pin/Remarks | Conditions                                                                | V <sub>DD</sub> [V] | Specification |     |             |      |
|---------------|-----------------|------------------------|--------------|------------------------|---------------------------------------------------------------------------|---------------------|---------------|-----|-------------|------|
|               |                 |                        |              |                        |                                                                           |                     | min           | typ | max         | unit |
| Serial clock  | Input clock     | Period                 | tSCK(1)      | SCK0(P12)              | • See Fig. 6.                                                             | 2.5 to 5.5          | 4             |     |             | tCYC |
|               |                 | Low level pulse width  | tSCKL(1)     |                        |                                                                           |                     | 2             |     |             |      |
|               |                 | High level pulse width | tSCKH(1)     |                        |                                                                           |                     | 2             |     |             |      |
|               |                 |                        | tSCKHA(1)    |                        | • Automatic communication mode<br>• See Fig. 6.                           |                     | 6             |     |             |      |
|               |                 |                        | tSCKHBSY(1a) |                        | • Automatic communication mode<br>• See Fig. 6.                           |                     | 23            |     |             |      |
|               |                 |                        | tSCKHBSY(1b) |                        | • Mode other than automatic communication mode<br>• See Fig. 6.           |                     | 4             |     |             |      |
|               | Output clock    | Period                 | tSCK(2)      | SCK0(P12)              | • CMOS output selected<br>• See Fig. 6.                                   | 2.5 to 5.5          | 4             |     |             | tSCK |
|               |                 | Low level pulse width  | tSCKL(2)     |                        |                                                                           |                     | 1/2           |     |             |      |
|               |                 | High level pulse width | tSCKH(2)     |                        |                                                                           |                     | 1/2           |     |             |      |
|               |                 |                        | tSCKHA(2)    |                        | • Automatic communication mode<br>• CMOS output selected<br>• See Fig. 6. |                     | 6             |     |             | tCYC |
|               |                 |                        | tSCKHBSY(2a) |                        | • Automatic communication mode<br>• CMOS output selected<br>• See Fig. 6. |                     | 4             |     | 23          |      |
|               |                 |                        | tSCKHBSY(2b) |                        | • Mode other than automatic communication mode<br>• See Fig. 6.           |                     | 4             |     |             |      |
| Serial input  | Data setup time |                        | tsDI(1)      | SI0(P11), SB0(P11)     | • Specified with respect to rising edge of SIOCLK<br>• See Fig. 6.        | 2.5 to 5.5          | 0.03          |     |             |      |
|               | Data hold time  |                        | thDI(1)      |                        |                                                                           |                     | 0.03          |     |             |      |
| Serial output | Input clock     | Output delay time      | tdDO(1)      | SO0(P10), SB0(P11)     | • (Note 4-1-2)                                                            | 2.5 to 5.5          |               |     | 1tCYC +0.05 | μs   |
|               | Output clock    |                        | tdDO(2)      |                        | • (Note 4-1-2)                                                            |                     |               |     | 1tCYC +0.05 |      |

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

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## SIO0 Serial Input/Output Characteristics (Wakeup Function Enabled) (Note 4-2-1)

| Parameter     |                 |                        | Symbol      | Applicable Pin/Remarks  | Conditions                                                                                                             | V <sub>DD</sub> [V] | Specification |     |                |      |
|---------------|-----------------|------------------------|-------------|-------------------------|------------------------------------------------------------------------------------------------------------------------|---------------------|---------------|-----|----------------|------|
|               |                 |                        |             |                         |                                                                                                                        |                     | min           | typ | max            | unit |
| Serial clock  | Input clock     | Period                 | tSCK(3)     | SCK0 (P12)              | • See Fig. 6.                                                                                                          | 2.5 to 5.5          | 2             |     |                | tCYC |
|               |                 | Low level pulse width  | tSCKL(3)    |                         |                                                                                                                        |                     | 1             |     |                |      |
|               |                 | High level pulse width | tSCKH(3)    |                         |                                                                                                                        |                     | 1             |     |                |      |
|               |                 |                        | tSCKHBSY(3) |                         |                                                                                                                        |                     | 2             |     |                |      |
| Serial input  | Data setup time |                        | tsDI(2)     | SIO (P11),<br>SB0 (P11) | <ul style="list-style-type: none"> <li>Specified with respect to rising edge of SIOCLK</li> <li>See Fig. 6.</li> </ul> | 2.5 to 5.5          | 0.03          |     |                | μs   |
|               | Data hold time  |                        | thDI(2)     |                         |                                                                                                                        |                     | 0.03          |     |                |      |
| Serial output | Input clock     | Output delay time      | tdD0(3)     | SO0 (P10),<br>SB0 (P11) | • (Note 4-2-2)                                                                                                         | 2.5 to 5.5          |               |     | 1tCYC<br>+0.05 |      |

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-2-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig.6.

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## SIO1 Serial Input/Output Characteristics (Wakeup Function Disabled) (Note 4-3-1)

| Parameter     |              |                        | Symbol       | Applicable Pin/Remarks | Conditions                                                                | V <sub>DD</sub> [V] | Specification |     |             |      |
|---------------|--------------|------------------------|--------------|------------------------|---------------------------------------------------------------------------|---------------------|---------------|-----|-------------|------|
|               |              |                        |              |                        |                                                                           |                     | min           | typ | max         | unit |
| Serial clock  | Input clock  | Period                 | tSCK(4)      | SCK1(P45)              | • See Fig. 6.                                                             | 2.5 to 5.5          | 4             |     |             | tCYC |
|               |              | Low level pulse width  | tSCKL(4)     |                        |                                                                           |                     | 2             |     |             |      |
|               |              | High level pulse width | tSCKH(4)     |                        |                                                                           |                     | 2             |     |             |      |
|               |              |                        | tSCKHA(4)    |                        | • Automatic communication mode<br>• See Fig. 6.                           |                     | 6             |     |             |      |
|               |              |                        | tSCKHBSY(4a) |                        | • Automatic communication mode<br>• See Fig. 6.                           |                     | 23            |     |             |      |
|               |              |                        | tSCKHBSY(4b) |                        | • Mode other than automatic communication mode<br>• See Fig. 6.           |                     | 4             |     |             |      |
|               | Output clock | Period                 | tSCK(5)      | SCK1(P45)              | • CMOS output selected<br>• See Fig. 6.                                   | 2.5 to 5.5          | 4             |     |             | tSCK |
|               |              | Low level pulse width  | tSCKL(5)     |                        |                                                                           |                     | 1/2           |     |             |      |
|               |              | High level pulse width | tSCKH(5)     |                        |                                                                           |                     | 1/2           |     |             | tCYC |
|               |              |                        | tSCKHA(5)    |                        | • Automatic communication mode<br>• CMOS output selected<br>• See Fig. 6. |                     | 6             |     |             |      |
|               |              |                        | tSCKHBSY(5a) |                        | • Automatic communication mode<br>• CMOS output selected<br>• See Fig. 6. |                     | 4             |     | 23          |      |
|               |              |                        | tSCKHBSY(5b) |                        | • Mode other than automatic communication mode<br>• See Fig. 6.           |                     | 4             |     |             |      |
| Serial input  |              | Data setup time        | tsDI(3)      | SI1(P44), SB1(P44)     | • Specified with respect to rising edge of SIOCLK<br>• See Fig. 6.        | 2.5 to 5.5          | 0.03          |     |             | μs   |
|               |              | Data hold time         | thDI(3)      |                        |                                                                           |                     | 0.03          |     |             |      |
| Serial output | Input clock  | Output delay time      | tdD0(4)      | SO1(P43), SB1(P44)     | • (Note 4-3-2)                                                            | 2.5 to 5.5          |               |     | 1tCYC +0.05 | μs   |
|               | Output clock |                        | tdD0(5)      |                        | • (Note 4-3-2)                                                            |                     |               |     | 1tCYC +0.05 |      |

Note 4-3-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-3-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

**SIO1 Serial Input/Output Characteristics (Wakeup Function Enabled) (Note 4-4-1)**

| Parameter     |                 |                        | Symbol      | Applicable Pin/Remarks | Conditions                                                         | V <sub>DD</sub> [V] | Specification |     |             |      |
|---------------|-----------------|------------------------|-------------|------------------------|--------------------------------------------------------------------|---------------------|---------------|-----|-------------|------|
|               |                 |                        |             |                        |                                                                    |                     | min           | typ | max         | unit |
| Serial clock  | Input clock     | Period                 | tSCK(6)     | SCK1(P45)              | • See Fig. 6.                                                      | 2.5 to 5.5          | 2             |     |             | tCYC |
|               |                 | Low level pulse width  | tSCKL(6)    |                        |                                                                    |                     | 1             |     |             |      |
|               |                 | High level pulse width | tSCKH(6)    |                        |                                                                    |                     | 1             |     |             |      |
|               |                 |                        | tSCKHBSY(6) |                        |                                                                    |                     | 2             |     |             |      |
|               |                 |                        |             |                        |                                                                    |                     |               |     |             |      |
| Serial input  | Data setup time |                        | tsDI(4)     | SI1(P44), SB1(P44)     | • Specified with respect to rising edge of SIOCLK<br>• See Fig. 6. | 2.5 to 5.5          | 0.03          |     |             | μs   |
|               | Data hold time  |                        | thDI(4)     |                        |                                                                    |                     | 0.03          |     |             |      |
| Serial output | Input clock     | Output delay time      | tdD0(6)     | SO1(P43), SB1(P44)     | • (Note 4-4-2)                                                     | 2.5 to 5.5          |               |     | 1tCYC +0.05 |      |

Note 4-4-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-4-2: Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

**SMIC0 Simple SIO Mode Input/Output Characteristics**

| Parameter     |                   |                        | Symbol   | Applicable Pin/Remarks | Conditions                                                                                                                                   | V <sub>DD</sub> [V] | Specification |     |             |      |
|---------------|-------------------|------------------------|----------|------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|---------------------|---------------|-----|-------------|------|
|               |                   |                        |          |                        |                                                                                                                                              |                     | min           | typ | max         | unit |
| Serial clock  | Input clock       | Period                 | tSCK(7)  | SM0CK(P22)             | See Fig. 6.                                                                                                                                  | 2.5 to 5.5          | 4             |     |             | tCYC |
|               |                   | Low level pulse width  | tSCKL(7) |                        |                                                                                                                                              |                     | 2             |     |             |      |
|               |                   | High level pulse width | tSCKH(7) |                        |                                                                                                                                              |                     | 2             |     |             |      |
|               | Output clock      | Period                 | tSCK(8)  | SM0CK(P22)             | • CMOS output selected<br>• See Fig. 6.                                                                                                      | 2.5 to 5.5          | 4             |     |             | tSCK |
|               |                   | Low level pulse width  | tSCKL(8) |                        |                                                                                                                                              |                     | 1/2           |     |             |      |
|               |                   | High level pulse width | tSCKH(8) |                        |                                                                                                                                              |                     | 1/2           |     |             |      |
| Serial input  | Data setup time   |                        | tsDI(5)  | SM0DA(P23)             | • Specified with respect to rising edge of SIOCLK<br>• See Fig. 6.                                                                           | 2.5 to 5.5          | 0.03          |     |             | μs   |
|               | Data hold time    |                        | thDI(5)  |                        |                                                                                                                                              |                     | 0.03          |     |             |      |
| Serial output | Output delay time |                        | tdD0(7)  | SM0DO(P24), SM0DA(P23) | • Specified with respect to falling edge of SIOCLK<br>• Specified as interval up to time when output state starts changing.<br>• See Fig. 6. | 2.5 to 5.5          |               |     | 1tCYC +0.05 |      |

Note 4-5-1: These specifications are theoretical values. Add margin depending on its use.

SMIIC0 I<sup>2</sup>C Mode Input/Output Characteristics

| Parameter                                         |              |                        | Symbol                   | Applicable Pin/Remarks   | Conditions                                                                                       | V <sub>DD</sub> [V] | Specification                                                                                    |          |                          |                                                                                                |
|---------------------------------------------------|--------------|------------------------|--------------------------|--------------------------|--------------------------------------------------------------------------------------------------|---------------------|--------------------------------------------------------------------------------------------------|----------|--------------------------|------------------------------------------------------------------------------------------------|
|                                                   |              |                        |                          |                          |                                                                                                  |                     | min                                                                                              | typ      | max                      | unit                                                                                           |
| Clock                                             | Input clock  | Period                 | tSCL                     | SM0CK(P22)               | • See Fig. 8.                                                                                    | 2.5 to 5.5          | 5                                                                                                |          |                          | Tfilt                                                                                          |
|                                                   |              | Low level pulse width  | tSCLL                    |                          |                                                                                                  |                     | 2.5                                                                                              |          |                          |                                                                                                |
|                                                   |              | High level pulse width | tSCLH                    |                          |                                                                                                  |                     | 2                                                                                                |          |                          |                                                                                                |
|                                                   | Output clock | Period                 | tSCLx                    | SM0CK(P22)               | • Specified as interval up to time when output state starts changing.                            | 2.5 to 5.5          | 10                                                                                               |          |                          | tSCL                                                                                           |
|                                                   |              | Low level pulse width  | tSCLLx                   |                          |                                                                                                  |                     | 1/2                                                                                              |          |                          |                                                                                                |
|                                                   |              | High level pulse width | tSCLHx                   |                          |                                                                                                  |                     | 1/2                                                                                              |          |                          |                                                                                                |
| SM0CK and SM0DA pins input spike suppression time |              | tsp                    | SM0CK(P22)<br>SM0DA(P23) | • See Fig. 8.            | 2.5 to 5.5                                                                                       |                     |                                                                                                  | 1        | Tfilt                    |                                                                                                |
| Bus release time between start and stop           |              | Input                  | tBUF                     | SM0CK(P22)<br>SM0DA(P23) | • See Fig. 8.                                                                                    | 2.5 to 5.5          | 2.5                                                                                              |          |                          | Tfilt                                                                                          |
|                                                   |              |                        | Output                   | tBUFx                    | SM0CK(P22)<br>SM0DA(P23)                                                                         |                     | • Standard clock mode<br>• Specified as interval up to time when output state starts changing.   | 5.5      |                          |                                                                                                |
|                                                   |              |                        |                          |                          |                                                                                                  |                     | • High-speed clock mode<br>• Specified as interval up to time when output state starts changing. | 1.6      |                          |                                                                                                |
| Start/restart condition hold time                 |              | Input                  | tHD;STA                  | SM0CK(P22)<br>SM0DA(P23) | • When SMIIC register control bit, I <sup>2</sup> CSHDS=0<br>• See Fig. 8.                       | 2.5 to 5.5          | 2.0                                                                                              |          |                          | Tfilt                                                                                          |
|                                                   |              |                        |                          |                          | • When SMIIC register control bit, I <sup>2</sup> CSHDS=1<br>• See Fig. 8.                       |                     | 2.5                                                                                              |          |                          |                                                                                                |
|                                                   |              | Output                 | tHD;STAx                 | SM0CK(P22)<br>SM0DA(P23) | • Standard clock mode<br>• Specified as interval up to time when output state starts changing.   |                     | 4.1                                                                                              |          |                          | μs                                                                                             |
|                                                   |              |                        |                          |                          | • High-speed clock mode<br>• Specified as interval up to time when output state starts changing. |                     | 1.0                                                                                              |          |                          |                                                                                                |
| Restart condition setup time                      |              | Input                  | tSU;STA                  | SM0CK(P22)<br>SM0DA(P23) | • See Fig. 8.                                                                                    | 2.5 to 5.5          | 1.0                                                                                              |          |                          | Tfilt                                                                                          |
|                                                   |              |                        |                          |                          |                                                                                                  |                     | Output                                                                                           | tSU;STAx | SM0CK(P22)<br>SM0DA(P23) | • Standard clock mode<br>• Specified as interval up to time when output state starts changing. |
|                                                   |              |                        |                          |                          | • High-speed clock mode<br>• Specified as interval up to time when output state starts changing. |                     |                                                                                                  |          |                          | 1.6                                                                                            |

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| Parameter                      | Symbol | Applicable Pin/Remarks | Conditions                 | V <sub>DD</sub> [V]                                                                              | Specification |                    |     |       |
|--------------------------------|--------|------------------------|----------------------------|--------------------------------------------------------------------------------------------------|---------------|--------------------|-----|-------|
|                                |        |                        |                            |                                                                                                  | min           | typ                | max | unit  |
| Stop condition setup time      | Input  | tSU;STO                | SM0CK(P22)<br>SM0DA(P23)   | • See Fig. 8.                                                                                    | 2.5 to 5.5    | 1.0                |     | Tfilt |
|                                | Output | tSU;STOx               | SM0CK(P22)<br>SM0DA(P23)   | • Standard clock mode<br>• Specified as interval up to time when output state starts changing.   |               | 4.9                |     | μs    |
|                                |        |                        |                            | • High-speed clock mode<br>• Specified as interval up to time when output state starts changing. |               | 1.1                |     |       |
| Data hold time                 | Input  | tHD;DAT                | SM0CK(P22)<br>SM0DA(P23)   | • See Fig. 8.                                                                                    | 2.5 to 5.5    | 0                  |     | Tfilt |
|                                | Output | tHD;DATx               | SM0CK(P22)<br>SM0DA(P23)   | • Specified as interval up to time when output state starts changing.                            |               | 1                  | 1.5 |       |
| Data setup time                | Input  | tSU;DAT                | SM0CK(P22)<br>SM0DA(P23)   | • See Fig. 8.                                                                                    | 2.5 to 5.5    | 1                  |     | Tfilt |
|                                | Output | tSU;DATx               | SM0CK(P22)<br>SM0DA(P23)   | • Specified as interval up to time when output state starts changing.                            |               | 1tSCL<br>-1.5Tfilt |     |       |
| SM0CK and SM0DA pins fall time | Input  | tF                     | SM0CK(P22)<br>SM0DA(P23)   | • See Fig. 8.                                                                                    | 2.5 to 5.5    |                    | 300 | ns    |
|                                | Output | tF                     | SM0CK (P22)<br>SM0DA (P23) | • When SMIIC register control bits, PSLW=1, P5V=1                                                | 5             | 20<br>+0.1Cb       | 250 |       |
|                                |        |                        |                            | • When SMIIC register control bits, PSLW=1, P5V=0                                                | 3             | 20<br>+0.1Cb       | 250 |       |
|                                |        |                        |                            | • SM0CK, SM0DA port output FAST mode<br>• Cb≤400pF                                               | 3 to 5.5      |                    | 100 |       |

Note 4-6-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-6-2: The value of Tfilt is determined by the values of the register SMIC0BRG, bits 7 and 6 (BRP1, BRP0) and the system clock frequency.

| BRP1 | BRP0 | Tfilt  |
|------|------|--------|
| 0    | 0    | tCYC×1 |
| 0    | 1    | tCYC×2 |
| 1    | 0    | tCYC×3 |
| 1    | 1    | tCYC×4 |

Set bits (BPR1, BPR0) so that the value of Tfilt falls between the following range:

$$250\text{ns} \geq \text{Tfilt} > 140\text{ns}$$

Note 4-6-3: Cb represents the total loads (in pF) connected to the bus pins. Cb ≤ 400pF

Note 4-6-4: The standard clock mode refers to a mode that is entered by configuring SMIC0BRG as follows:

$$250\text{ns} \geq \text{Tfilt} > 140\text{ns}$$

$$\text{BRDQ (bit5)} = 1$$

$$\text{SCL frequency setting} \leq 100\text{kHz}$$

The high-speed clock mode refers to a mode that is entered by configuring SMIC0BRG as follows:

$$250\text{ns} \geq \text{Tfilt} > 140\text{ns}$$

$$\text{BRDQ (bit5)} = 0$$

$$\text{SCL frequency setting} \leq 400\text{kHz}$$

SM1C1 Simple SIO Mode Input/Output Characteristics

| Parameter     |                   |                        | Symbol   | Applicable Pin/Remarks | Conditions                                                                                                                                   | V <sub>DD</sub> [V] | Specification |     |             |      |
|---------------|-------------------|------------------------|----------|------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|---------------------|---------------|-----|-------------|------|
|               |                   |                        |          |                        |                                                                                                                                              |                     | min           | typ | max         | unit |
| Serial clock  | Input clock       | Period                 | tSCK(7)  | SM1CK(PB4)             | See Fig. 6.                                                                                                                                  | 2.5 to 5.5          | 4             |     |             | tCYC |
|               |                   | Low level pulse width  | tSCKL(7) |                        |                                                                                                                                              |                     | 2             |     |             |      |
|               |                   | High level pulse width | tSCKH(7) |                        |                                                                                                                                              |                     | 2             |     |             |      |
|               | Output clock      | Period                 | tSCK(8)  | SM1CK(PB4)             | • CMOS output selected<br>• See Fig. 6.                                                                                                      | 2.5 to 5.5          | 4             |     |             | tSCK |
|               |                   | Low level pulse width  | tSCKL(8) |                        |                                                                                                                                              |                     | 1/2           |     |             |      |
|               |                   | High level pulse width | tSCKH(8) |                        |                                                                                                                                              |                     | 1/2           |     |             |      |
| Serial input  | Data setup time   |                        | tsDI(5)  | SM1DA(PB5)             | • Specified with respect to rising edge of SIOCLK<br>• See Fig. 6.                                                                           | 2.5 to 5.5          | 0.03          |     |             | μs   |
|               | Data hold time    |                        | thDI(5)  |                        |                                                                                                                                              |                     | 0.03          |     |             |      |
| Serial output | Output delay time |                        | tdD0(7)  | SM1DO(PB6), SM1DA(PB5) | • Specified with respect to falling edge of SIOCLK<br>• Specified as interval up to time when output state starts changing.<br>• See Fig. 6. | 2.5 to 5.5          |               |     | 1tCYC +0.05 |      |

Note 4-7-1: These specifications are theoretical values. Add margin depending on its use.

SMIIC1 I<sup>2</sup>C Mode Input/Output Characteristics

| Parameter                                         |              |                                                                                                  | Symbol                   | Applicable Pin/Remarks   | Conditions                                                                                       | V <sub>DD</sub> [V] | Specification                                                                                  |          |                          |                                                                                                |
|---------------------------------------------------|--------------|--------------------------------------------------------------------------------------------------|--------------------------|--------------------------|--------------------------------------------------------------------------------------------------|---------------------|------------------------------------------------------------------------------------------------|----------|--------------------------|------------------------------------------------------------------------------------------------|
|                                                   |              |                                                                                                  |                          |                          |                                                                                                  |                     | min                                                                                            | typ      | max                      | unit                                                                                           |
| Clock                                             | Input clock  | Period                                                                                           | tSCL                     | SM1CK(PB4)               | • See Fig. 8.                                                                                    | 2.5 to 5.5          | 5                                                                                              |          |                          | Tfilt                                                                                          |
|                                                   |              | Low level pulse width                                                                            | tSCLL                    |                          |                                                                                                  |                     | 2.5                                                                                            |          |                          |                                                                                                |
|                                                   |              | High level pulse width                                                                           | tSCLH                    |                          |                                                                                                  |                     | 2                                                                                              |          |                          |                                                                                                |
|                                                   | Output clock | Period                                                                                           | tSCLx                    | SM1CK(PB4)               | • Specified as interval up to time when output state starts changing.                            | 2.5 to 5.5          | 10                                                                                             |          |                          | tSCL                                                                                           |
|                                                   |              | Low level pulse width                                                                            | tSCLLx                   |                          |                                                                                                  |                     | 1/2                                                                                            |          |                          |                                                                                                |
|                                                   |              | High level pulse width                                                                           | tSCLHx                   |                          |                                                                                                  |                     | 1/2                                                                                            |          |                          |                                                                                                |
| SM0CK and SM0DA pins input spike suppression time |              | tsp                                                                                              | SM1CK(PB4)<br>SM1DA(PB5) | • See Fig. 8.            | 2.5 to 5.5                                                                                       |                     |                                                                                                | 1        | Tfilt                    |                                                                                                |
| Bus release time between start and stop           |              | Input                                                                                            | tBUF                     | SM1CK(PB4)<br>SM1DA(PB5) | • See Fig. 8.                                                                                    | 2.5 to 5.5          | 2.5                                                                                            |          |                          | Tfilt                                                                                          |
|                                                   |              |                                                                                                  | Output                   | tBUFx                    | SM1CK(PB4)<br>SM1DA(PB5)                                                                         |                     | • Standard clock mode<br>• Specified as interval up to time when output state starts changing. | 5.5      |                          |                                                                                                |
|                                                   |              | tBUFx                                                                                            |                          |                          | • High-speed clock mode<br>• Specified as interval up to time when output state starts changing. |                     | 1.6                                                                                            |          |                          |                                                                                                |
| Start/restart condition hold time                 |              | Input                                                                                            | tHD;STA                  | SM1CK(PB4)<br>SM1DA(PB5) | • When SMIIC register control bit, I <sup>2</sup> CSHDS=0<br>• See Fig. 8.                       | 2.5 to 5.5          | 2.0                                                                                            |          |                          | Tfilt                                                                                          |
|                                                   |              |                                                                                                  |                          |                          | • When SMIIC register control bit, I <sup>2</sup> CSHDS=1<br>• See Fig. 8.                       |                     | 2.5                                                                                            |          |                          |                                                                                                |
|                                                   |              | Output                                                                                           | tHD;STAx                 | SM1CK(PB4)<br>SM1DA(PB5) | • Standard clock mode<br>• Specified as interval up to time when output state starts changing.   |                     | 4.1                                                                                            |          |                          | μs                                                                                             |
|                                                   |              |                                                                                                  |                          |                          | • High-speed clock mode<br>• Specified as interval up to time when output state starts changing. |                     | 1.0                                                                                            |          |                          |                                                                                                |
| Restart condition setup time                      |              | Input                                                                                            | tSU;STA                  | SM1CK(PB4)<br>SM1DA(PB5) | • See Fig. 8.                                                                                    | 2.5 to 5.5          | 1.0                                                                                            |          |                          | Tfilt                                                                                          |
|                                                   |              |                                                                                                  |                          |                          |                                                                                                  |                     | Output                                                                                         | tSU;STAx | SM1CK(PB4)<br>SM1DA(PB5) | • Standard clock mode<br>• Specified as interval up to time when output state starts changing. |
|                                                   |              | • High-speed clock mode<br>• Specified as interval up to time when output state starts changing. | 1.6                      |                          |                                                                                                  |                     |                                                                                                |          |                          |                                                                                                |

Continued on next page.

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Continued from preceding page

| Parameter                      |        | Symbol                | Applicable Pin/Remarks   | Conditions                                                                                       | V <sub>DD</sub> [V] | Specification                  |     |     |       |
|--------------------------------|--------|-----------------------|--------------------------|--------------------------------------------------------------------------------------------------|---------------------|--------------------------------|-----|-----|-------|
|                                |        |                       |                          |                                                                                                  |                     | min                            | typ | max | unit  |
| Stop condition setup time      | Input  | t <sub>SU</sub> ;STO  | SM1CK(PB4)<br>SM1DA(PB5) | • See Fig. 8.                                                                                    | 2.5 to 5.5          | 1.0                            |     |     | Tfilt |
|                                | Output | t <sub>SU</sub> ;STOx | SM1CK(PB4)<br>SM1DA(PB5) | • Standard clock mode<br>• Specified as interval up to time when output state starts changing.   |                     | 4.9                            |     |     | μs    |
|                                |        |                       |                          | • High-speed clock mode<br>• Specified as interval up to time when output state starts changing. |                     | 1.1                            |     |     |       |
| Data hold time                 | Input  | t <sub>HD</sub> ;DAT  | SM1CK(PB4)<br>SM1DA(PB5) | • See Fig. 8.                                                                                    | 2.5 to 5.5          | 0                              |     |     | Tfilt |
|                                | Output | t <sub>HD</sub> ;DATx | SM1CK(PB4)<br>SM1DA(PB5) | • Specified as interval up to time when output state starts changing.                            |                     | 1                              |     | 1.5 |       |
| Data setup time                | Input  | t <sub>SU</sub> ;DAT  | SM1CK(PB4)<br>SM1DA(PB5) | • See Fig. 8.                                                                                    | 2.5 to 5.5          | 1                              |     |     | Tfilt |
|                                | Output | t <sub>SU</sub> ;DATx | SM1CK(PB4)<br>SM1DA(PB5) | • Specified as interval up to time when output state starts changing.                            |                     | 1t <sub>SCL</sub><br>-1.5Tfilt |     |     |       |
| SM0CK and SM0DA pins fall time | Input  | t <sub>F</sub>        | SM1CK(PB4)<br>SM1DA(PB5) | • See Fig. 8.                                                                                    | 2.5 to 5.5          |                                |     | 300 | ns    |
|                                | Output | t <sub>F</sub>        | SM1CK(PB4)<br>SM1DA(PB5) | • When SMIIC register control bits PSLW=1, P5V=1                                                 | 5                   | 20<br>+0.1Cb                   |     | 250 |       |
|                                |        |                       |                          | • When SMIIC register control bits PSLW=1, P5V=0                                                 | 3                   | 20<br>+0.1Cb                   |     | 250 |       |
|                                |        |                       |                          | • SM0CK, SM0DA port output FAST mode<br>• Cb≤400pF                                               | 3 to 5.5            |                                |     | 100 |       |

Note 4-8-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-8-2: The value of Tfilt is determined by the values of the register SMIC1BRG, bits 7 and 6 (BRP1, BRP0) and the system clock frequency.

| BRP1 | BRP0 | Tfilt  |
|------|------|--------|
| 0    | 0    | tCYC×1 |
| 0    | 1    | tCYC×2 |
| 1    | 0    | tCYC×3 |
| 1    | 1    | tCYC×4 |

Set bits (BPR1, BPR0) so that the value of Tfilt falls between the following range:

$$250\text{ns} \geq \text{Tfilt} > 140\text{ns}$$

Note 4-8-3: Cb represents the total loads (in pF) connected to the bus pins. Cb ≤ 400pF

Note 4-8-4: The standard clock mode refers to a mode that is entered by configuring SMIC1BRG as follows:

$$250\text{ns} \geq \text{Tfilt} > 140\text{ns}$$

$$\text{BRDQ (bit5)} = 1$$

$$\text{SCL frequency setting} \leq 100\text{kHz}$$

The high-speed clock mode refers to a mode that is entered by configuring SMIC1BRG as follows:

$$250\text{ns} \geq \text{Tfilt} > 140\text{ns}$$

$$\text{BRDQ (bit5)} = 0$$

$$\text{SCL frequency setting} \leq 400\text{kHz}$$

SLIIC0 Simple SIO Mode Input/Output Characteristics

| Parameter     |                   |                        | Symbol   | Applicable Pin/Remarks    | Conditions                                                                                                                                                                                           | V <sub>DD</sub> [V] | Specification |     |                |      |
|---------------|-------------------|------------------------|----------|---------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|---------------|-----|----------------|------|
|               |                   |                        |          |                           |                                                                                                                                                                                                      |                     | min           | typ | max            | unit |
| Serial clock  | Input clock       | Period                 | tSCK(9)  | SL0CK(PA4)                | See Fig. 6.                                                                                                                                                                                          | 2.5 to 5.5          | 4             |     |                | tCYC |
|               |                   | Low level pulse width  | tSCKL(9) |                           |                                                                                                                                                                                                      |                     | 2             |     |                |      |
|               |                   | High level pulse width | tSCKH(9) |                           |                                                                                                                                                                                                      |                     | 2             |     |                |      |
| Serial input  | Data setup time   |                        | tsDI(7)  | SL0DA(PA5)                | <ul style="list-style-type: none"> <li>Specified with respect to rising edge of SIOCLK</li> <li>See Fig. 6.</li> </ul>                                                                               | 2.5 to 5.5          | 0.03          |     |                | μs   |
|               | Data hold time    |                        | thDI(7)  |                           |                                                                                                                                                                                                      |                     | 0.03          |     |                |      |
| Serial output | Output delay time |                        | tdD0(9)  | SL0DO(PA6),<br>SL0DA(PA5) | <ul style="list-style-type: none"> <li>Specified with respect to falling edge of SIOCLK</li> <li>Specified as interval up to time when output state starts changing.</li> <li>See Fig. 6.</li> </ul> | 2.5 to 5.5          |               |     | 1tCYC<br>+0.05 |      |

Note 4-9-1: These specifications are theoretical values. Add margin depending on its use.

SLIIC1 I<sup>2</sup>C Mode Input/Output Characteristics

| Parameter                                         |             |                        | Symbol   | Applicable Pin/Remarks   | Conditions                                                                 | V <sub>DD</sub> [V] | Specification      |     |     |       |
|---------------------------------------------------|-------------|------------------------|----------|--------------------------|----------------------------------------------------------------------------|---------------------|--------------------|-----|-----|-------|
|                                                   |             |                        |          |                          |                                                                            |                     | min                | typ | max | unit  |
| Clock                                             | Input clock | Period                 | tSCL     | SLOCK(PA4)               | • See Fig. 8.                                                              | 2.5 to 5.5          | 5                  |     |     | Tfilt |
|                                                   |             | Low level pulse width  | tSCLL    |                          |                                                                            |                     | 2.5                |     |     |       |
|                                                   |             | High level pulse width | tSCLH    |                          |                                                                            |                     | 2                  |     |     |       |
| SLOCK and SLODA pins input spike suppression time |             |                        | tsp      | SLOCK(PA4)<br>SLODA(PA5) | • See Fig. 8.                                                              | 2.5 to 5.5          |                    |     | 1   | Tfilt |
| Bus release time between start and stop           |             | Input                  | tBUF     | SLOCK(PA4)<br>SLODA(PA5) | • See Fig. 8.                                                              | 2.5 to 5.5          | 2.5                |     |     | Tfilt |
| Start/restart condition hold time                 |             | Input                  | tHD;STA  | SLOCK(PA4)<br>SLODA(PA5) | • When SMIIC register control bit, I <sup>2</sup> CSHDS=0<br>• See Fig. 8. | 2.5 to 5.5          | 2.0                |     |     | Tfilt |
|                                                   |             |                        |          |                          | • When SMIIC register control bit I <sup>2</sup> CSHDS=1<br>• See Fig. 8.  |                     | 2.5                |     |     |       |
| Restart condition setup time                      |             | Input                  | tSU;STA  | SLOCK(PA4)<br>SLODA(PA5) | • See Fig. 8.                                                              | 2.5 to 5.5          | 1.0                |     |     | Tfilt |
| Stop condition setup time                         |             | Input                  | tSU;STO  | SLOCK(PA4)<br>SLODA(PA5) | • See Fig. 8.                                                              | 2.5 to 5.5          | 1.0                |     |     | Tfilt |
| Data hold time                                    |             | Input                  | tHD;DAT  | SLOCK(PA4)<br>SLODA(PA5) | • See Fig. 8.                                                              | 2.5 to 5.5          | 0                  |     |     | Tfilt |
|                                                   |             | Output                 | tHD;DATx | SLOCK(PA4)<br>SLODA(PA5) | • Specified as interval up to time when output state starts changing.      |                     | 1                  |     | 1.5 |       |
| Data setup time                                   |             | Input                  | tSU;DAT  | SLOCK(PA4)<br>SLODA(PA5) | • See Fig. 8.                                                              | 2.5 to 5.5          | 1                  |     |     | Tfilt |
|                                                   |             | Output                 | tSU;DATx | SLOCK(PA4)<br>SLODA(PA5) | • Specified as interval up to time when output state starts changing.      |                     | 1tSCL<br>-1.5Tfilt |     |     |       |

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### UART0 Operating Conditions at Ta = -40 to +85°C, VSS1 = VSS2 = VSS3 = VSS4 = 0V

| Parameter     | Symbol | Applicable Pin/Remarks                 | Conditions | Specification       |     |     |     |        |
|---------------|--------|----------------------------------------|------------|---------------------|-----|-----|-----|--------|
|               |        |                                        |            | V <sub>DD</sub> [V] | min | typ | max | unit   |
| Transfer rate | UBR0   | U0RX(P13),<br>U0TX(P14),<br>U0BRG(P07) |            | 2.5 to 5.5          | 4   |     | 8   | tBGCYC |

Note 4-9: tBGCYC denotes one cycle of the baudrate clock source.

### UART2 Operating Conditions at Ta = -40 to +85°C, VSS1 = VSS2 = VSS3 = VSS4 = 0V

| Parameter     | Symbol | Applicable Pin/Remarks  | Conditions | Specification       |     |     |      |        |
|---------------|--------|-------------------------|------------|---------------------|-----|-----|------|--------|
|               |        |                         |            | V <sub>DD</sub> [V] | min | typ | max  | unit   |
| Transfer rate | UBR2   | U2RX(P16),<br>U2TX(P17) |            | 2.5 to 5.5          | 8   |     | 4096 | tBGCYC |

Note 4-10: tBGCYC denotes one cycle of the baudrate clock source.

### UART3 Operating Conditions at Ta = -40 to +85°C, VSS1 = VSS2 = VSS3 = VSS4 = 0V

| Parameter     | Symbol | Applicable Pin/Remarks  | Conditions | Specification       |     |     |      |        |
|---------------|--------|-------------------------|------------|---------------------|-----|-----|------|--------|
|               |        |                         |            | V <sub>DD</sub> [V] | min | typ | max  | unit   |
| Transfer rate | UBR3   | U3RX(P34),<br>U3TX(P35) |            | 2.5 to 5.5          | 8   |     | 4096 | tBGCYC |

Note 4-10: tBGCYC denotes one cycle of the baudrate clock source.

### UART4 Operating Conditions at Ta = -40 to +85°C, VSS1 = VSS2 = VSS3 = VSS4 = 0V

| Parameter     | Symbol | Applicable Pin/Remarks  | Conditions | Specification       |     |     |      |        |
|---------------|--------|-------------------------|------------|---------------------|-----|-----|------|--------|
|               |        |                         |            | V <sub>DD</sub> [V] | min | typ | max  | unit   |
| Transfer rate | UBR4   | U4RX(PB2),<br>U4TX(PB3) |            | 2.5 to 5.5          | 8   |     | 4096 | tBGCYC |

Note 4-10: tBGCYC denotes one cycle of the baudrate clock source.

### Pulse Input Conditions at Ta = -40 to +85°C, VSS1 = VSS2 = VSS3 = VSS4 = 0V

| Parameter                  | Symbol             | Applicable Pin/Remarks                                                                                      | Conditions                                                                                                                                | Specification       |     |     |     |      |
|----------------------------|--------------------|-------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|---------------------|-----|-----|-----|------|
|                            |                    |                                                                                                             |                                                                                                                                           | V <sub>DD</sub> [V] | min | typ | max | unit |
| High/low level pulse width | tPIH(1)<br>tPIL(1) | INT0(P30),<br>INT1(P31),<br>INT2(P32),<br>INT3(P33),<br>INT4(P20),<br>INT5(P21),<br>INT6(P40),<br>INT7(P41) | <ul style="list-style-type: none"> <li>Interrupt source flag can be set.</li> <li>Event inputs for timers 2 and 3 are enabled.</li> </ul> | 2.5 to 5.5          | 2   |     |     | tCYC |
|                            | tPIL(2)            | RESB                                                                                                        | Resetting is enabled.                                                                                                                     | 2.5 to 5.5          | 10  |     |     | μs   |

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**AD Converter Characteristics** at Ta = -40 to +85°C, VSS1 = VSS2 = VSS3 = VSS4 = 0V

### 12-bit AD Conversion Mode

| Parameter                  | Symbol | Applicable Pin /Remarks  | Conditions                 | VDD[V]     | Specification |     |     |      |
|----------------------------|--------|--------------------------|----------------------------|------------|---------------|-----|-----|------|
|                            |        |                          |                            |            | min           | typ | max | unit |
| Resolution                 | NAD    | AN0(P60) to              |                            | 3.0 to 5.5 |               | 12  |     | bit  |
| Absolute accuracy          | ETAD   | AN7(P67),                | (Note 6-1)                 | 3.0 to 5.5 |               |     | ±16 | LSB  |
| Conversion time            | TCAD12 | AN8(P70) to<br>AN15(P77) | Conversion time calculated | 4.5 to 5.5 | 27            |     | 209 | μs   |
|                            |        |                          |                            | 3.0 to 5.5 | 67            |     | 209 |      |
| Analog input voltage range | VAIN   |                          |                            | 3.0 to 5.5 | VSS           |     | VDD | V    |
| Analog port input current  | IAINH  |                          | VAIN=VDD                   | 3.0 to 5.5 |               |     | 1   | μA   |
|                            | IAINL  |                          | VAIN=VSS                   | 3.0 to 5.5 | -1            |     |     |      |

Conversion time calculation formula: TCAD12= ((52/(AD division ratio))+2) × tCYC

### 8-bit AD Conversion Mode

| Parameter                  | Symbol | Applicable Pin /Remarks  | Conditions                 | VDD[V]     | Specification |     |      |      |
|----------------------------|--------|--------------------------|----------------------------|------------|---------------|-----|------|------|
|                            |        |                          |                            |            | min           | typ | max  | unit |
| Resolution                 | NAD    | AN0(P60) to              |                            | 3.0 to 5.5 |               | 8   |      | bit  |
| Absolute accuracy          | ETAD   | AN7(P67),                | (Note 6-1)                 | 3.0 to 5.5 |               |     | ±1.5 | LSB  |
| Conversion time            | TCAD8  | AN8(P70) to<br>AN15(P77) | Conversion time calculated | 4.5 to 5.5 | 17            |     | 129  | μs   |
|                            |        |                          |                            | 3.0 to 5.5 | 42            |     | 129  |      |
| Analog input voltage range | VAIN   |                          |                            | 3.0 to 5.5 | VSS           |     | VDD  | V    |
| Analog port input current  | IAINH  |                          | VAIN=VDD                   | 3.0 to 5.5 |               |     | 1    | μA   |
|                            | IAINL  |                          | VAIN=VSS                   | 3.0 to 5.5 | -1            |     |      |      |

Conversion time calculation formula: TCAD8= ((32/(AD division ratio))+2) × tCYC

Note 6-1: The quantization error (±1/2LSB) is excluded from the absolute accuracy.

Note 6-2: The conversion time refers to the interval from the time a conversion starting instruction is issued till the time the complete digital value against the analog input value is loaded in the result register.

The conversion time is twice the normal value when one of the following conditions occurs:

- The first AD conversion is executed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is executed after the AD conversion mode is switched from 8-bit to 12-bit AD conversion mode.

**DA Converter Characteristics** at Ta=-40 to+85°C, VSS1=VSS2=VSS3=VSS4=0V

| Parameter                  | Symbol | Applicable Pin /Remarks   | Conditions | VDD[V]     | Specification |      |      |      |
|----------------------------|--------|---------------------------|------------|------------|---------------|------|------|------|
|                            |        |                           |            |            | min           | typ  | max  | unit |
| Resolution                 | NDA    | DA00(PD0) to              |            | 3.0 to 5.5 |               | 8    |      | bit  |
| Absolute accuracy          | ETDA   | DA02(PD2)                 |            | 3.0 to 5.5 |               |      | ±2.0 | LSB  |
| Output resistor            | DAOR   | DA10(PD3) to<br>DA12(PD5) |            | 3.0 to 5.5 | 9.5           | 16.0 | 22.9 | kΩ   |
| Analog port output current | VDAOUT |                           |            | 3.0 to 5.5 | VSS           |      | VDD  | V    |

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**Consumption Current Characteristics** at Ta=-40 to +85°C, V<sub>SS1</sub>=V<sub>SS2</sub>=V<sub>SS3</sub>=V<sub>SS4</sub>=0V  
typ: 5.0V (V<sub>DD</sub>=4.5V to 5.5V), 3.3V (V<sub>DD</sub>=3.0V to 4.5V, 2.2V to 4.5V)

| Parameter                                     | Symbol    | Applicable Pin/Remarks                                                          | Conditions                                                                                                                                                                                                                                                                                | Specification       |     |      |      |      |
|-----------------------------------------------|-----------|---------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|-----|------|------|------|
|                                               |           |                                                                                 |                                                                                                                                                                                                                                                                                           | V <sub>DD</sub> [V] | min | typ  | max  | unit |
| Normal mode consumption current<br>(Note 7-1) | IDDOP(1)  | V <sub>DD1</sub><br>=V <sub>DD2</sub><br>=V <sub>DD3</sub><br>=V <sub>DD4</sub> | <ul style="list-style-type: none"> <li>FmCF=12MHz ceramic oscillation mode</li> <li>FmX'tal=32.768kHz crystal oscillation mode</li> <li>System clock set to 12MHz</li> <li>Internal RC oscillation stopped</li> <li>1/1 frequency division mode</li> </ul>                                | 4.5 to 5.5          |     | 10.4 | 19   | mA   |
|                                               | IDDOP(2)  |                                                                                 | <ul style="list-style-type: none"> <li>FmCF=8MHz ceramic oscillator mode</li> <li>FmX'tal=32.768kHz crystal oscillator mode</li> <li>System clock set to 8MHz</li> <li>Internal RC oscillation stopped</li> <li>1/1 frequency division mode</li> </ul>                                    | 4.5 to 5.5          |     | 8.50 | 17   |      |
|                                               | IDDOP(3)  |                                                                                 | <ul style="list-style-type: none"> <li>FmCF=4MHz ceramic oscillator mode</li> <li>FmX'tal=32.768kHz crystal oscillator mode</li> <li>System clock set to 4MHz</li> <li>Internal RC oscillation stopped</li> <li>1/2 frequency division mode</li> </ul>                                    | 3.0 to 4.5          |     | 4.91 | 13   |      |
|                                               | IDDOP(4)  |                                                                                 | <ul style="list-style-type: none"> <li>FmCF=0Hz (oscillation stopped)</li> <li>FmX'tal=32.768kHz crystal oscillator mode</li> <li>System clock set to internal RC oscillation</li> <li>1/1 frequency division mode</li> </ul>                                                             | 4.5 to 5.5          |     | 4.02 | 6.1  |      |
|                                               | IDDOP(5)  |                                                                                 | <ul style="list-style-type: none"> <li>FmCF=0Hz (oscillation stopped)</li> <li>FmX'tal=32.768kHz crystal oscillator mode</li> <li>System clock set to 32.768kHz</li> <li>Internal RC oscillation stopped</li> <li>1/1 frequency division mode</li> </ul>                                  | 2.5 to 4.5          |     | 2.62 | 4.3  |      |
|                                               | IDDOP(6)  |                                                                                 | <ul style="list-style-type: none"> <li>FmCF=0Hz (oscillation stopped)</li> <li>FmX'tal=32.768kHz crystal oscillator mode</li> <li>System clock set to 32.768kHz</li> <li>Internal RC oscillation stopped</li> <li>1/1 frequency division mode</li> </ul>                                  | 4.5 to 5.5          |     | 2.18 | 6.0  |      |
|                                               | IDDOP(7)  |                                                                                 | <ul style="list-style-type: none"> <li>FmCF=0Hz (oscillation stopped)</li> <li>FmX'tal=32.768kHz crystal oscillator mode</li> <li>System clock set to 32.768kHz</li> <li>Internal RC oscillation stopped</li> <li>1/1 frequency division mode</li> </ul>                                  | 2.2 to 4.5          |     | 1.28 | 4.2  |      |
|                                               | IDDOP(8)  |                                                                                 | <ul style="list-style-type: none"> <li>FmCF=0Hz (oscillation stopped)</li> <li>FmX'tal=32.768kHz crystal oscillator mode</li> <li>System clock set to 32.768kHz</li> <li>Internal RC oscillation stopped</li> <li>1/1 frequency division mode</li> </ul>                                  | 4.5 to 5.5          |     | 72.9 | 195  | μA   |
|                                               | IDDOP(9)  |                                                                                 | <ul style="list-style-type: none"> <li>FmCF=0Hz (oscillation stopped)</li> <li>FmX'tal=32.768kHz crystal oscillator mode</li> <li>System clock set to 32.768kHz</li> <li>Internal RC oscillation stopped</li> <li>1/1 frequency division mode</li> </ul>                                  | 2.2 to 4.5          |     | 39.8 | 160  |      |
|                                               | IDDOP(10) |                                                                                 | <ul style="list-style-type: none"> <li>FmCF=0Hz (oscillation stopped)</li> <li>FmVCO=11.1MHz oscillator mode</li> <li>FmX'tal=32.768kHz crystal oscillator mode</li> <li>System clock set to VCO</li> <li>Internal RC oscillation stopped</li> <li>1/1 frequency division mode</li> </ul> | 4.5 to 5.5          |     | 10.5 | 19.2 | mA   |
|                                               | IDDOP(11) |                                                                                 | <ul style="list-style-type: none"> <li>FmCF=0Hz (oscillation stopped)</li> <li>FmVCO=7.34MHz oscillator mode</li> <li>FmX'tal=32.768kHz crystal oscillator mode</li> <li>System clock set to VCO</li> <li>Internal RC oscillation stopped</li> <li>1/1 frequency division mode</li> </ul> | 4.5 to 5.5          |     | 9.07 | 17.3 |      |
|                                               | IDDOP(12) |                                                                                 | <ul style="list-style-type: none"> <li>FmCF=0Hz (oscillation stopped)</li> <li>FmVCO=7.34MHz oscillator mode</li> <li>FmX'tal=32.768kHz crystal oscillator mode</li> <li>System clock set to VCO</li> <li>Internal RC oscillation stopped</li> <li>1/1 frequency division mode</li> </ul> | 3.0 to 4.5          |     | 5.23 | 13.8 |      |

Note 7-1: The consumption current value includes none of the currents that flow into the output transistor and internal pull-up resistors.

Continued on next page.

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Continued from preceding page.

| Parameter                                   | Symbol      | Applicable Pin/Remarks                                                          | Conditions                                                                                                                                                                                                                                                                                                                 | Specification       |     |      |     |      |
|---------------------------------------------|-------------|---------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|-----|------|-----|------|
|                                             |             |                                                                                 |                                                                                                                                                                                                                                                                                                                            | V <sub>DD</sub> [V] | min | typ  | max | unit |
| HALT mode consumption current<br>(Note 7-1) | IDDHALT(1)  | V <sub>DD1</sub><br>=V <sub>DD2</sub><br>=V <sub>DD3</sub><br>=V <sub>DD4</sub> | <ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF=12MHz ceramic mode</li> <li>• FmX'tal=32.768kHz crystal oscillation mode</li> <li>• System clock set to 12MHz</li> <li>• Internal RC oscillation stopped</li> <li>• 1/1 frequency division mode</li> </ul>                                              | 4.5 to 5.5          |     | 3.70 | 6.5 | mA   |
|                                             | IDDHALT(2)  |                                                                                 | <ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF=10MHz ceramic oscillator mode</li> <li>• FmX'tal=32.768kHz crystal oscillator mode</li> <li>• System clock set to 10MHz</li> <li>• Internal RC oscillation stopped</li> <li>• 1/1 frequency division mode</li> </ul>                                    | 4.5 to 5.5          |     | 2.60 | 5.0 |      |
|                                             | IDDHALT(3)  |                                                                                 | <ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF=10MHz ceramic oscillator mode</li> <li>• FmX'tal=32.768kHz crystal oscillator mode</li> <li>• System clock set to 10MHz</li> <li>• Internal RC oscillation stopped</li> <li>• 1/1 frequency division mode</li> </ul>                                    | 3.0 to 4.5          |     | 1.34 | 3.5 |      |
|                                             | IDDHALT(4)  |                                                                                 | <ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF=4MHz ceramic oscillator mode</li> <li>• FmX'tal=32.768kHz crystal oscillator mode</li> <li>• System clock set to 4MHz</li> <li>• Internal RC oscillation stopped</li> <li>• 1/2 frequency division mode</li> </ul>                                      | 4.5 to 5.5          |     | 1.08 | 3.1 |      |
|                                             | IDDHALT(5)  |                                                                                 | <ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF=4MHz ceramic oscillator mode</li> <li>• FmX'tal=32.768kHz crystal oscillator mode</li> <li>• System clock set to 4MHz</li> <li>• Internal RC oscillation stopped</li> <li>• 1/2 frequency division mode</li> </ul>                                      | 2.2 to 4.5          |     | 0.50 | 2.2 |      |
|                                             | IDDHALT(6)  |                                                                                 | <ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF=0Hz (oscillation stopped)</li> <li>• FmX'tal=32.768kHz crystal oscillator mode</li> <li>• System clock set to internal RC oscillation</li> <li>• 1/1 frequency division mode</li> </ul>                                                                 | 4.5 to 5.5          |     | 0.53 | 3.0 |      |
|                                             | IDDHALT(7)  |                                                                                 | <ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF=0Hz (oscillation stopped)</li> <li>• FmX'tal=32.768kHz crystal oscillator mode</li> <li>• System clock set to internal RC oscillation</li> <li>• 1/1 frequency division mode</li> </ul>                                                                 | 2.2 to 4.5          |     | 0.26 | 2.1 |      |
|                                             | IDDHALT(8)  |                                                                                 | <ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF=0Hz (oscillation stopped)</li> <li>• FmX'tal=32.768kHz crystal oscillator mode</li> <li>• System clock set to 32.768kHz</li> <li>• Internal RC oscillation stopped</li> <li>• 1/1 frequency division mode</li> </ul>                                    | 4.5 to 5.5          |     | 27.3 | 145 | μA   |
|                                             | IDDHALT(9)  |                                                                                 | <ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF=0Hz (oscillation stopped)</li> <li>• FmX'tal=32.768kHz crystal oscillator mode</li> <li>• System clock set to 32.768kHz</li> <li>• Internal RC oscillation stopped</li> <li>• 1/1 frequency division mode</li> </ul>                                    | 2.2 to 4.5          |     | 9.52 | 112 |      |
|                                             | IDDHALT(10) |                                                                                 | <ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF=0Hz (oscillation stopped)</li> <li>• FmVCO=11.1MHz oscillator mode</li> <li>• FmX'tal=32.768kHz crystal oscillator mode</li> <li>• System clock set to VCO</li> <li>• Internal RC oscillation stopped</li> <li>• 1/1 frequency division mode</li> </ul> | 4.5 to 5.5          |     | 4.19 | 6.8 | mA   |
|                                             | IDDHALT(11) |                                                                                 | <ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF=0Hz (oscillation stopped)</li> <li>• FmVCO=7.34MHz oscillator mode</li> <li>• FmX'tal=32.768kHz crystal oscillator mode</li> <li>• System clock set to VCO</li> <li>• Internal RC oscillation stopped</li> <li>• 1/1 frequency division mode</li> </ul> | 4.5 to 5.5          |     | 3.18 | 5.5 |      |
|                                             | IDDHALT(12) |                                                                                 | <ul style="list-style-type: none"> <li>• HALT mode</li> <li>• FmCF=0Hz (oscillation stopped)</li> <li>• FmVCO=7.34MHz oscillator mode</li> <li>• FmX'tal=32.768kHz crystal oscillator mode</li> <li>• System clock set to VCO</li> <li>• Internal RC oscillation stopped</li> <li>• 1/1 frequency division mode</li> </ul> | 3.0 to 4.5          |     | 1.68 | 4.0 |      |
| HOLD mode consumption current               | IDDHOLD(1)  | V <sub>DD1</sub>                                                                | <ul style="list-style-type: none"> <li>• HOLD mode</li> <li>• CF1=V<sub>DD</sub> or open (external clock mode)</li> </ul>                                                                                                                                                                                                  | 4.5 to 5.5          |     | 0.11 | 98  | μA   |
|                                             | IDDHOLD(2)  |                                                                                 | <ul style="list-style-type: none"> <li>• HOLD mode</li> <li>• CF1=V<sub>DD</sub> or open (external clock mode)</li> </ul>                                                                                                                                                                                                  | 2.5 to 4.5          |     | 0.04 | 72  |      |
|                                             | IDDHOLD(3)  |                                                                                 | <ul style="list-style-type: none"> <li>• HOLD mode</li> <li>• CF1=V<sub>DD</sub> or open (external clock mode)</li> <li>• FmX'tal=32.768kHz crystal oscillator mode</li> </ul>                                                                                                                                             | 4.5 to 5.5          |     | 19.0 | 132 |      |
|                                             | IDDHOLD(4)  |                                                                                 | <ul style="list-style-type: none"> <li>• HOLD mode</li> <li>• CF1=V<sub>DD</sub> or open (external clock mode)</li> <li>• FmX'tal=32.768kHz crystal oscillator mode</li> </ul>                                                                                                                                             | 2.5 to 4.5          |     | 4.91 | 90  |      |

Note 7-1: The consumption current value includes none of the currents that flow into the output transistor and internal pull-up resistors.

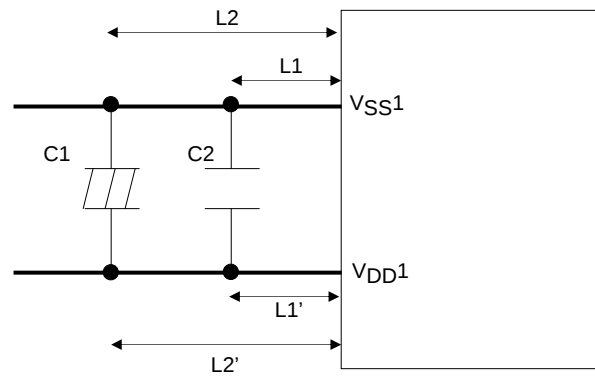
**F-ROM Programming Characteristics** at  $T_a = +10^{\circ}\text{C}$  to  $+55^{\circ}\text{C}$ ,  $V_{SS1}=V_{SS2}=V_{SS3}=V_{SS4}=0\text{V}$

| Parameter                   | Symbol        | Applicable Pin/Remarks | Conditions                                           | $V_{DD}[\text{V}]$ | Specification |     |     |               |
|-----------------------------|---------------|------------------------|------------------------------------------------------|--------------------|---------------|-----|-----|---------------|
|                             |               |                        |                                                      |                    | min           | typ | max | unit          |
| Onboard programming current | $I_{DDFW}(1)$ | $V_{DD1}$              | • Microcontroller erase current current is excluded. | 3.0 to 5.5         |               |     | 15  | mA            |
| Onboard programming time    | $t_{FW}(1)$   |                        | • 512-/1K-byte erase operation                       | 3.0 to 5.5         |               |     | 30  | ms            |
|                             | $t_{FW}(2)$   |                        | • 2-byte programming operation                       | 3.0 to 5.5         |               |     | 60  | $\mu\text{s}$ |

**Power Pin Treatment Conditions 1 ( $V_{DD1}$ ,  $V_{SS1}$ )**

Connect capacitors that meet the following conditions between the  $V_{DD1}$  and  $V_{SS1}$  pins:

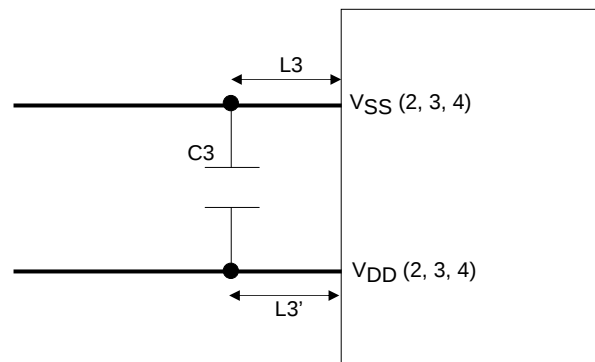
- Connect among the  $V_{DD1}$  and  $V_{SS1}$  pins and the capacitors C1 and C2 with the shortest possible lead wires, of the same length ( $L1=L1'$ ,  $L2=L2'$ ) wherever possible.
- Connect a large-capacity capacitor C1 and a small-capacity capacitor C2 in parallel.  
The capacitance of C2 should be approximately  $0.1\mu\text{F}$  or larger.
- The  $V_{DD1}$  and  $V_{SS1}$  traces must be thicker than the other traces.



**Power Pin Treatment Conditions 2 ( $V_{DD}(2, 3, 4)$ ,  $V_{SS}(2, 3, 4)$ )**

Connect capacitors that meet the following condition between the  $V_{DD}(2, 3, 4)$  and  $V_{SS}(2, 3, 4)$  pins:

- Connect among the  $V_{DD}(2, 3, 4)$  and  $V_{SS}(2, 3, 4)$  pins and the capacitor C3 with the shortest possible lead wires, of the same length ( $L3=L3'$ ) wherever possible.
- The capacitance of C3 should be approximately  $0.1\mu\text{F}$  or larger.
- The  $V_{DD}(2, 3, 4)$  and  $V_{SS}(2, 3, 4)$  traces must be thicker than the other traces.



## Characteristics of a Sample OSC1 System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Resonator

| Nominal<br>Frequency | Vendor<br>Name | Resonator       | Circuit Constant |            |           |            | Operating<br>Voltage<br>Range<br>[V] | Oscillation<br>Stabilization Time |             | Remarks                   |
|----------------------|----------------|-----------------|------------------|------------|-----------|------------|--------------------------------------|-----------------------------------|-------------|---------------------------|
|                      |                |                 | C3<br>[pF]       | C4<br>[pF] | Rf<br>[Ω] | Rd2<br>[Ω] |                                      | typ<br>[ms]                       | max<br>[ms] |                           |
| 12MHz                | MURATA         | CSTCE12M0G52-R0 | (10)             | (10)       | OPEN      | 470        | 2.4 to 5.5                           | 0.02                              | 0.2         | C1, C2<br>integrated type |
| 8MHz                 |                | CSTCE8M00G52-R0 | (10)             | (10)       | OPEN      | 1k         | 2.3 to 5.5                           | 0.02                              | 0.2         | C1, C2<br>integrated type |
|                      |                | CSTLS8M00G53-B0 | (15)             | (15)       | OPEN      | 1k         | 2.5 to 5.5                           | 0.02                              | 0.2         | C1, C2<br>integrated type |
| 4MHz                 |                | CSTCR4M00G53-R0 | (15)             | (15)       | OPEN      | 1.5k       | 2.2 to 5.5                           | 0.02                              | 0.2         | C1, C2<br>integrated type |
|                      |                | CSTLS4M00G53-B0 | (15)             | (15)       | OPEN      | 1.5k       | 2.3 to 5.5                           | 0.02                              | 0.2         | C1, C2<br>integrated type |

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after VDD goes above the lower limit level of the operating voltage range (see Figure 4)

## Characteristics of a Sample System Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Resonator

| Nominal Frequency | Vendor Name   | Oscillator Name | Circuit Constant |         |                  |                  | Operating Voltage Range [V] | Oscillation Stabilization Time |         | Remarks                   |
|-------------------|---------------|-----------------|------------------|---------|------------------|------------------|-----------------------------|--------------------------------|---------|---------------------------|
|                   |               |                 | C3 [pF]          | C4 [pF] | Rf2 [ $\Omega$ ] | Rd2 [ $\Omega$ ] |                             | typ [s]                        | max [s] |                           |
| 32.768kHz         | EPSON TOYOCOM | MC-306          | 10               | 10      | OPEN             | 0                | 2.2 to 5.5                  | 0.8                            | 2       | Applicable CL value=7.0pF |

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillator circuit is executed plus the time interval that is required for the oscillation to get stabilized after the HOLD mode is released (see Figure 4).

Note: The traces to and from the components that are involved in oscillation should be kept as short as possible as the oscillation characteristics are affected by their trace pattern.

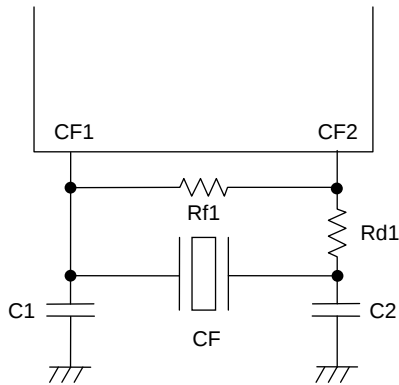


Figure 1 CF Oscillator Circuit

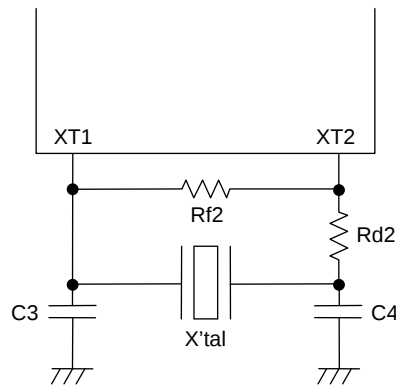


Figure 2 XT Oscillator Circuit

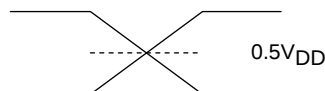
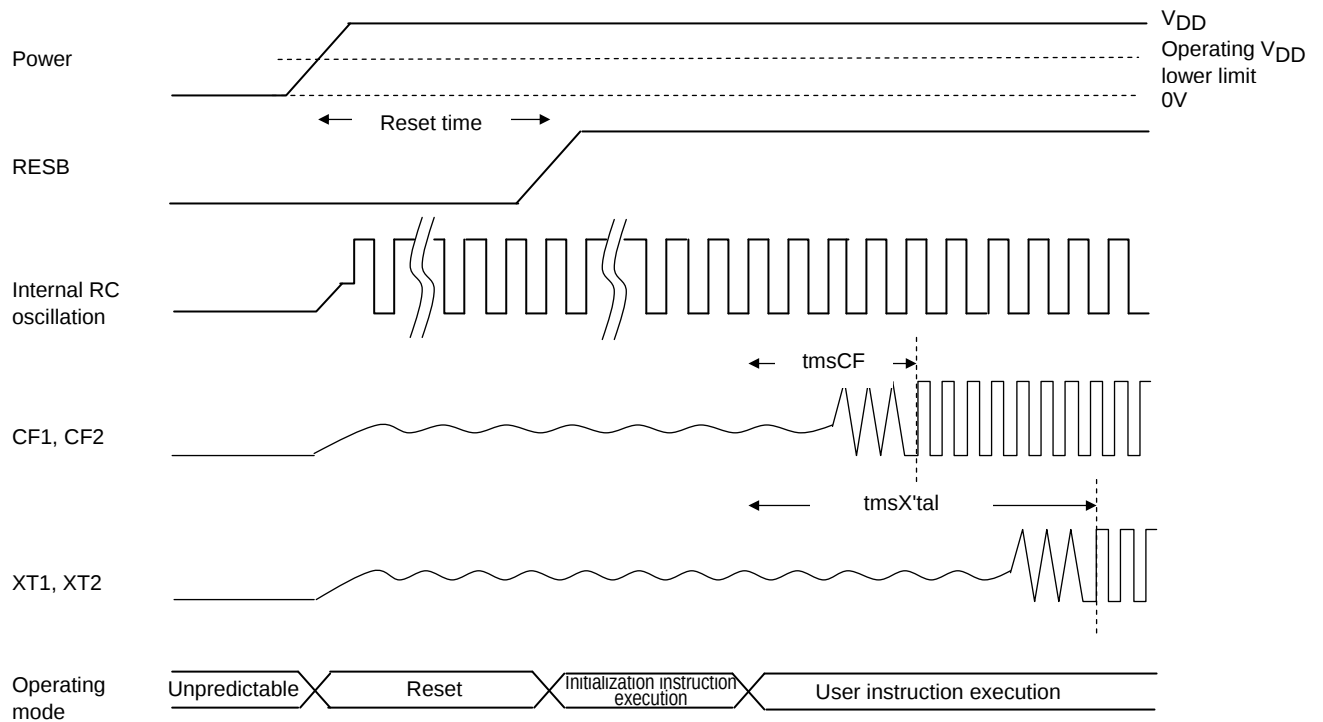
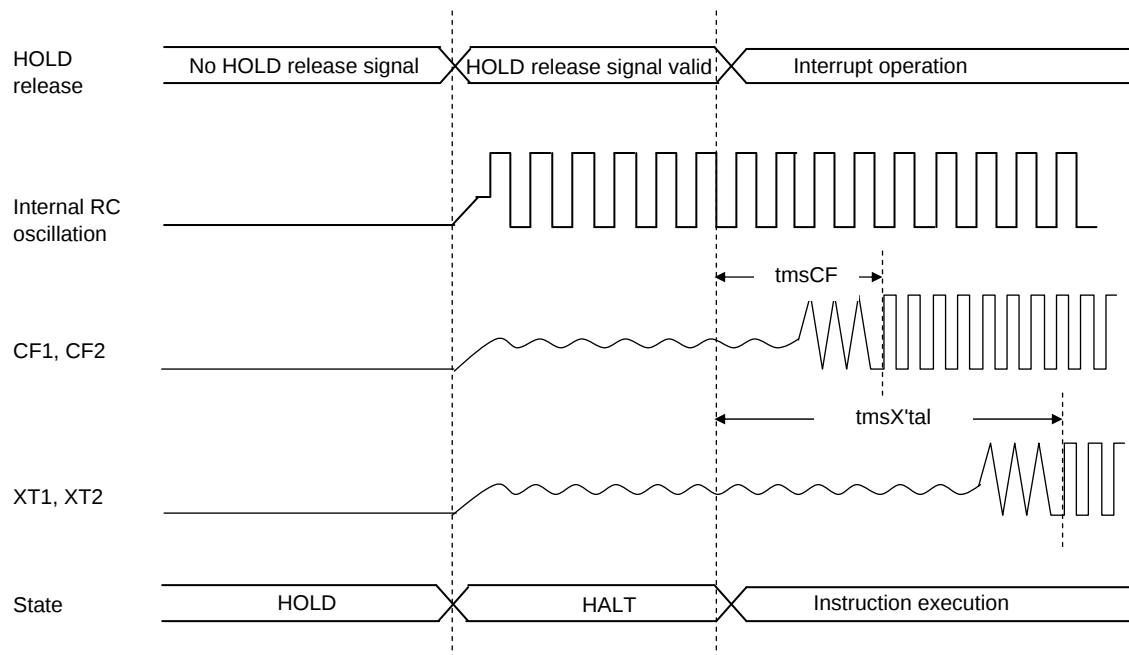


Figure 3 AC Timing Measurement Point

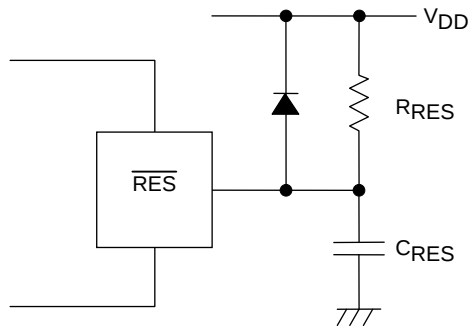


Reset Time and Oscillation Stabilization Time



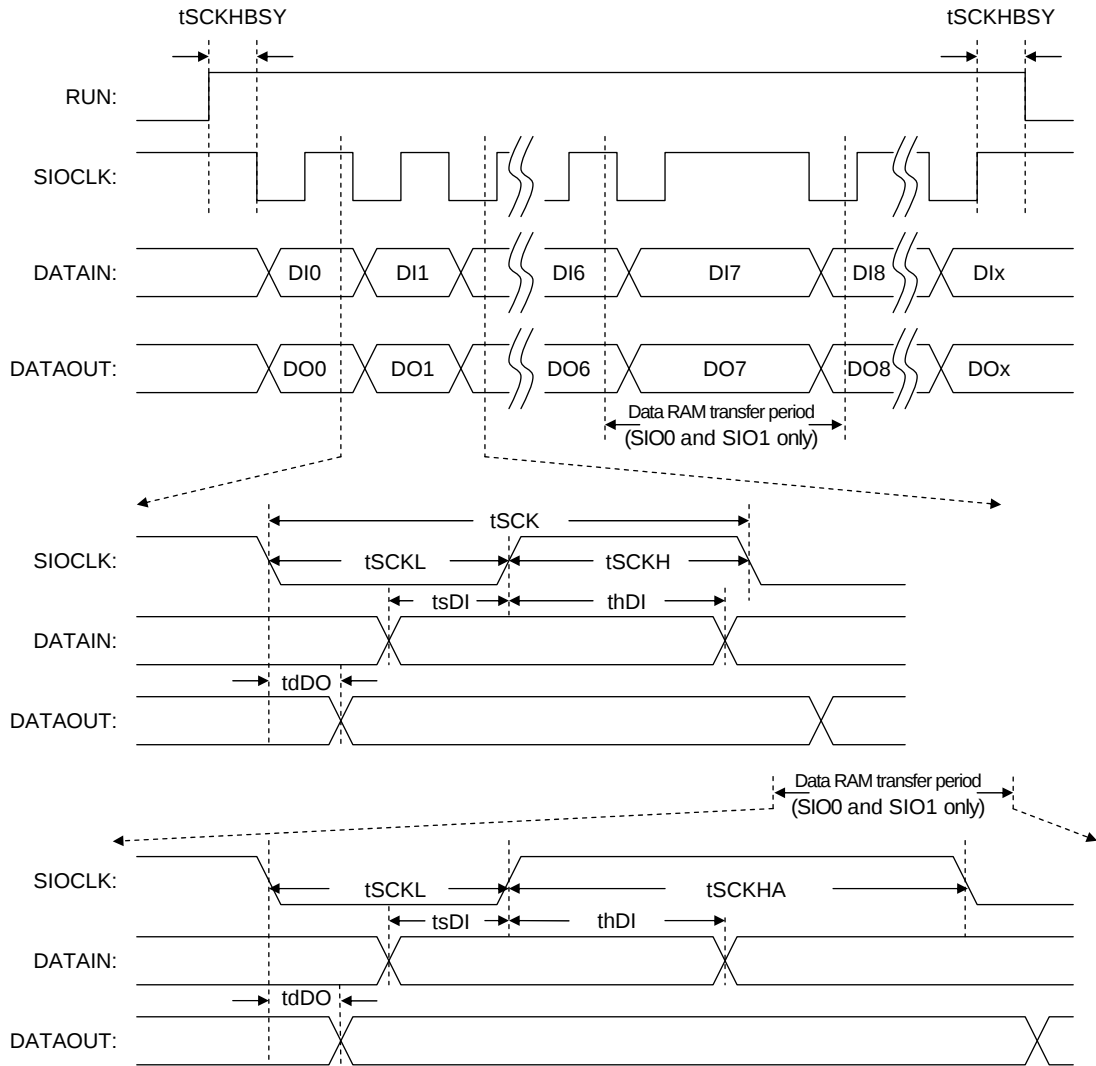
HOLD Release and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Time Timing Charts



Note:  
Reset signal must be present when power supply rises.  
Determine the value of  $C_{RES}$  and  $R_{RES}$  so that the reset signal is present for  $10\mu s$  after the supply voltage gets stabilized.

Figure 5 Reset Circuit



\*: \* Remarks: DIx and DOx denote the last bits communicated;  $x = 0$  to 32768

Figure 6 Serial I/O Waveforms

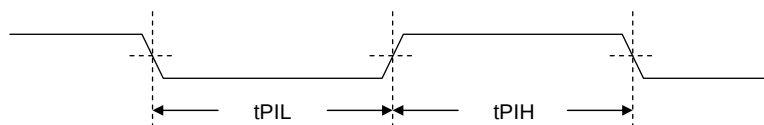
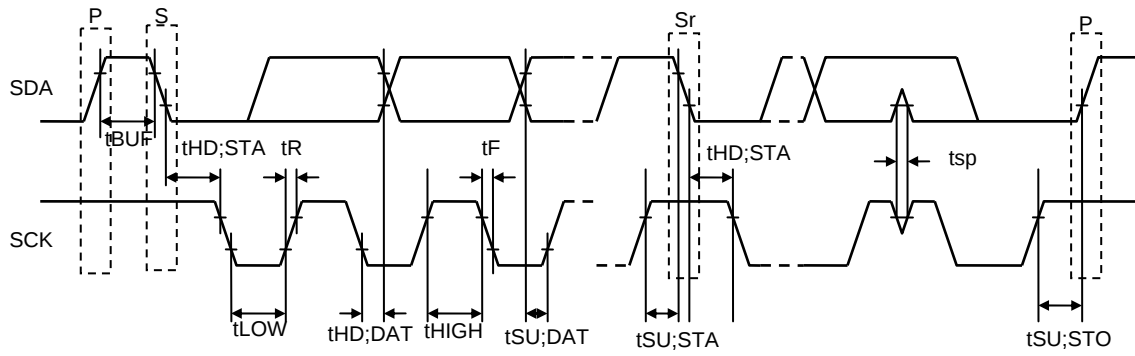


Figure 7 Pulse Input Timing Signal Waveform



S: Start condition  
P: Stop condition  
Sr: Restart condition

Figure 8 I<sup>2</sup>C Timing

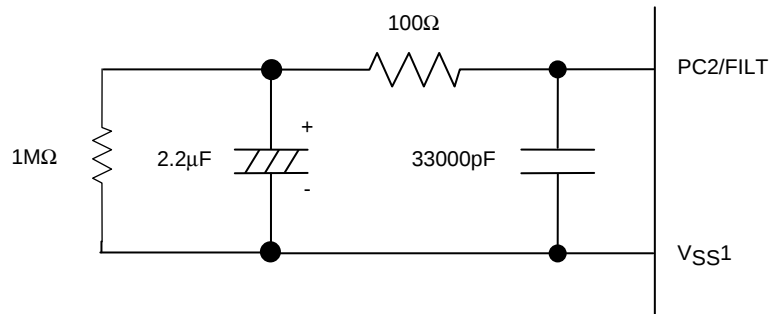


Figure 9 FILT recommended circuit

\*Take at least 50ms to oscillation to stabilize after PLL is started.

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