![Motorola] MOTOROLA

MC14013B

DUAL TYPE D FLIP-FLOP

The MC14013B dual type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Each flip-flop has independent Data, (D), Direct Set, (S), Direct Reset, (R), and Clock (C) inputs and complementary outputs (Q and $\overline{Q}$). These devices may be used as shift register elements or as type T flip-flops for counter and toggle applications.

- Static Operation
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Logic Edge-Clocked Flip-Flop Design —
  Logic state is retained indefinitely with clock level either high or low; information is transferred to the output only on the positive-going edge of the clock pulse
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4013B

CMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL TYPE D FLIP-FLOP
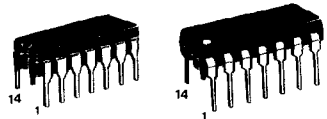
L SUFFIX	P SUFFIX
CERAMIC PACKAGE	PLASTIC PACKAGE
CASE 632	CASE 646

ORDERING INFORMATION

A Series: −55°C to +125°C
  MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
  MC14XXXBCP (Plastic Package)
  MC14XXXBCL (Ceramic Package)

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
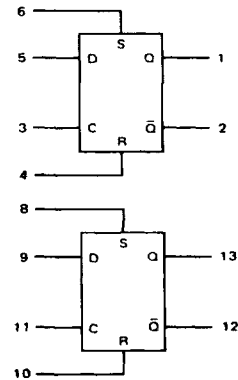Ceramic "L" Package: −12mW/°C from 100°C to 125°C

BLOCK DIAGRAM

V_{DD} = Pin 14
V_{SS} = Pin 7

TRUTH TABLE

INPUTS				OUTPUTS		
CLOCK†	DATA	RESET	SET	Q	$\overline{Q}$	
⤒	0	0	0	0	1	
⤒	1	0	0	1	0	
⤓	X	0	0	Q	$\overline{Q}$	No Change
X	X	1	0	0	1	
X	X	0	1	1	0	
X	X	1	1	1	1	

X = Don't Care
† = Level Change

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MC14013B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
$V_{in} = V_{DD}$ or 0		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
$V_{in} = 0$ or V_{DD}		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	—	3.5	2.75	—	3.5	—	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−3.0	—	−2.4	−4.2	—	−1.7	—	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	—	−0.51	−0.88	—	−0.36	—	
(V_{OH} = 9.5 Vdc)		10	−1.6	—	−1.3	−2.25	—	−0.9	—	
(V_{OH} = 13.5 Vdc)		15	−4.2	—	−3.1	−8.8	—	−2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−2.5	—	−2.1	−4.2	—	−1.7	—	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	—	−0.44	−0.88	—	−0.36	—	
(V_{OH} = 9.5 Vdc)		10	−1.3	—	−1.1	−2.25	—	−0.9	—	
(V_{OH} = 13.5 Vdc)		15	−3.6	—	−3.0	−8.8	—	−2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	—	0.44	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	—	1.1	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	3.6	—	3.0	8.8	—	2.4	—	
Input Current (AL Device)	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	—	±0.3	—	±0.00001	±0.3	—	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (AL Device)	I_{DD}	5.0	—	1.0	—	0.002	1.0	—	30	μAdc
(Per Package)		10	—	2.0	—	0.004	2.0	—	60	
		15	—	4.0	—	0.006	4.0	—	120	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	—	4.0	—	0.002	4.0	—	30	μAdc
(Per Package)		10	—	8.0	—	0.004	8.0	—	60	
		15	—	16	—	0.006	16	—	120	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	$I_T = (0.75~\mu A/kHz) f + I_{DD}$ $I_T = (1.5~\mu A/kHz) f + I_{DD}$ $I_T = (2.3~\mu A/kHz) f + I_{DD}$							μAdc

*T_{low} = −55°C for AL Device, −40°C for CL/CP Device
T_{high} = +125°C for AL Device, +85°C for CL/CP Device

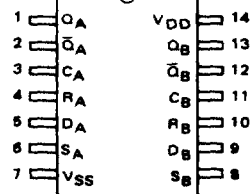#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance

**The formulas given are for the typical characteristics only at 25°C

†To calculate total supply current at loads other than 50 pF

$$I_T(C_L) = I_T(50~pF) + (C_L - 50) V f k$$

where I_T is in μA (per package), C_L in pF, V = ($V_{DD} - V_{SS}$) in volts
f in kHz is input frequency, and k = 0.002

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT

|		
1	Q_A	V_{DD} 14
2	$\bar{Q}_A$	Q_B 13
3	C_A	$\bar{Q}_B$ 12
4	R_A	C_B 11
5	D_A	R_B 10
6	S_A	D_B 9
7	V_{SS}	S_B 8

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH}, t_{PHL}					ns
Clock to Q, $\overline{Q}$						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns		5.0	–	175	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	75	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns		15	–	50	100	
Set to Q, $\overline{Q}$						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 90 ns		5.0	–	175	350	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 42 ns		10	–	75	150	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 25 ns		15	–	50	100	
Reset to Q, $\overline{Q}$						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 265 ns		5.0	–	350	450	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 67 ns		10	–	100	200	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 50 ns		15	–	75	150	
Setup Times**	t_{su}	5.0	40	20	–	ns
		10	20	10	–	
		15	15	7.5	–	
Hold Times**	t_h	5.0	40	20	–	ns
		10	20	10	–	
		15	15	7.5	–	
Clock Pulse Width	t_{WL}, t_{WH}	5.0	250	125	–	ns
		10	100	50	–	
		15	70	35	–	
Clock Pulse Frequency	f_{cl}	5.0	–	4.0	2.0	MHz
		10	–	10	5.0	
		15	–	14	7.0	
Clock Pulse Rise and Fall Time	t_{TLH}	5.0	–	–	15	μs
	t_{THL}	10	–	–	5.0	
		15	–	–	4.0	
Set and Reset Pulse Width	t_{WL}, t_{WH}	5.0	250	125	–	ns
		10	100	50	–	
		15	70	35	–	
Removal Times	t_{rem}					ns
Set		5	80	0	–	
		10	45	5	–	
		15	35	5	–	
Reset		5	50	–35	–	
		10	30	–10	–	
		15	25	–5	–	

*The formulas given are for the typical characteristics only at 25°C.

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intended as an indication of the IC's potential performance.

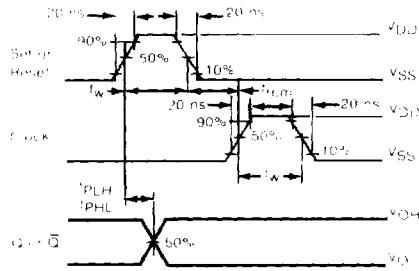**Data must be valid for 250 ns with a 5 V supply, 100 ns with 10 V, and
70 ns with 15 V.

LOGIC DIAGRAM
(1/2 of Device Shown)

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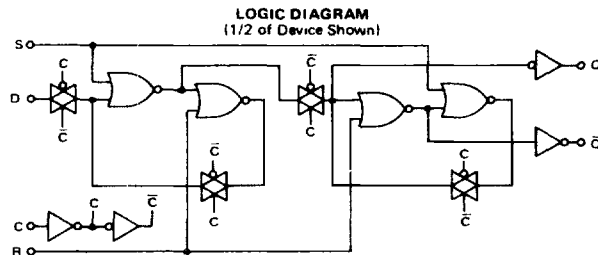
MC14013B

FIGURE 1 — DYNAMIC SIGNAL WAVEFORMS
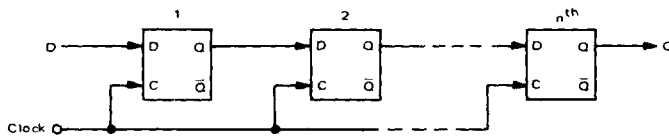(Data, Clock, and Output)
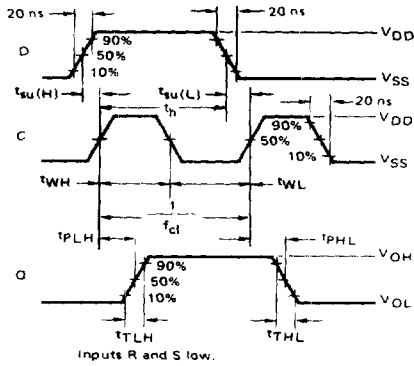
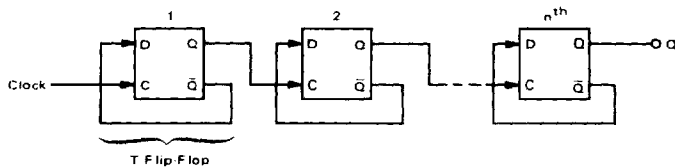### FIGURE 2 — DYNAMIC SIGNAL WAVEFORMS
(Set, Reset, Clock, and Output)

Inputs R and S low.

TYPICAL APPLICATIONS

n-STAGE SHIFT REGISTER

BINARY RIPPLE UP-COUNTER (Divide-by-2^n)

T Flip-Flop

MODIFIED RING COUNTER (Divide-by-(n + 1))

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