# SIEMENS

## TV-Stereo Sound

**TDA 6612-2**

Preliminary Data

**Bipolar IC**

### Features

The TDA 6612-2 represents a complete TV-stereo system controlled by the I²C Bus according to German TV-Stereo standard.

- All functions inclusive matrix adjustment are I²C Bus controlled
- Inputs for AM sound or NICAM
- SCART-interface
- Independent headphones
- Universal clock generation circuit build-in
- Clipping detector build-in
- Volume control
- High signal-to-noise ratio
- Extremely low total harmonic distortions
- High security for the detection of the identification signals because of the digital interference suppression and the very narrow bandwidth
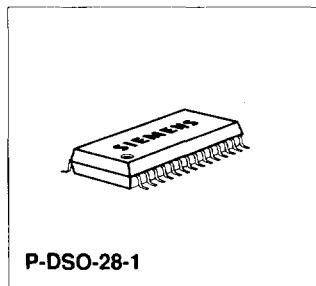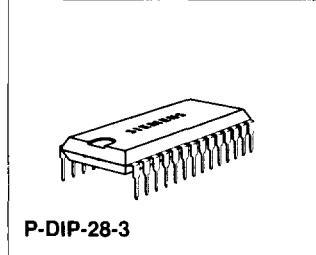
**P-DIP-28-3**

**P-DSO-28-1**

| Type | Ordering Code | Package |
|------|---------------|---------|
| TDA 6612-2 | Q67000-A5097 | P-DIP-28-3 |
| TDA 6612-2X | Q67000-A5194 | P-DSO-28-1 |

The IC is divided into three functional blocks

## 1 Stereo Sound Processing with High Performance (exceeds DIN 45500; suitable for NICAM and CD)

a) Matrix for G-standard with crosstalk compensation controlled via the I²C Bus

b) Additional single channel AF input (for e.g. AF signal according to L-standard)

c) Stereo SCART interface according to FTZ-official specification

d) Stereo loudspeaker signal section with Ch1/Ch2 switch, bass/treble control, quasi stereo/stereo base width expansion and separate loudspeaker volume control for left and right (balance)

e) Separate stereo head phone signal section with Ch1/Ch2 switch and volume control

## 2 TV-Sound Identification Signal Decoder Consisting of:

a) Active pilot signal filter

b) Phase independent rectifier with very narrow bandwidth for evaluation of the identification signal

c) Digital integrator to reduce interferences by noise

d) Multiplexer for cyclical switch over between "stereo" or "dual" evaluation

e) Reference signal generation with externally synchronized PLL

- synchronization with external H-sync pulse or 62.5-kHz clock
- build-in crystal oscillator and external 4-MHz crystal
- external 4-MHz (or 1-MHz) clock signal

## 3 Control Section for:

a) I²C Bus interface with listen/talk function

b) Control of the complete AF-sound signal detector

c) Read access to the clipping detector

d) Control of the identification signal decoder

e) Reading of the status of the identification signal decoder

f) Test modes

## Circuit Description

### Signal Section

The audio signal processing in the matrix and the switch-over for multi channel TV-sound signals according to the two carrier system used in Germany takes place in the matrix and switching sections. Crosstalk compensation is carried out in the sound 1 input stage. The crosstalk compensation range has an adjustment range of $\pm 3$ dB with a step width of 0.2 dB. In addition to the two inputs for the demodulated sound carrier a two channel SCART-input and an additional mono input (e.g. for demodulated L-standard sound) are provided. The two AF (pin 1 and pin 2) inputs can be by-passed internally in such a way that decoded stereo sound of other audio systems (NICAM) can be processed. The switching section includes also the SCART-output with the possibility to select the sound 1 or 2 during the "dual" mode. The Ch1/Ch2-switches for the loudspeaker and headphone outputs are independently switchable.

In the signal path for the volume control unit output there is the Ch1/Ch2-switch followed by two different volume control units. The first has a control range from 0 to $- 15$ dB with a step width of 1.25 dB. In conjunction with the main volume control after bass and treble control a high immunity against overdriving the output stage is reached. The first volume control is used as a "pre-stage" of the main volume control in conjuntion with the clipping detector. This section is followed by a switchable quasi stereo stage which provides a stereophonic audio effect with mono signals due to a 180˚ phase shift at medium frequencies (about 1 kHz) in one channel. The following bass control has a control range of +15/–12 dB with a step width of 3 dB. The cut-off frequency for each channel is set with an external capacitor. The implemented switchable circuit for stereo base width expansion provides a three dimensional aural reception. This is realized with a 50% frequency dependent crosstalk with opposite phase of the signal between both channels. The circuit operates with the same cut-off frequency as the bass control, but the function is widely independent. The treble control has a step width of 3 dB with an control range of +/–12 dB. The cut-off frequency of the treble control is derived from one capacitor for each channel. The loudspeaker signal path is terminated with the loudspeaker control, independently adjustable for left and right. With 57 steps of 1.25 dB the adjustment range is 70 dB, where step 57 activates the "MUTE" function. Functions such as "balance" or "loudness" are realized by software and adjustment of the appropriate tone and volume controls. In the volume control unit there is a clipping detector. The status of the clipping detector can be evaluated via the I²C Bus. Therefore it is possible to implement an automatic volume control using the clipping detector and software implemented into the controller.

After every evaluation the clipping bit is reset. Therefore after a read access to the clipping bit a new evaluation of the clipping detector status is possible.

The signal path for the headphones contains a volume control after the Ch1/Ch2-switch with a common adjustment for left and right. Thirty two steps of 2 dB give an adjustment range of 62 dB (31 x 2 dB = 62 dB, the 32nd step is MUTE).

### Identification Signal Decoder

The input of the identification signal decoder consists of an op-amp for the pilot signal with its side bands. An external LC-circuit is used. The signal is then passed to a phase independent active band-pass filter with a very narrow bandwidth (adjustable externally). This filter detects whether the lower side band of the pilot carrier, which is modulated with the identification signal, is present. The

center frequency of the filter is switched between "dual" and "stereo" by a multiplexer. The multiplexing frequency is adjustable by software. If a side band is detected, the multiplexer stops. The interferences on the first "detected" criterion are suppressed by a digital integrator with a following comparator and can be read out via I²C Bus (talk mode) as the "stereo" or "dual" mode. The control of the corresponding signal can be either directly internally or through the µC. All the necessary clock signal are derived from a fast setting PLL which is synchronized by a reference frequency. This reference frequency must be sufficiently close to the horizontal frequency, but a **rigid phase coupling is not required**. Therefore, alternatively the use of a crystal controlled 62.5-kHz frequency commonly found in PLL-tuning systems is possible. A further alternative for the clock signal generation is a build-in crystal oscillator with an external 4-MHz crystal or the use an external 1- or 4-MHz clock frequency.

## Control Section

All functions are controlled via an I²C Bus interface with "listen" / "talk" functions. The data bytes currently used are stored in a block of latches.

The telegram structure is formed in the following manner:

start condition - chip address - any number of bytes - stop condition

The following conditions apply to the data bytes:

Before the actual data byte (with the adjustment information), **always** an I²C Bus sub-address byte has to be transmitted. The I²C Bus interface however is interpreting this sub-address byte as a data byte.

Example: The headphone volume is to be increased in a number of steps.

| Right | Wrong |
|---|---|
| Start condition | Start condition |
| Chip address 84 (Hex) | Chip address 84 (Hex) |
| Sub-addr. vol. HP 03 (Hex) | Sub-addr. vol. HP 03 (Hex) |
| Vol. step 8 08 (Hex) | Vol. step 8 08 (Hex) |
| Sub-addr. vol. HP 03 (Hex) | Vol. step 9 09 (Hex) |
| Vol. step 9 09 (Hex) | Vol. step 10 0A (Hex) |
| Sub-addr. vol. HP 03 (Hex) | Stop condition |
| Vol. step 10 0A (Hex) | |
| Stop condition | |

Within a telegram (i.e. without a new start condition) any different sub-addresses can be accessed. The changeover between "listen" and "talk" access to the IC however must always occur using the following sequence: stop condition - start condition - chip address. Before each read access always a start condition and chip address (talk) must be transmitted. The data to be read out are then loaded into the I²C Bus interface and can be transferred to the µC.

## Chip Address

| MSB | • | • | • | • | • | • | LSB |
|-----|---|---|---|---|---|---|-----|
| 1 | 0 | 0 | 0 | 0 | 1 | 0 | R/W |

R/W = 0 → Read (Listen)
R/W = 1 → Write (Talk)

## Subaddress Bytes

|  | MSB • | • | • | • | • | • | LSB |
|--|-----|---|---|---|---|---|-----|
| Volume input control | X X X X X | 1 | 0 | 0 | | | |
| Volume of left speaker | X X X X X | 0 | 0 | 1 | | | |
| Volume of right speaker | X X X X X | 0 | 1 | 0 | | | |
| Volume of headphones | X X X X X | 0 | 1 | 1 | | | |
| Treble / bass | X X X X X | 1 | 0 | 1 | | | |
| Switch byte I | X X X X X | 1 | 1 | 1 | | | |
| Switch byte II | X X X X X | 0 | 0 | 0 | | | |
| Crosstalk adjustment | X X X X X | 1 | 1 | 0 | | | |

## Control Bytes
### a) Volume Input Control

|  | MSB | • | • | • | • | • | • | LSB |
|--|-----|---|---|---|---|---|---|-----|
| Maximum volume | Qu-H | Ch1/Ch2EN | Ch1/Ch2SC | 0 | 0 | 0 | 0 | MUTE III |
| Max − 1 | Qu-H | Ch1/Ch2EN | Ch1/Ch2SC | 0 | 0 | 0 | 1 | MUTE III |
| Min + 1 | Qu-H | Ch1/Ch2EN | Ch1/Ch2SC | 1 | 0 | 1 | 1 | MUTE III |
| Minimum volume | Qu-H | Ch1/Ch2EN | Ch1/Ch2SC | 1 | 1 | 0 | 0 | MUTE III |
| Power ON | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Qu-H = 0    PLL synchronization with H-pulse; power ON

Qu-H = 1    PLL synchronization with crystal oszillator,

additionally the bit "H-pulse" has to be set to "H" in switch byte II

| Ch1/Ch2en | Ch1/Ch2sc | SCART output pin 9 | SCART output pin 10 |
|---|---|---|---|
| 0 | 0 | sound 1 | sound 2 |
| 0 | 1 | sound 2 | sound 1 |
| 1 | 0 | sound 1 | sound 1 |
| 1 | 1 | sound 2 | sound 2 |

Ch1/Ch2en, Ch1/Ch2sc are only activated if the matrix is in the dual mode

(switch byte II: matrix 0 = 1 and matrix 1 = 0 or matrix 0 = 1 , matrix 1 = 1 and the identification decoder is in the mode "dual")

MUTE III = 0     SCART output are muted.

MUTE III = 1     SCART output ON; power ON

                    (will be overwritten by MUTE 1 = 0 equal to all audio outputs muted)

                    MUTE III is "or" wired with MUTE I.

## b) Volume of Left / Right Loudspeaker

| | MSB | • | • | • | • | • | • | LSB |
|---|---|---|---|---|---|---|---|---|
| Maximum volume | X | X | 1 | 1 | 1 | 1 | 1 | 1 |
| Max −1 | X | X | 1 | 1 | 1 | 1 | 1 | 0 |
| Max −15 | X | X | 1 | 1 | 0 | 0 | 0 | 0 |
| Max −55 | X | X | 0 | 0 | 1 | 0 | 0 | 0 |
| MUTE | X | X | 0 | 0 | 0 | 1 | 1 | 1 |
| MUTE | X | X | 0 | 0 | 0 | 0 | 0 | 0 |
| MUTE | X | X | 0 | 0 | 0 | X | X | X |
| Power ON | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

## c) Volume of Headphones

| | MSB | • | • | • | • | • | • | LSB |
|---|---|---|---|---|---|---|---|---|
| Maximum volume | T2 | T1 | T0 | 1 | 1 | 1 | 1 | 1 |
| Max −1 | T2 | T1 | T0 | 1 | 1 | 1 | 1 | 0 |
| Max −15 | T2 | T1 | T0 | 1 | 0 | 0 | 0 | 0 |
| Max −31 | T2 | T1 | T0 | 0 | 0 | 0 | 0 | 1 |
| MUTE | T2 | T1 | T0 | 0 | 0 | 0 | 0 | 0 |
| Power ON | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

T0, T2 are test bits; these must be set to 0 for normal operation

## d) Crosstalk Compensation Matrix (sound 1)

|                    | MSB | • | • | • | • | • | • | LSB |
|--------------------|-----|---|---|---|---|---|---|-----|
| Max. amplification | 0   | 0 | 0 | 1 | 1 | 1 | 1 | 1   |
| Max −1             | 0   | 0 | 0 | 1 | 1 | 1 | 1 | 0   |
| Gain 0 dB          | 0   | 0 | 0 | 1 | 0 | 0 | 0 | 0   |
| Min. gain          | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 1   |
| Min. gain          | 0   | 0 | 0 | 0 | 0 | 0 | 0 | X   |
| Power ON           | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 1   |

## e) Treble/Bass

|                       | MSB | • | • | • | • | • | • | LSB |
|-----------------------|-----|---|---|---|---|---|---|-----|
| Linear                | 1   | 0 | 0 | 0 | 1 | 0 | 0 | 0   |
| Max. treble, lin. bass| 1   | 1 | 0 | 0 | 1 | 0 | 0 | 0   |
| Max. treble, lin. bass| 1   | 1 | X | X | 1 | 0 | 0 | 0   |
| Min. treble, lin. bass| 0   | 1 | 0 | 0 | 1 | 0 | 0 | 0   |
| Min. treble, lin. bass| 0   | 0 | X | X | 1 | 0 | 0 | 0   |
| Lin. treble, max. bass| 1   | 0 | 0 | 0 | 1 | 1 | 0 | 1   |
| Lin. treble, max. bass| 1   | 0 | 0 | 0 | 1 | 1 | X | 1   |
| Lin. treble, max. bass| 1   | 0 | 0 | 0 | 1 | 1 | 1 | X   |
| Lin. treble, min. bass| 1   | 0 | 0 | 0 | 0 | 1 | 0 | 0   |
| Lin. treble, min. bass| 1   | 0 | 0 | 0 | 0 | 0 | X | X   |
| Max. treble, max. bass| 1   | 1 | X | X | 1 | 1 | X | 1   |
| Min. treble, min. bass| 0   | 0 | X | X | 0 | 0 | X | X   |
| Power ON              | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 1   |
|                       | MSB |   |   |   | LSB | MSB |   | LSB |
|                       | treble |  |  |  | treble | bass |  | bass |

## f) Switch Byte I

| MSB | • | • | • | • | • | • | LSB |
|-----|-----|-----|-----|-----|-----|-----|-----|
| MUTE I | MUTE II | CH1/CH2LS | CH1/CH2KH | Mono | SCART | SCART-D | AM |

MUTE I    = 0    All AF-outputs are muted (speakers, headphones, SCART); power ON

MUTE I    = 1    All AF-outputs ON

MUTE II    = 0    Loudspeaker outputs muted; power ON

MUTE II    = 1    Loudspeaker outputs ON

MUTE I and MUTE II are OR gated with respect to the loudspeaker outputs

MUTE I and MUTE III are OR gated with respect to the SCART output

| MUTE I | MUTE II | MUTE III | Loudspeaker output | Headphone output | SCART output |
|--------|---------|----------|--------------------|------------------|--------------|
| 0 | 0 | 0 | muted | muted | muted |
| 0 | 0 | 1 | muted | muted | muted |
| 0 | 1 | 0 | muted | muted | muted |
| 0 | 1 | 1 | muted | muted | muted |
| 1 | 0 | 0 | muted | ON | muted |
| 1 | 0 | 1 | muted | ON | ON |
| 1 | 1 | 0 | ON | ON | muted |
| 1 | 1 | 1 | ON | ON | ON |

| | | | |
|---|---|---|---|
| Ch1/Ch2LS | = | 0 | Sound 1 on the loudspeaker outputs; power ON |
| Ch1/Ch2LS | = | 1 | Sound 2 on the loudspeaker outputs |
| Ch1/Ch2KH | = | 0 | Sound 1 on the headphone outputs; power ON |
| Ch1/Ch2KH | = | 1 | Sound 2 on the headphone outputs |

Ch1/Ch2LS and Ch1/Ch2KH are only effective if the matrix is set to the position "dual sound".

| | | | |
|---|---|---|---|
| Mono | = | 0 | identification signal decoder is set to the position mono and held; power ON |
| Mono | = | 1 | normal operation if ID-signal decoder |
| SCART | = | 0 | normal TV-operation; power ON |
| SCART | = | 1 | SCART playback; connection of SCART inputs - AF - outputs SCART = 1 has priority over AM = 1 (loudspeaker and headphones) |
| SCART-D | = | 0 | SCART-playback stereo (mono); power ON |
| SCART-D | = | 1 | Enable for the Ch1/Ch2 switch during SCART playback. (only effective when SCART = 1) |
| AM | = | 0 | Normal operation (G-standard) |
| AM | = | 1 | AM AF-input is activated; power ON AM = 1 has priority over bypass = 1 |

Qu-H, Ch1/Ch2EN, Ch1/Ch2SC MUTE III see chapter Control Bytes a).

**g) Switch Byte II**

| MSB | • | • | • | • | • | • | LSB |
|-----|-----|-----|-----|-----|-----|-----|-----|
| MPX0 | MPX1 | Quasi-st | BS | H-pulse | Matrix 0 | Matrix 1 | Bypass |

| MPX0 | MPX1 | MPX-period | | recommended $C_{25, 26}$ | permissible crystal tolerance |
|------|------|------------|---|---------|---------|
| 0 | 0 | 2 s | power ON | 1 μF | |
| 0 | 1 | 4 s | | 2.2 μF | |
| 1 | 0 | 8 s | | 4.7 μF | |

special for crystal operation recommended adjustments:

| 0 | 0 | 2 s | 470 nF | ± 40 ppm |
|---|---|-----|--------|----------|
| 0 | 1 | 4 s | 330 nF | ± 70 ppm |

MPX period = 2 s signifies: ID-signal decoder searches 1 second dual and 1 second stereo.
It is inprinciple permitted to make with given $C_{25, 26}$ the MPX-period higher than indicated, but not lower.

| Quasi stereo | = | 0 | Quasi stereo OFF; power ON |
|---|---|---|---|
| Quasi stereo | = | 1 | Quasi stereo ON |
| Bb | = | 0 | Stereo base width expansion OFF; power ON |
| Bb | = | 1 | Stereo base width expansion ON; |

| H-pulse | = | 0 | ID-signal decoder synchronization with $f_H$ = 15.625 kHz; power ON |
|---|---|---|---|
| H-pulse | = | 1 | ID-synchronization with $4 \times f_H$ (has to be set to 1 during operation with crystal or 4-MHz reference frequency) |

| Matrix 0 | Matrix1 | Matrix status | |
|---|---|---|---|
| 0 | 0 | mono | power ON |
| 0 | 1 | stereo | |
| 1 | 0 | dual | |
| 1 | 1 | automatic according to ID-signal decoder | |

| Bypass = | 0 | Normal operations (G-standard) |
|---|---|---|
| Bypass = | 1 | Matrix is bridge so that left/right signals can be fed; power ON (AM = 1 has priority over bypass = 1) |

**Priority List of Setting Bits**

1. MUTE I

2. MUTE II (only with regard to the loudspeaker output)

3. SCART

4. AM

5. Bypass

6. Matrix 0, 1

**h) Talk Mode**

| MS | • | • | • | • | • | • | LSB |
|---|---|---|---|---|---|---|---|
| St | D | T3 | T4 | T5 | CL | X | X |
| 0 | 0 | decoder detects mono | | | | | |
| 1 | 0 | decoder detects stereo | | | | | |
| 0 | 1 | decoder detects dual | | | | | |
| 1 | 1 | internally inhibited | | | | | |
| CL = 1 | The signal path for the loudspeaker reached the clipping level (The bit CL is automatical reset) | | | | | | |

T3 - T5 are test bits

## Pin Functions

| Pin No. | Function |
|---|---|
| 1 | AF-input mono, left, sound 1 (may be balanced) |
| 2 | Bias for AF-operating point |
| 3 | AF-input right, sound 2 |
| 4 | 54-kHz input |
| 5 | 54-kHz filter |
| 6 | AF-input (L-standard) |
| 7 | AF-input SCART left (sound 1) |
| 8 | AF-input SCART right (sound 2) |
| 9 | AF-output SCART (mono, sound 1, left) |
| 10 | AF-output SCART (mono, sound 2, right) |
| 11 | Phase shifter quasi stereo |
| 12 | Phase shifter quasi stereo |
| 13 | Cut-off frequency bass (base width) left |
| 14 | Cut-off frequency bass (base width) right |
| 15 | AF-output, loudspeaker right |
| 16 | AF-output, loudspeaker left |
| 17 | Cut-off frequency treble left |
| 18 | Cut-off frequency treble right |
| 19 | AF-output, headphones right |
| 20 | AF-output, headphones left |
| 21 | $+ V_S$ (supply voltage) |
| 22 | I²C Bus SCL |
| 23 | I²C Bus SDA |
| 24 | Input H-pulse (4 x H-pulse), crystal oscillator |
| 25 | Filter ID-signal decoder |
| 26 | Filter ID-signal decoder |
| 27 | PLL-filter ID-signal decoder |
| 28 | Ground |

UEB03400

**Block diagram labels (rotated):**

- 15 — AF Loudspeakers Right — Volume Main Control
- 16 — AF Loudspeakers Left — Basewidth
- Base
- 14 — Cut-Off Frequency Base
- 13 — Cut-Off Frequency Base
- 17 — Cut-Off Frequency Treble — Treble
- Clipping Detector
- 18 — Cut-Off Frequency Treble — Quasi-Stereo
- 12 — Phase Rotation Quasi-Stereo
- 11 — Phase Rotation Quasi-Stereo
- 19 — AF Headphones Right — Volume Headphones
- 20 — AF Headphones Left — Volume Precontrol
- 10 — SCART Output Mono Right
- 9 — SCART Output Mono Left
- 21 — $V_S$ — Reference Voltage
- Switch
- 8 — SCART Input Right Sound 2
- 22 — $I^2C$ Bus SCL — $I^2C$ Bus
- 7 — SCART Input Left Sound 1
- 23 — $I^2C$ Bus SDA
- 6 — AF Input L Standard
- H-Pulse (4× H-Pulse 1MHz, 4MHz)
- 24 — 54-kHz Filter
- 5 — 54-kHz Filter
- 4-MHz Crystal (Alternatively)
- Bandwidth ID-Signal Decoder
- 25 — Filter — Multiplexer
- 4 — AF Input Sound 2, Right
- 26 — 54-kHz Filter
- 3 — AF Input Sound 2, Right
- Loop Filter PLL
- 27 — Integrator — Matrix
- 2 — Bias AF Unit
- 28 — PLL — Cross. Adj.
- 1 — AF Input Mono, Sound 1 (L+R)/2, Left

**Block Diagram**

**PLL Filter ID-Signal Decoder (Pin 27)**



**Filter ID-Signal Decoder (Pin 25/26)**

UES03404

**H-Pulse/Crystal Oscillator (Pin 24)**



UES05876

**I²C Bus SDA (Pin 23)**

UES05877

**I²C Bus SCL (Pin 22)**



50 Ω  19/20
      15/16
       9/10

UES05878
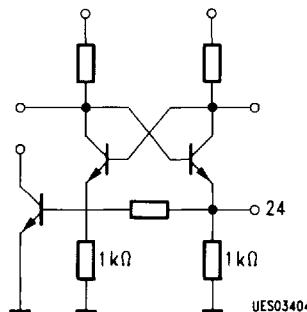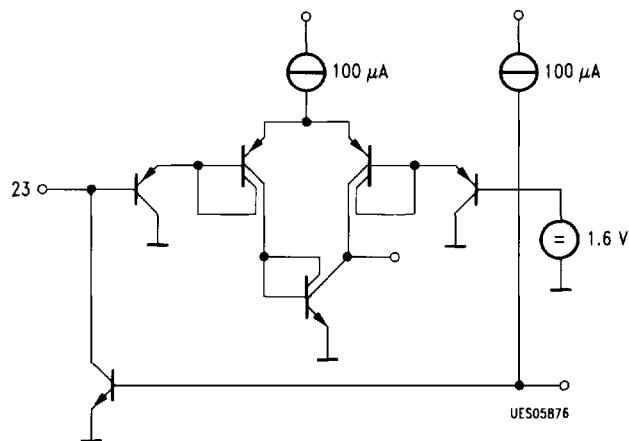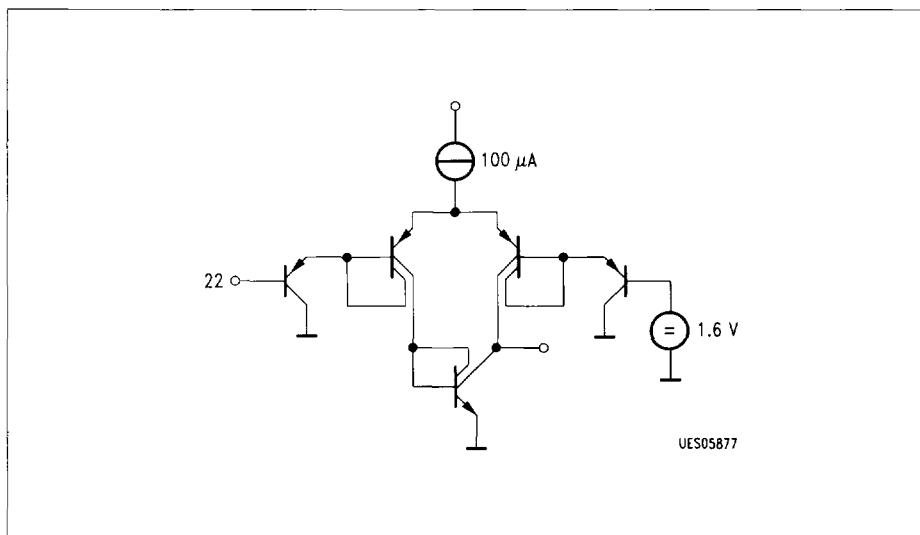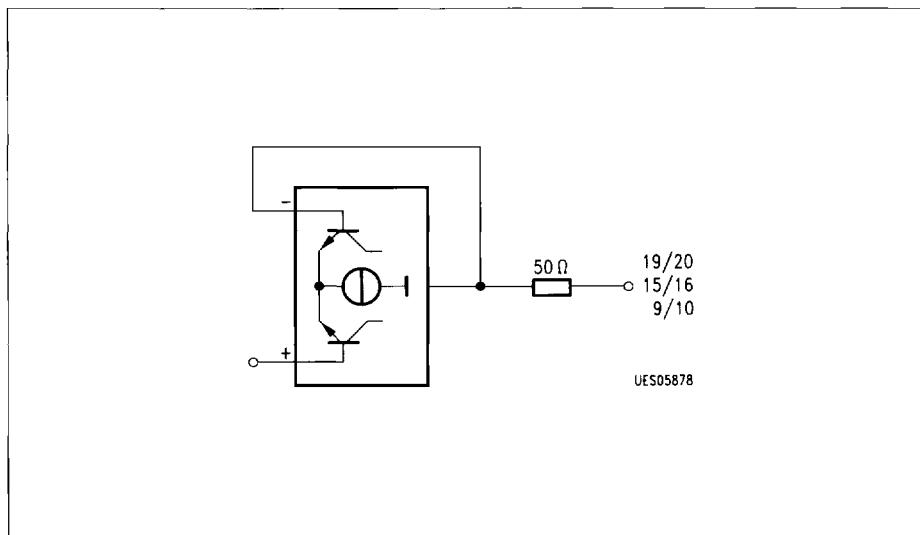
**AF-Outputs Headphones (Pin 19/20)**
**Loudspeaker (Pin 15/16)**
**SCART (Pin 9/10)**
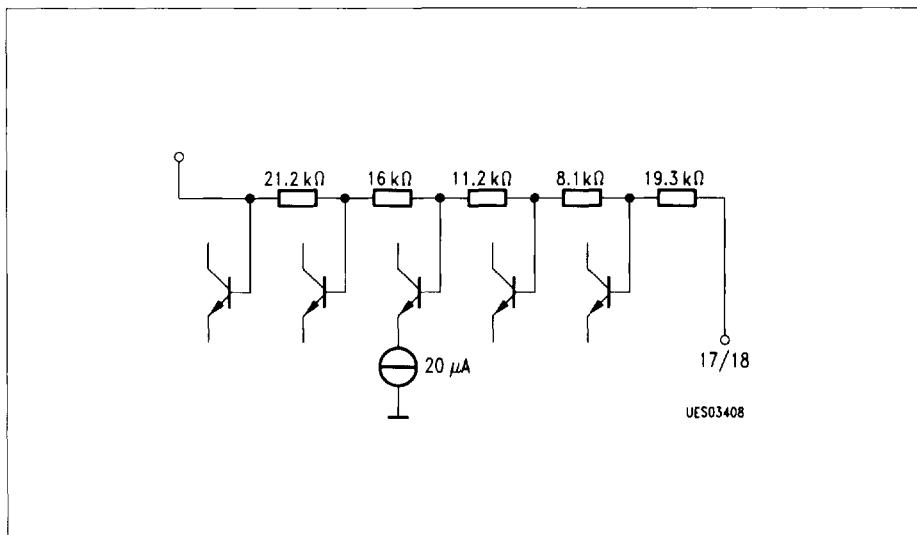
**Cut-Off Frequency Treble (Pin 17/18)**
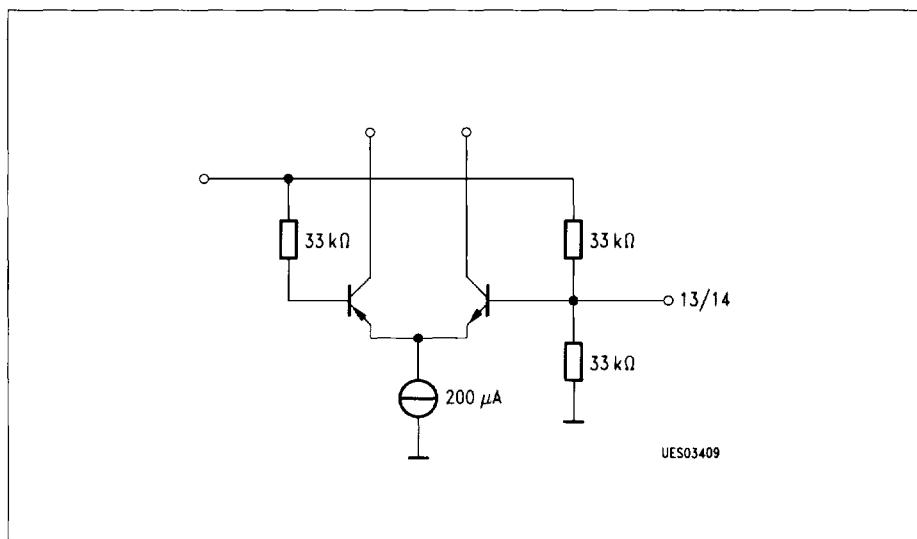


**Cut-Off Frequency Bass (Pin 13/14)**

UES03410
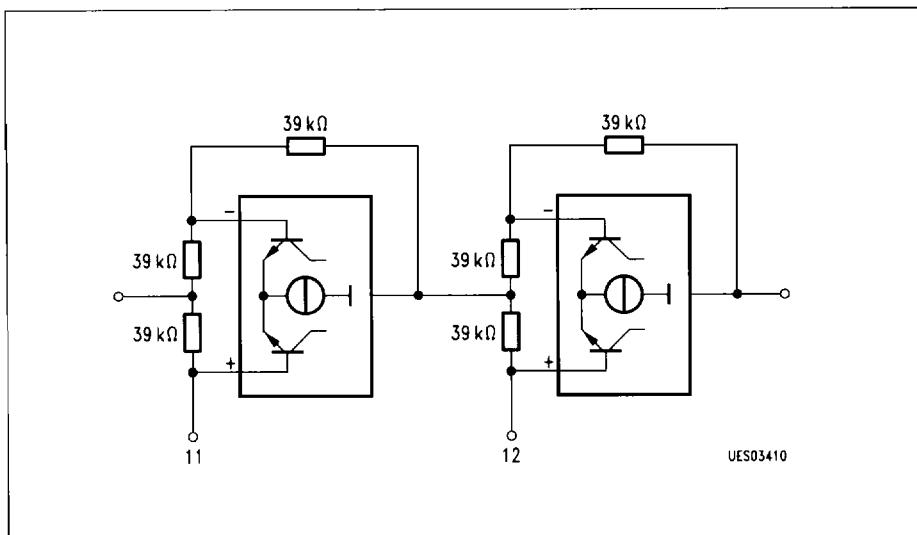
**Phase Advancer Quasi Stereo (Pin 11/12)**
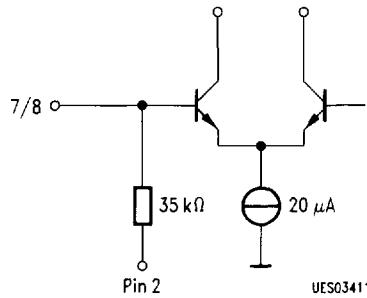
**AF-Inputs SCART (Pin 7/8)**
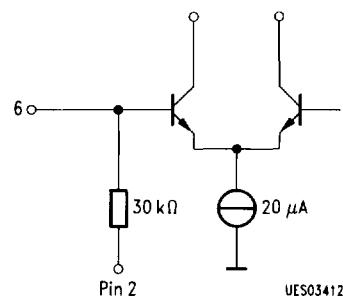


**AF-Input AM (Pin 6)**
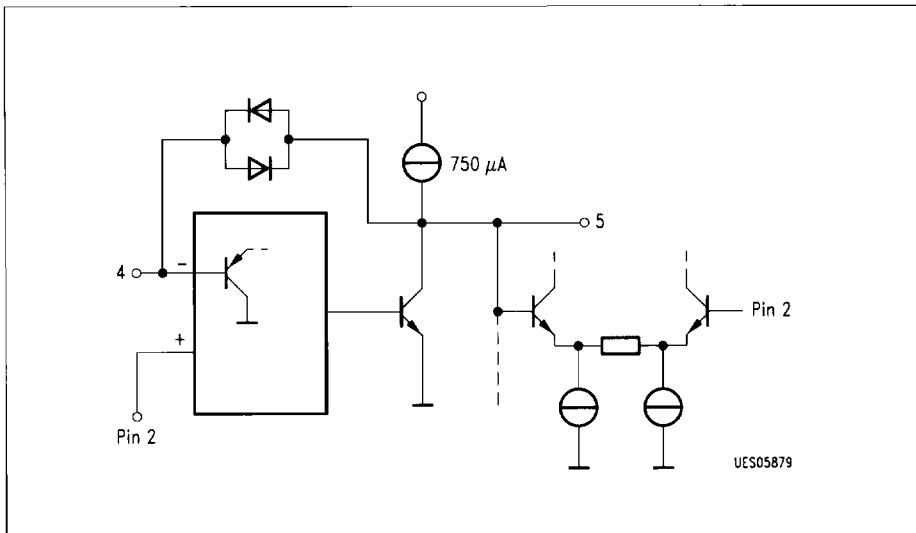
**54-kHz Filter (Pin 4/5)**
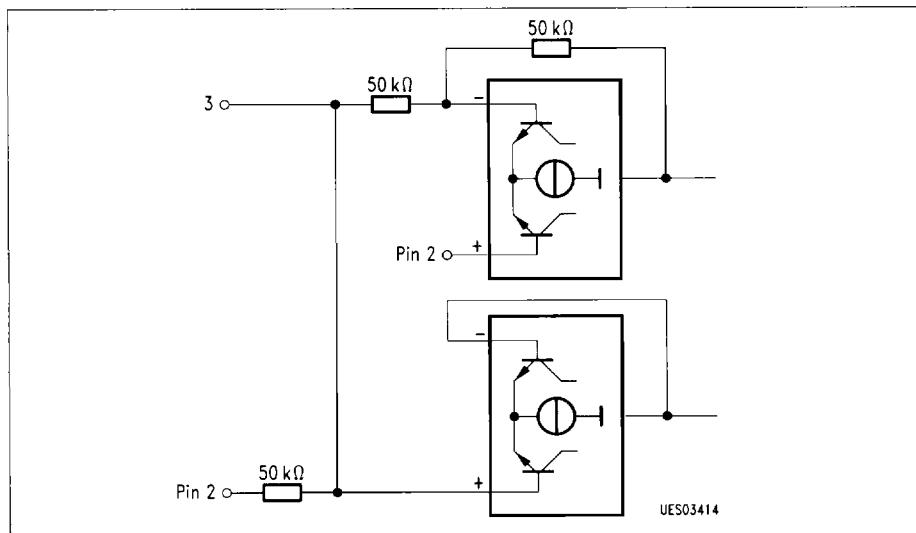


**AF-Input (Pin 3)**
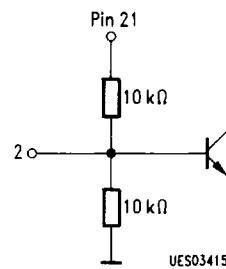
**Input for AF-Unit Bias Blocking Capacitor (Pin 2)**
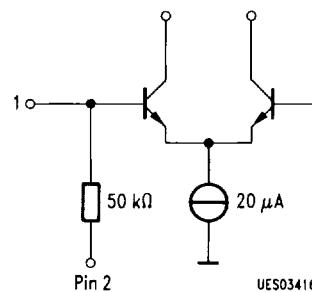


**AF-Input (Pin 1)**

## Absolute Maximum Ratings

$T_A = 0$ to 70 °C; all voltages relatives to $V_{ss}$

| Parameter | Symbol | Limit Values | | Unit | Remarks |
|---|---|---|---|---|---|
| | | min. | max. | | |
| Supply voltage | $V_{21}$ | 0 | 14 | V | |
| Max. DC-voltage | $V_1$ | 0 | $V_{21}$ | V | |
| Max. DC-voltage | $V_2$ | 0 | $V_{21}$ | V | |
| Max. DC-voltage | $V_3$ | 0 | $V_{21}$ | V | |
| Max. DC-voltage | $V_4$ | 0 | $V_{21}$ | V | |
| Max. DC-voltage | $V_6$ | 0 | $V_{21}$ | V | |
| Max. DC-voltage | $V_7$ | 0 | $V_{21}$ | V | |
| Max. DC-voltage | $V_8$ | 0 | $V_{21}$ | V | |
| Max. DC-voltage | $V_{11}$ | 0 | $V_{21}$ | V | |
| Max. DC-voltage | $V_{12}$ | 0 | $V_{21}$ | V | |
| Max. DC-voltage | $V_{13}$ | 0 | $V_{21}$ | V | |
| Max. DC-voltage | $V_{14}$ | 0 | $V_{21}$ | V | |
| Max. DC-voltage | $V_{17}$ | 0 | $V_{21}$ | V | |
| Max. DC-voltage | $V_{18}$ | 0 | $V_{21}$ | V | |
| Max. DC-voltage | $V_{22}$ | 0 | $V_{21}$ | V | |
| Max. DC-voltage | $V_{23}$ | 0 | $V_{21}$ | V | |
| Max. DC-voltage | $V_{24}$ | 0 | $V_{21}$ | V | |
| Max. DC-voltage | $V_{25}$ | 0 | $V_{21}$ | V | |
| Max. DC-voltage | $V_{26}$ | 0 | $V_{21}$ | V | |
| Max. DC-current | $I_5$ | 0 | 2 | mA | |
| Max. DC-current | $I_9$ | 0 | 2 | mA | |
| Max. DC-current | $I_{10}$ | 0 | 2 | mA | |
| Max. DC-current | $I_{15}$ | 0 | 2 | mA | |
| Max. DC-current | $I_{16}$ | 0 | 2 | mA | |
| Max. DC-current | $I_{19}$ | 0 | 2 | mA | |
| Max. DC-current | $I_{20}$ | 0 | 2 | mA | |
| Max. DC-current | $I_{27}$ | 0 | 1 | mA | |

**Absolute Maximum Ratings** (cont'd)

| Parameter | Symbol | Limit Values | | Unit | Remarks |
|---|---|---|---|---|---|
| | | min. | max. | | |
| ESD-voltage | $V_{ESD}$ | − 2 | 2 | kV | HBM ($R$ = 1.5 k$\Omega$, $C$ = 100 pF) |
| ESD-voltage | $V_{ESD7,8,9,10}$ | − 6 | 6 | kV | HBM ($R$ = 1.5 k$\Omega$, $C$ = 100 pF) |
| Junction temperature | $T_j$ | | 150 | °C | |
| Storage temperature | $T_{stg}$ | − 40 | 125 | °C | |
| Thermal resistance system ambient | $R_{th\,SA}$ | | 53 | K/W | |

**Operating Range**

| Parameter | Symbol | min. | max. | Unit | Remarks |
|---|---|---|---|---|---|
| Supply voltage | $V_6$ | 10 | 13.2 | V | |
| Ambiente temperature | $T_A$ | 0 | 70 | °C | |
| Input frequency range | $f_I$ | 0.01 | 20 | kHz | |

**Characteristics**

$V_S$ = 12 V; $T_A$ = 25 °C, audio reference level 0 dB–250 mVrms, if not differently defined.

I²C Bus preset: start - 84 - 01,3F - 0 2,3F - 04,00 - 0 3,1F - 0 5,88 - 0 6,10 - 07,C8 - 00,01 - stop

Chip address - Vol $_{LSl}$ 63 - Vol $_{LSr}$ 63 - Vol $_{VLs}$ - Vol $_{HP}$ 31 - Sound lin Adjust 0dB - MUTE I, MUTE II, Mono - Bypass

The basic setting for each point in the specification is always preset; only settings which deviate from this are given in the test conditions. Details in *italics* only provide explanation of the hexadecimal codes. If switch byte are mentioned only the bit status and activated features are indicated.

| Parameter | Symbol | Limit Values | | | Unit | Test Condition (in accordance with test circuit 1) |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Current consumption | $I_{21}$ | | 58. | 80 | mA | |
| **Signal Section** | | | | | | |
| Max. gain | $V_{16-1}$ | – 2 | 0 | 2 | dB | |
| Max. gain | $V_{15-3}$ | – 2 | 0 | 2 | dB | |
| Max. gain | $V_{20-1}$ | – 2 | 0 | 2 | dB | |
| Max. gain | $V_{19-3}$ | – 2 | 0 | 2 | dB | |
| Max. gain | $V_{16-3}$ | – 2 | 0 | 2 | dB | 00,02; $V_1$ = 01 Matrix: Stereo |
| Max. gain | $V_{15-3}$ | – 2 | 0 | 2 | dB | 00,02; $V_1$ = 01 Matrix: Stereo |
| Max. gain | $V_{20-3}$ | – 2 | 0 | 2 | dB | 00,02; $V_1$ = 0 Matrix: Stereo |
| Max. gain | $V_{19-3}$ | – 2 | 0 | 2 | dB | 00,02; $V_1$ = 0 Matrix: Stereo |
| Max. gain | $V_{16-1}$ | 4 | 6 | 8 | dB | 00,02; $V_3$ = 0 Matrix: Stereo |
| Max. gain | $V_{20-1}$ | 4 | 6 | 8 | dB | 00,02; $V_3$ = 0 Matrix: Stereo |
| Max. gain | $V_{16-7}$ | – 2 | 0 | 2 | dB | 07,CC, SCART |
| Max. gain | $V_{15-8}$ | – 2 | 0 | 2 | dB | 07,CC, SCART |
| Max. gain | $V_{20-7}$ | – 2 | 0 | 2 | dB | 07,CC, SCART |
| Max. gain | $V_{19-8}$ | – 2 | 0 | 2 | dB | 07,CC, SCART |
| Max. gain | $V_{16-6}$ | – 2 | 0 | 2 | dB | 07,C9, AM |
| Max. gain | $V_{15-6}$ | – 2 | 0 | 2 | dB | 07,C9, AM |
| Max. gain | $V_{20-6}$ | – 2 | 0 | 2 | dB | 07,C9, AM |
| Max. gain | $V_{19-6}$ | – 2 | 0 | 2 | dB | 07,C9, AM |

**Characteristics** (cont'd)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Gain | $V_{9\text{-}1}$ | $-2$ | 0 | 2 | dB | |
| Gain | $V_{10\text{-}3}$ | $-2$ | 0 | 2 | dB | |
| Gain | $V_{9\text{-}3}$ | $-2$ | 0 | 2 | dB | |
| Gain | $V_{10\text{-}3}$ | $-2$ | 0 | 2 | dB | 00,02; $V_1 = 0$ <br> *Matrix: Stereo* |
| Gain | $V_{9\text{-}1}$ | 4 | 6 | 8 | dB | 00,02; $V_1 = 0$ <br> *Matrix: Stereo* |
| Gain | $V_{10\text{-}6}$ | $-2$ | 0 | 2 | dB | 00,02; $V_1 = 0$ <br> *Matrix: Stereo* |
| Gain | $V_{9\text{-}6}$ | $-2$ | 0 | 2 | dB | 07,C9, *AM* |
| Min. gain <br> Main control | $V_{16\text{-}1}$ | | $-70$ | $-65$ | dB | 01,08-02,08 <br> *Vol $_{LSi}$ 8 – Vol $_{LSr}$ 8* |
| Min. gain <br> Main control | $V_{15\text{-}3}$ | | $-70$ | $-65$ | dB | 01,08-02,08 <br> *Vol $_{LSi}$ 8 – Vol $_{LSr}$ 8* |
| Min. gain <br> 1st. control | $V_{16\text{-}1}$ | $-17$ | $-15$ | $-13$ | dB | 04,18 <br> *Vol $_{VLS}$ 24* |
| Min. gain <br> 1st. control | $V_{15\text{-}3}$ | $-17$ | $-15$ | $-13$ | dB | 04,18 <br> *Vol $_{VLS}$ 24* |
| Min. gain | $V_{20\text{-}1}$ | | $-62$ | $-57$ | dB | 03,01, *Vol $_{HP}$ 1* |
| Min. gain | $V_{19\text{-}3}$ | | $-62$ | $-57$ | dB | 03,01, *Vol $_{HP}$ 1* |

### Characteristics (cont'd)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Analogous values are valid for feed in at the pins 6, 7 and 8 | | | | | | |
| Channel tracking error | $\Delta V_{15\text{-}16}$ | | | ± 2 | dB | 01,3F to 01,24<br>02,3F to 02,24<br>$Vol_{LSl}\ 63\text{-}36 - Vol_{LSr}\ 63\text{-}36$ |
| Channel tracking error | $\Delta V_{19\text{-}26}$ | | | ± 2 | dB | 03,1F to 03,13<br>$Vol_{HP}\ 31\text{-}19$ |
| Step width Vol $_{15}$ | $\Delta V_{15}$ | 0 | 1.25 | 2.5 | dB | 01,X-01,(X ± 1)<br>$Vol_{LSl}\ X - Vol_{LSl}\ (X \pm 1)$ |
| Step width Vol $_{16}$ | $\Delta V_{16}$ | 0 | 1.25 | 2.5 | dB | 02,X-02,(X ± 1)<br>$Vol_{LSr}\ X - Vol_{LSr}\ (X \pm 1)$ |
| Step width Vol $_{15}$ | $\Delta V_{15}$ | 0 | 1.25 | 2.5 | dB | 04,X-04,(X ± 1)<br>$Vol_{VLS}\ X - Vol_{VLS}\ (X \pm 1)$ |
| Step width Vol $_{16}$ | $\Delta V_{16}$ | 0 | 1.25 | 2.5 | dB | 04,X-04,(X ± 1)<br>$Vol_{VLS}\ X - Vol_{VLS}\ (X \pm 1)$ |
| Step width Vol $_{19}$ | $\Delta V_{19}$ | 0 | 2 | 4 | dB | 03,X-03,(X ± 1)<br>$Vol_{HP}\ X - Vol_{HP}\ (X \pm 1)$ |
| Step width Vol $_{20}$ | $\Delta V_{20}$ | 0 | 2 | 4 | dB | 03,X-03,(X ± 1)<br>$Vol_{HP}\ X - Vol_{HP}\ (X \pm 1)$ |
| Matrix adjustment | $V_{16\text{-}1}$ | 2.5 | 3 | 3.5 | dB | 06,1F, *Adjust. max* |
| Matrix adjustment | $V_{20\text{-}1}$ | 2.5 | 3 | 3.5 | dB | 06,1F, *Adjust. max* |
| Matrix adjustment | $V_{9\text{-}1}$ | 2.5 | 3 | 3.5 | dB | 06,1F, *Adjust. max* |
| Matrix adjustment | $V_{16\text{-}1}$ | – 3.5 | – 3 | – 2.5 | dB | 06,01, *Adjust. min* |
| Matrix adjustment | $V_{20\text{-}1}$ | – 3.5 | – 3 | – 2.5 | dB | 06,01, *Adjust. min* |
| Matrix adjustment | $V_{9\text{-}1}$ | – 3.5 | – 3 | – 2.5 | dB | 06,1F, *Adjust. max* |
| Adjust. step width | $\Delta V_{16}$ | 0.1 | 0.2 | 0.3 | dB | 06,X-06,(X ± 1)<br>*Adjust. X – adjust. (X ± 1)* |

**Characteristics** (cont'd)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Adjust. step width | $\Delta V_{20}$ | 0.1 | 0.2 | 0.3 | dB | 06,X-06,(X ± 1) _Adjust. X – adjust. (X ± 1)_ |
| Adjust. step width | $\Delta V_9$ | 0.1 | 0.2 | 0.3 | dB | 06,X-06,(X ± 1) _Adjust. X – adjust. (X ± 1)_ |
| Bass boost | $V_{16\text{-}1}$ | 13 | 15 | | dB | 05,8 F; $f_\mathrm{i}$ = 40 Hz _Bass max, treble lin._ |
| Bass boost | $V_{15\text{-}3}$ | 13 | 15 | | dB | 05,8 F; $f_\mathrm{i}$ = 40 Hz _Bass max, treble lin._ |
| Bass cut | $V_{16\text{-}1}$ | | – 12 | | dB | 05,8 F; $f_\mathrm{i}$ = 40 Hz _Bass max, treble lin._ |
| Bass cut | $V_{15\text{-}3}$ | | – 12 | | dB | 05,8 F; $f_\mathrm{i}$ = 40 Hz _Bass max, treble lin._ |
| Step width bass | $\Delta V_{15}$ | 1 | 3 | 5 | dB | 05,8X-05,8 (X ± 1) _Bass X – bass (X ± 1)_ |
| Step width bass | $\Delta V_{16}$ | 1 | 3 | 5 | dB | 05,8X-05,8 (X ± 1) _Bass X – bass (X ± 1)_ |

**Characteristics** (cont'd)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|-----------|--------|------|------|------|------|----------------|
| | | min. | typ. | max. | | |
| Treble boost | $V_{16\text{-}1}$ | 10 | 12 | | dB | 05,8 F; $f_\text{l}$ = 15 Hz<br>*Treble max, bass lin.* |
| Treble boost | $V_{15\text{-}3}$ | 10 | 12 | | dB | 05,8 F; $f_\text{l}$ = 15 Hz<br>*Treble max, bass lin.* |
| Treble cut | $V_{16\text{-}1}$ | | – 12 | | dB | 05,8 F; $f_\text{l}$ = 15 Hz<br>*Treble max, bass lin.* |
| Treble cut | $V_{15\text{-}3}$ | | – 12 | | dB | 05,8 F; $f_\text{l}$ = 15 Hz<br>*Treble max, bass lin.* |
| Step width bass | $\Delta V_{15}$ | 1 | 3 | 5 | dB | 05,X8-05 (X ± 1)8<br>*Treble X – treble (X ± 1)* |
| Step width bass | $\Delta V_{16}$ | 1 | 3 | 5 | dB | 05,X8-05 (X ± 1)8<br>*Treble X – treble (X ± 1)* |
| Linearity sound | $\Delta V_{15}$ | | | ± 2 | dB | 05,88;<br>$f_\text{l}$ = 40 Hz – 15 kHz<br>*Treble, bass lin.* |
| Linearity sound | $\Delta V_{16}$ | | | ± 2 | dB | 05,88;<br>$f_\text{l}$ = 40 Hz – 15 kHz<br>*Treble, bass lin.* |
| Detection level of the clipping detector | $V_1$ | | 580 | | mVrms | 05,8 F; $f_\text{l}$ = 40 Hz<br>*Treble lin, bass* max.<br>01,2F - 02,2F<br>*Vol* $_{LSl}$ *47 – Vol* $_{LSr}$ *47* |

The same values are valid if the test signals are applied at pin 3, 6, 7 or 8

| | | | | | | |
|-----------|--------|------|------|------|------|----------------|
| Channel separation | $\Delta V_{15\text{-}16}$ | 50 | | | dB | $V_3$ or $V_8$ = 600 mVrms |
| Channel separation of the clipping | $\Delta V_{19\text{-}20}$ | 50 | | | dB | $V_3$ or $V_8$ = 600 mVrms |
| Channel separation | $\Delta V_{9\text{-}10}$ | 50 | | | dB | $V_3$ or $V_8$ = 600 mVrms |
| Cross talk attenuation switch | $\alpha_\text{I interf / Q rms}$ | | | | | $V_\text{I rms}$ = 0<br>$V_\text{I Interf, 3,6}$ = 600 mVrms |
| | | 60 | | | dB | $V_\text{I Interf, 7,8}$ = 2 Vrms |

**Characteristics** (cont'd)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Attenuation MUTE | $\alpha_{1-16}$ | 80 | | | dB | 01,00 - 02,00<br>$Vol_{LSl}\ 0 - Vol_{LSr}\ 0$<br>$V_1 = 600$ mVrms |
| Attenuation MUTE | $\alpha_{1-16}$ | 80 | | | dB | 07,48;<br>$V_1 = 600$ mVrms<br>$MUTE\ I:\ 0$ |
| Attenuation MUTE | $\alpha_{1-16}$ | 80 | | | dB | 07,88;<br>$V_1 = 600$ mVrms<br>$MUTE\ II:\ 0$ |
| Attenuation MUTE | $\alpha_{3-15}$ | 80 | | | dB | 01,00 - 02,00<br>$Vol_{LSl}\ 0 - Vol_{LSr}\ 0$<br>$V_3 = 600$ mVrms |
| Attenuation MUTE | $\alpha_{3-15}$ | 80 | | | dB | 07,48;<br>$V_3 = 600$ mVrms<br>$MUTE\ I:\ 0$ |
| Attenuation MUTE | $\alpha_{3-15}$ | 80 | | | dB | 07,88;<br>$V_3 = 600$ mVrms<br>$MUTE\ II:\ 0$ |
| Attenuation MUTE | $\alpha_{1-20}$ | 80 | | | dB | 03,00;<br>$V_1 = 600$ mVrms<br>$Vol_{HP}\ 0$ |
| Attenuation MUTE | $\alpha_{1-20}$ | 80 | | | dB | 07,48;<br>$V_1 = 600$ mVrms<br>$MUTE\ I:\ 0$ |

**Characteristics** (cont'd)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Attenuation MUTE | $\alpha_{3-19}$ | 80 | | | dB | 03,00;<br>$V_3 = 600$ mVrms<br>*MUTE I: 0* |
| Attenuation MUTE | $\alpha_{3-19}$ | 80 | | | dB | 07,48;<br>$V_1 = 600$ mVrms<br>*MUTE I: 0* |
| Analogous values are valid for feed in at pins 6, 7, 8; $V_{7,8} = 2$ Vrms; $V_6 = 600$ mVrms | | | | | | |
| Attenuation MUTE | $\alpha_{3-10}$ | 80 | | | dB | 07,48;<br>$V_3 = 600$ mVrms<br>*MUTE I: 0* |
| Attenuation MUTE | $\alpha_{1-9}$ | 80 | | | dB | 07,48;<br>$V_1 = 600$ mVrms<br>*MUTE I: 0* |
| Attenuation MUTE | $\alpha_{6-10}$ | 80 | | | dB | 07,49;<br>$V_6 = 600$ mVrms<br>*MUTE I: 0, AM* |
| Attenuation MUTE | $\alpha_{6-9}$ | 80 | | | dB | 07,49;<br>$V_6 = 600$ mVrms<br>*MUTE I: 0, AM* |
| Max. input voltage | $V_6$ | 600 | | | mVrms | $THD_{15, 16} = 1\%$ |
| Max. input voltage | $V_3$ | 600 | | | mVrms | $THD_{15} = 1\%$ |
| Max. input voltage | $V_3$ | 600 | | | mVrms | $THD_{16} = 1\%$ |
| Max. input voltage | $V_1$ | 300 | | | mVrms | $THD_{16} = 1\%$; 00,02<br>*Matrix; Stereo* |
| Max. input voltage*) | $V_7$ | 2 | | | Vrms | $THD_{16} = 3\%$; 07,<br>*CC, Scart* |
| Max. input voltage*) | $V_8$ | 2 | | | Vrms | $THD_{15} = 1\%$; 07,<br>*CC, Scart* |

*) The tone control is possible over the full functional range if 04, 18, *Vol* $_{VLS}$ *24*

**Characteristics** (cont'd)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|-----------|--------|------|------|------|------|----------------|
|           |        | min. | typ. | max. |      |                |
| Distortion | $THD_{19}$ |  | 0.01 | 0.1 | % | $V_3$ = 250 mVrms |
| Distortion | $THD_{20}$ |  | 0.01 | 0.1 | % | $V_1$ = 250 mVrms |
| Distortion | $THD_{19}$ |  | 0.01 | 0.1 | % | $V_3$ = 250 mVrms; 03,15 *Vol* $_{HP}$ *21* |
| Distortion | $THD_{20}$ |  | 0.01 | 0.1 | % | $V_3$ = 250 mVrms; 03,15 *Vol* $_{HP}$ *21* |
| Analogous values are valid for feed in at pins 6, 7, 8; $V_{7,8}$ = 600 Vrms; $V_6$ = 250 mVrms | | | | | | |
| Distortion | $THD_{16}$ |  | 0.01 | 0.1 | % | $V_1$ = 250 mVrms; |
| Distortion | $THD_{15}$ |  | 0.01 | 0.1 | % | $V_3$ = 250 mVrms |
| Distortion | $THD_{15}$ |  | 0.01 | 0.2 | % | $V_1$ = 250 mVrms; 01,2F-02,2F *Vol* $_{LSl}$ *47 Vol* $_{LSr}$ *47* |
| Distortion | $THD_{15}$ |  | 0.01 | 0.2 | % | $V_3$ = 250 mVrms; 01,2F-02,2F *Vol* $_{LSl}$ *47 Vol* $_{LSr}$ *47* |
| Distortion | $THD_{16}$ |  | 0.1 | 0.4 | % | $V_1$ = 250 mVrms; 05,XX any sound |
| Distortion | $THD_{15}$ |  | 0.1 | 0.4 | % | $V_3$ = 250 mVrms; 05,XX any sound |
| Analogous values are valid for feed in at pins 6, 7, 8; $V_{7,8}$ = 600 mVrms; $V_6$ = 250 mVrms | | | | | | |
| Distortion | $THD_{10}$ |  | 0.01 | 0.1 | % | $V_3$ = 250 mVrms |
| Distortion | $THD_9$ |  | 0.01 | 0.1 | % | $V_1$ = 250 mVrms |
| Distortion | $THD_{10}$ |  | 0.01 | 0.1 | % | $V_6$ = 250 mVrms; 07,C9,*AM* |
| Distortion | $THD_9$ |  | 0.01 | 0.1 | % | $V_6$ = 250 mVrms; 07,C9,*AM* |

**Characteristics** (cont'd)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Anti-phase cross talk Base width | $\Delta V_{16\text{-}15}$ | 0.5 | 0.55 | | | $V_3$ = 600 mVrms $f_1$ = 2 kHz; 00, 11 *Base width* |
| Anti-phase cross talk Base width | $\Delta V_{15\text{-}16}$ | 0.5 | 0.55 | | | $V_1$ = 600 mVrms $f_1$ = 2 kHz; 00, 11 *Base width* |
| Base width phase | $\Phi_{16\text{-}15}$ | 150 | 180 | 210 | deg | $V_1$ = 600 mVrms $f$ = 2 kHz; 00, 11 *Base width* |
| Base width phase | $\Phi_{15\text{-}16}$ | 150 | 180 | 210 | deg | $V_3$ = 600 mVrms $f$ = 2 kHz; 00, 11 *Base width* |
| Phase rotation quasi stereo | $\Phi_{16\text{-}15}$ | 0 | 10 | 40 | deg | $V_{3,1}$ = 600 mVrms $f$ = 40 kHz; 00, 21 *Quasi stereo* |
| Phase rotation quasi stereo | $\Phi_{16\text{-}15}$ | 130 | 180 | 230 | deg | $V_{3,1}$ = 600 mVrms $f$ = 700 kHz; 00, 21 *Quasi stereo* |
| Phase rotation quasi stereo | $\Phi_{16\text{-}15}$ | – 30 | 10 | 0 | deg | $V_{3,1}$ = 600 mVrms $f$ = 15 kHz; 00, 21 *Quasi stereo* |
| Signal-to-noise ratio | $\alpha_{S/N16}$ | 85 | 94 | | dB | $V_{N\text{ rms 20 Hz-20 kHz}}$; $V_1$ = 0.6 Vrms |
| Signal-to-noise ratio | $\alpha_{S/N15}$ | 85 | 94 | | dB | $V_{N\text{ rms 20 Hz-20 kHz}}$; $V_3$ = 0.6 Vrms |
| Signal-to-noise ratio | $\alpha_{S/N16}$ | 60 | 70 | | dB | $V_{N\text{ rms 20 Hz-20 kHz}}$; $V_1$ = 0.6 Vrms 01,27-02,27 $Vol_{LSl}$ 39-$Vol_{LSr}$ 39 |
| Signal-to-noise ratio | $\alpha_{S/N15}$ | 60 | 70 | | dB | $V_{N\text{ rms 20 Hz-20 kHz}}$; $V_3$ = 0.6 Vrms 01,27-02,27 $Vol_{LSl}$ 39 – $Vol_{LSr}$ 39 |

**Characteristics** (cont'd)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Output noise voltage | $V_{N16}$ | | 12 | 33 | μVrms | $V_{N}$ rms 20 Hz-20 kHz; 01,00-02,00 $Vol_{LSl}\,0$-$Vol_{LSr}\,0$ |
| Output noise voltage | $V_{N15}$ | | 12 | 33 | μVrms | $V_{N}$ rms 20 Hz-20 kHz; 01,00-02,00 $Vol_{LSl}\,0$-$Vol_{LSr}\,0$ |
| Signal-to-noise ratio | $\alpha_{S/N20}$ | 85 | 94 | | dB | $V_{N}$ rms 20 Hz-20 kHz; $V_1 = 0.6$ Vrms |
| Signal-to-noise ratio | $\alpha_{S/N19}$ | 85 | 94 | | dB | $V_{N}$ rms 20 Hz-20 kHz; $V_3 = 0.6$ Vrms |
| Signal-to-noise ratio | $\alpha_{S/N20}$ | 65 | 70 | | dB | $V_{N}$ rms 20 Hz-20 kHz; $V_1 = 0.6$ Vrms 03, 10, $Vol_{HP}\,16$ |
| Signal-to-noise ratio | $\alpha_{S/N19}$ | 65 | 70 | | dB | $V_{N}$ rms 20 Hz-20 kHz; $V_3 = 0.6$ Vrms 03, 10, $Vol_{HP}\,16$ |
| Output noise voltage | $V_{N20}$ | | 12 | 33 | μVrms | $V_{N}$ rms 20 Hz-20 kHz; 03, 00, $Vol_{HP}\,0$ |
| Output noise voltage | $V_{N19}$ | | 12 | 33 | μVrms | $V_{N}$ rms 20 Hz-20 kHz; 03, 00, $Vol_{HP}\,0$ |
| Signal-to-noise ratio | $\alpha_{S/N9}$ | 90 | 97 | | dB | $V_{N}$ rms 20 Hz-20 kHz; $V_1 = 0.6$ Vrms |
| Signal-to-noise ratio | $\alpha_{S/N10}$ | 90 | 97 | | dB | $V_{N}$ rms 20 Hz-20 kHz; $V_1 = 0.6$ Vrms |

Characteristics (cont'd)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| DC/pop $\Delta 1$ Bit | $\Delta V_{16}$ | | | $\pm 4$ | mV | 01, X-01, X $\pm$ 1 $Vol_{LSl} X - Vol_{LSl} (X \pm 1)$ |
| DC/pop $\Delta 1$ Bit | $\Delta V_{15}$ | | | $\pm 4$ | mV | 02, X-02, X $\pm$ 1 $Vol_{LSr} X - Vol_{LSr} (X \pm 1)$ |
| DC/pop $\Delta 1$ Bit | $\Delta V_{16}$ | | | $\pm 4$ | mV | 04, X-04, X $\pm$ 1 $Vol_{VLS} X - Vol_{VLS} (X \pm 1)$ |
| DC/pop $\Delta 1$ Bit | $\Delta V_{15}$ | | | $\pm 4$ | mV | 04, X-04, X $\pm$ 1 $Vol_{VLS} X - Vol_{VLS} (X \pm 1)$ |
| DC/pop $\Delta 1$ Bit | $\Delta V_{16}$ | | | $\pm 2$ | mV | 05, X-05, X $\pm$ 1 $Tone X - Tone (X \pm 1)$ |
| DC/pop $\Delta 1$ Bit | $\Delta V_{15}$ | | | $\pm 2$ | mV | 05, X-05, X $\pm$ 1 $Tone X - Tone (X \pm 1)$ |
| DC/pop $\Delta 1$ Bit | $\Delta V_{19}$ | | | $\pm 4$ | mV | 03, X-03, X $\pm$ 1 $Vol_{HP} X - Vol_{HP} (X \pm 1)$ |
| DC/pop $\Delta 1$ Bit | $\Delta V_{20}$ | | | $\pm 4$ | mV | 03, X-03, X $\pm$ 1 $Vol_{HP} X - Vol_{HP} (X \pm 1)$ |

**Design-Related Data**

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Input resistance | $R_7$ | 35 | | | k$\Omega$ | |
| Input resistance | $R_8$ | 35 | | | k$\Omega$ | |
| Input resistance | $R_6$ | 20 | | | k$\Omega$ | |
| Input resistance | $R_3$ | 22 | | | k$\Omega$ | |
| Input resistance | $R_1$ | 22 | | | k$\Omega$ | |
| Output resistance | $R_{19}$ | | | 70 | $\Omega$ | |
| Output resistance | $R_{20}$ | | | 70 | $\Omega$ | |
| Output resistance | $R_{15}$ | | | 70 | $\Omega$ | |
| Output resistance | $R_{16}$ | | | 70 | $\Omega$ | |
| Output resistance | $R_9$ | | | 70 | $\Omega$ | |
| Output resistance | $R_{10}$ | | | 70 | $\Omega$ | |

## Characteristics (cont'd)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition | Test Circuit |
|---|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | | |
| **ID-Signal Decoder** | | | | | | | |
| Gain filter OP-amplif. | $V_5$ | 13 | 14 | 15 | dB | $V_{IF} = 80$ mVpp | 1 |
| Max. input voltage | $V_5$ | 600 | | | mVpp | Function | 2 |
| VCO-voltage PLL | $V_{27}$ | 1.3 | | | V | $f_{24} = 14.6$ kHz; $V_{24} = 2.5$ V | 2 |
| VCO-voltage PLL | $V_{27}$ | 2 | 3 | 4 | V | $f_{24} = 15.625$ kHz; $V_{24} = 2.5$ V | 2 |
| VCO-voltage PLL | $V_{27}$ | | | 4.7 | V | $f_{24} = 16.6$ kHz; $V_{24} = 2.5$ V | 2 |
| VCO-voltage PLL | $V_{27}$ | 1.3 | | | V | $f_{24} = 58.4$ kHz; $V_{24} = 2.5$ V 00,08, *H-pulse* | 2 |
| VCO-voltage PLL | $V_{27}$ | | | 4.7 | V | $f_{24} = 66.4$ kHz; $V_{24} = 2.5$ V 00,08, *H-pulse* | 2 |
| VCO-voltage PLL | $V_{27}$ | 2 | 3 | 4 | V | 00,08 - 04.81 *H-pulse; quartz cont. function* | 4 |

$$V_{Filter\ gain} = \frac{\sqrt{(V_{25} - V_{25}^{*})^2 + (V_{26} - V_{26}^{*})^2}}{V_5} \quad \begin{array}{l} V_{25}\ or\ V_{26}\ when\ V_5 = 0 \\ V_{25}^{*}\ or\ V_{26}^{*}\ when\ V_5 = 100\ mVpp;\ m = 50\% \end{array}$$

| Parameter | Symbol | Limit Values | | | Unit | Test Condition | Test Circuit |
|---|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | | |
| ID-filter gain | $V_{KT\ Filter}$ | 3.4 | | 6.8 | V | $f_5$ = pilot signal dual; I²C-talk: dual | 2 |
| ID-filter gain | $V_{KT\ Filter}$ | 3.4 | | 6.8 | V | $f_5$ = pilot signal stereo; I²C-talk: stereo | 2 |

$V_{5\ test} = V_{25\ (V_5 = 0)} \pm \Delta V_{25}$; $V_{26\ test} = V_{26\ (V_5 = 0)} \pm \Delta V_{26}$

**Characteristics** (cont'd)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition | Test Circuit |
|---|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | | |
| Detection threshold | $\Delta V_{25}$ | 900 | | | mV | I²C-talk: stereo or dual | 3 |
| Detection threshold | $-\Delta V_{25}$ | 900 | | | mV | I²C-talk: stereo or dual | 3 |
| Detection threshold | $\Delta V_{26}$ | 900 | | | mV | I²C-talk: stereo or dual | 3 |
| Detection threshold | $-\Delta V_{26}$ | 900 | | | mV | I²C-talk: stereo or dual | 3 |
| Mono threshold | $\Delta V_{25}$ | 0 | | 100 | mV | I²C-talk: mono | 3 |
| Mono threshold | $-\Delta V_{25}$ | 0 | | 100 | mV | I²C-talk: mono | 3 |
| Mono threshold | $\Delta V_{26}$ | 0 | | 100 | mV | I²C-talk: mono | 3 |
| Mono threshold | $-\Delta V_{26}$ | 0 | | 100 | mV | I²C-talk: mono | 3 |
| Response of detection | $t_{det}$ | 1/4 | | 1/2 | $t_{MPX}$ | I²C-talk: stereo or dual; $\pm\Delta V_{25}$ = 1 V | 3 |
| Response of detection | $t_{det}$ | 1/4 | | 1/2 | $t_{MPX}$ | I²C-talk: stereo or dual; $\pm\Delta V_{26}$ = 1 V | 3 |

**Characteristics** (cont'd)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition | Test Circuit |
|---|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | | |
| Switching threshold $f_{REF}$-input | $V_{H \, in \, L}$ | 0 | | 1.5 | V | | 2 |
| Switching threshold $f_{REF}$-input | $V_{H \, in \, L}$ | 3.5 | | $V_{21}$ | V | | 2 |
| Amplitude crystal oscillator | $V_{24}$ | | 0.3 | | Vpp | $f_0 = 4.00000$ MHz Serial resonance | 4 |
| Ext. 1- or 4 MHz-clock signal | $V_{24}$ | | 2 | | Vpp | | 3 |
| Crystal current | $I_C$ | 0.29 | 0.35 | 0.42 | mArms | $R_C = 40 \ \Omega$ | |
| Multiplexer clock | $t_{MPX}$ | | 2.17 | | s | 09,08, $MPX = 2 \, s$ | |
| Multiplexer clock | $t_{MPX}$ | | 4.34 | | s | 09,48, $MPX = 4 \, s$ | |
| Multiplexer clock | $t_{MPX}$ | | 8.68 | | s | 09,88, $MPX = 8 \, s$ | |
| **Design-Related Data** | | | | | | | |
| Filter output resistance | $R_{25,26}$ | 110 | | | k$\Omega$ | | |
| $f_{REF}$-input resistance | $R_{24}$ | 800 | | | $\Omega$ | | |
| Input impedance crystal oscillator | $Z_{24}$ | $-600$ | $-500$ | $-400$ | $\Omega$ | | |
| Crystal serial resistance | $R_{C1}$ | | | 100 | $\Omega$ | $P_{tot} = 1 \ \mu W$, fundamental | |
| Crystal serial resistance | $R_{C3}$ | 300 | | | $\Omega$ | $P_{tot} = 1 \ \mu W$ 3rd harmonic | |
| Spurious wave spacing (fundamental wave to harmonic and nonharmonic signals) | | 20 | | | dB | $P_{tot} = 1 \ \mu W$ $f < 15$ MHz | |

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**Characteristics** (cont'd)

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| **I²C Bus (SCL, SDA)** | | | | | | |
| SCL, SDA edges | | | | | | |
| Rise time | $t_R$ | | | 1 | μs | |
| Fall time | $t_F$ | | | 300 | ns | |
| Shift register clock pulse SCL | | | | | | |
| Frequency | $f_{SCL}$ | 0 | | 100 | kHz | |
| H-pulse width | $t_{HIGH}$ | 4 | | | μs | |
| L-pulse width | $t_{LOW}$ | 4 | | | μs | |
| Start | | | | | | |
| Set-up time | $t_{SUSTA}$ | 4 | | | μs | |
| Hold time | $t_{HDSTA}$ | 4 | | | μs | |
| Stop | | | | | | |
| Set-up time | $t_{SUDAT}$ | 1 | | | μs | |
| Bus free time | $t_{HDDAT}$ | 1 | | | μs | |
| Data transfer | | | | | | |
| Set-up time | $t_{SUDAT}$ | 1 | | | μs | |
| Hold time | $t_{HDDAT}$ | 600 | | | ns | |
| Input SCL, SDA | | | | | | |
| Input voltage | $V_{QH}$ | 3 | | 5.5 | V | |
| | $V_{QL}$ | | | 1.5 | V | |
| Input current | $V_{QH}$ | | | 50 | μA | |
| | $V_{QL}$ | | | 100 | μA | |
| Output SDA (Open collector) | | | | | | |
| Output voltage | $V_{QH}$ | 5.4 | | | V | $R_L = 2.5\ \text{k}\Omega$ |
| | $V_{QL}$ | | | 0.4 | V | $I_{QL} = 3\ \text{mA}$ |

UEB03417
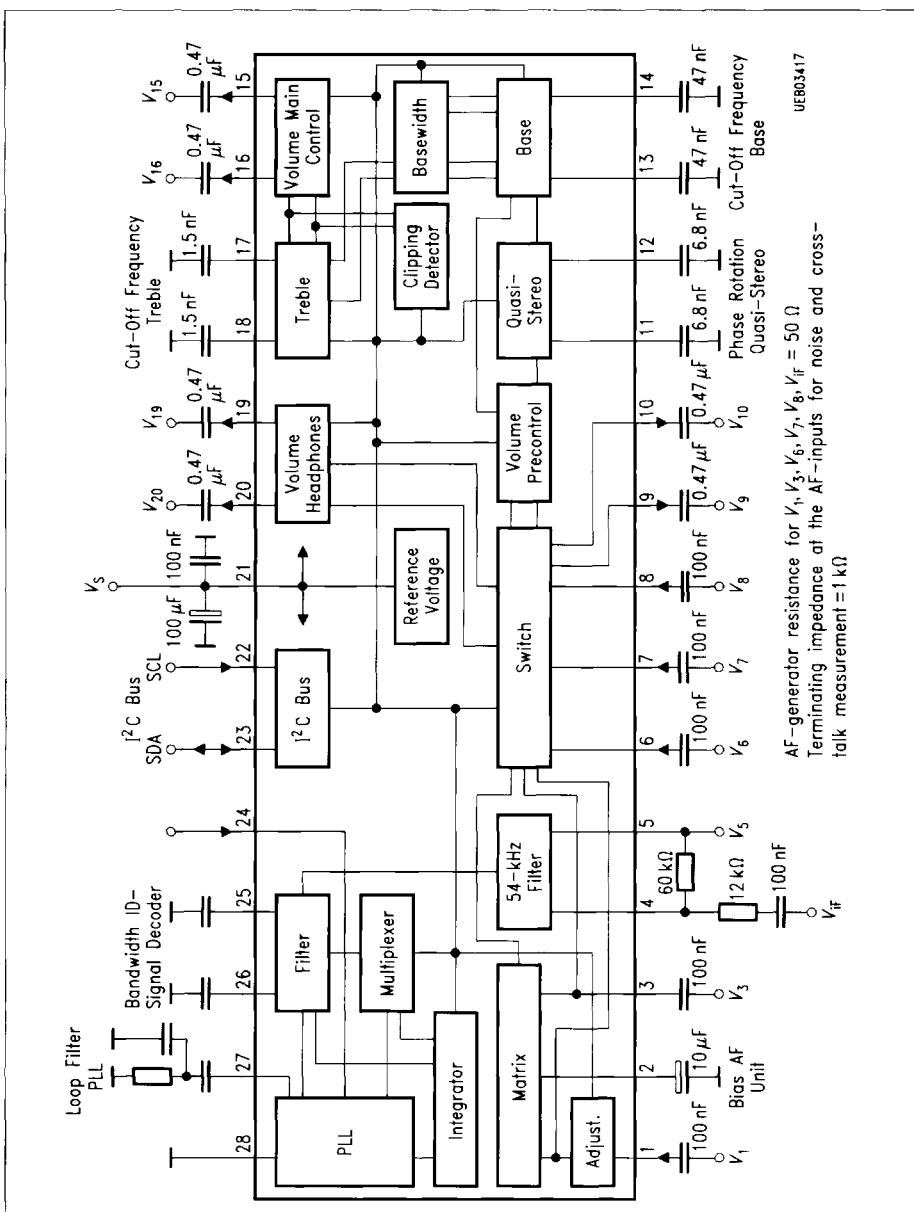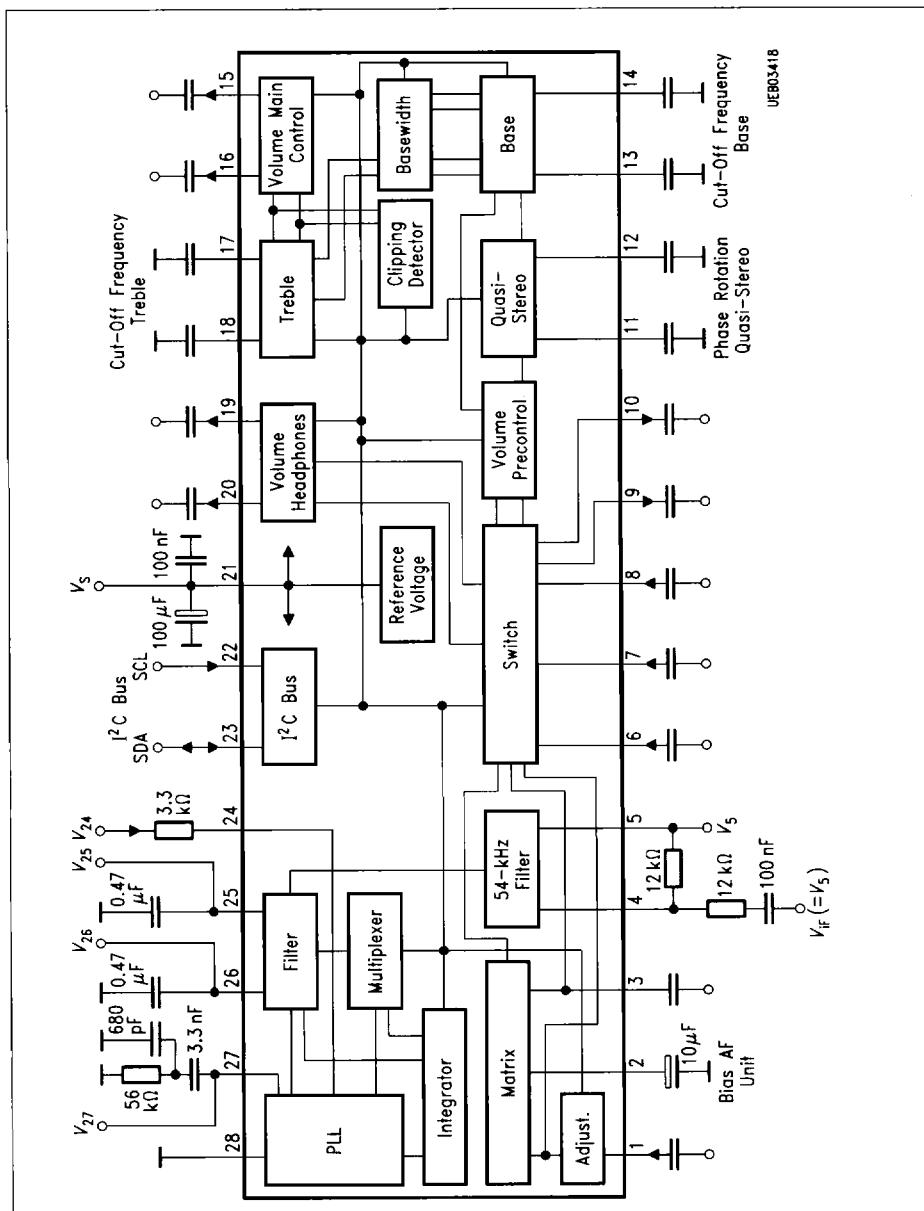
**Test Circuit 1**

**Test Circuit 2**

**Test Circuit 3**

UEB03420

**Test Circuit 4**

UEB03421

**Application Circuit 1**

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**Application Circuit 2**

**Application Circuit 3**

UED03424
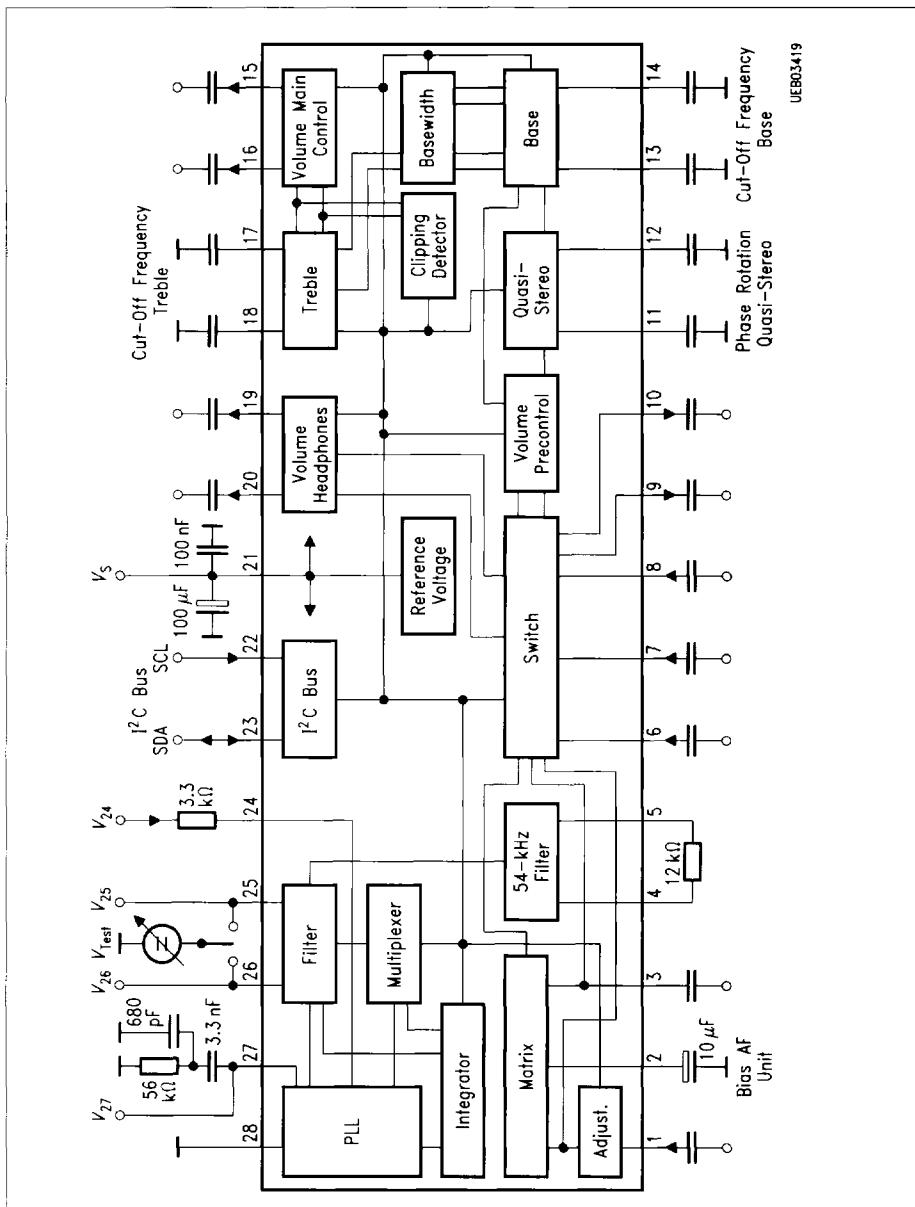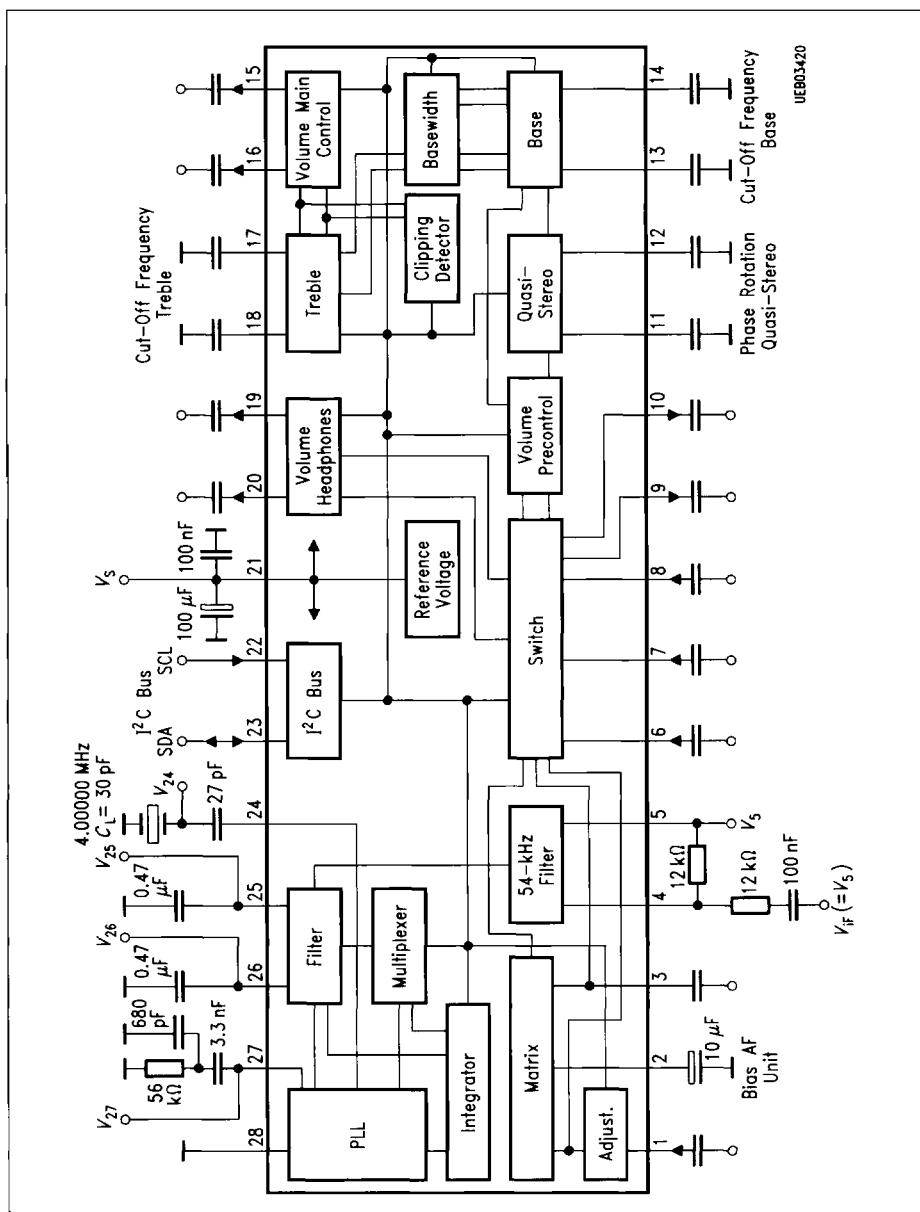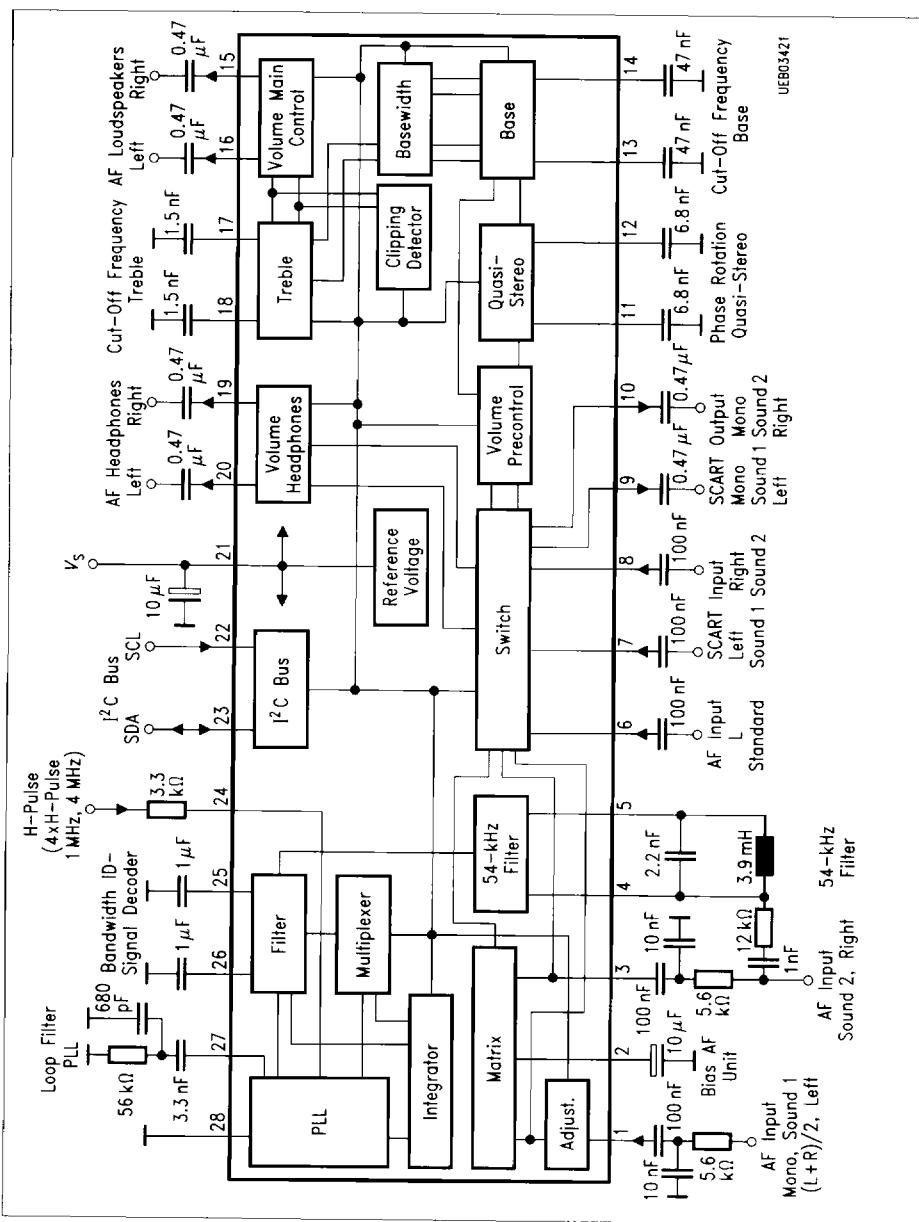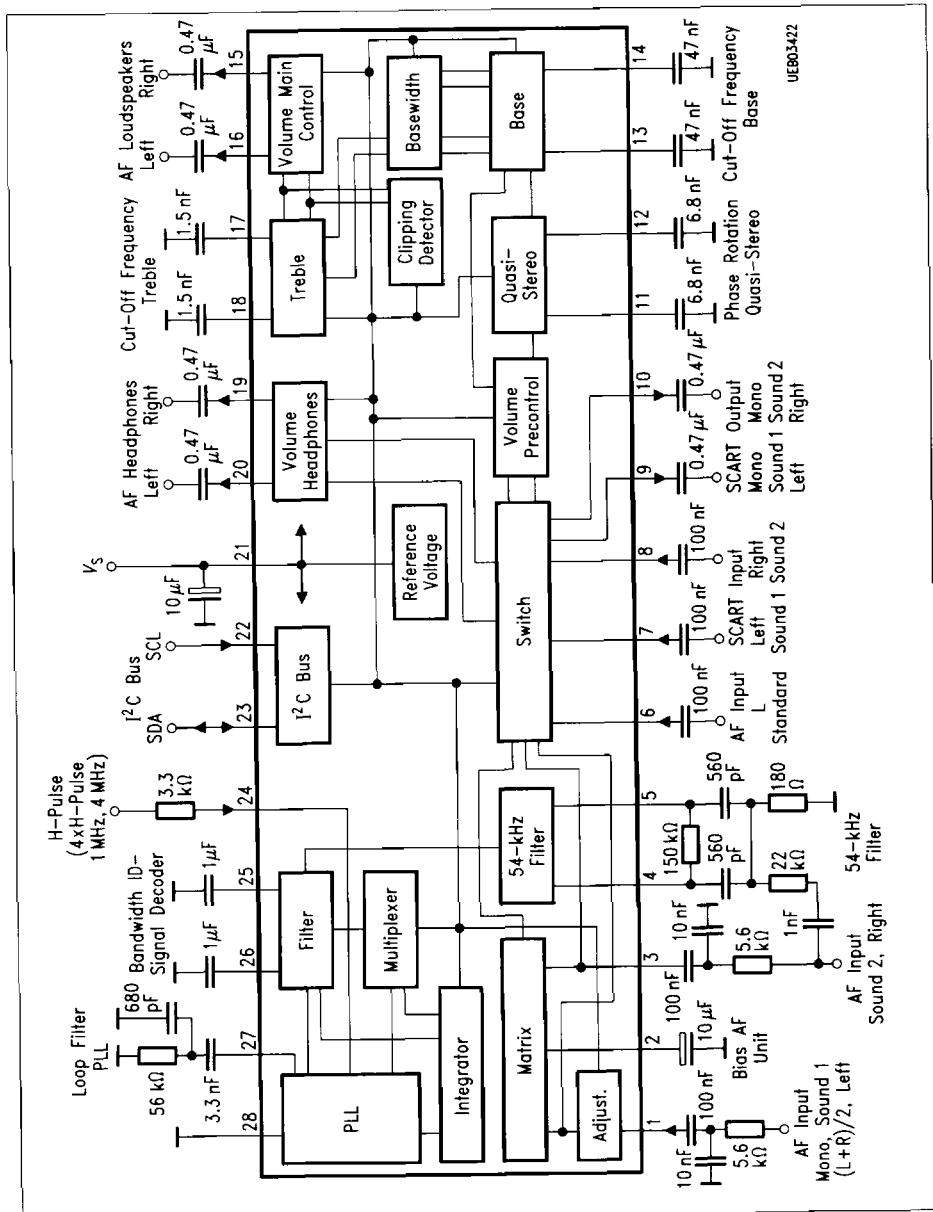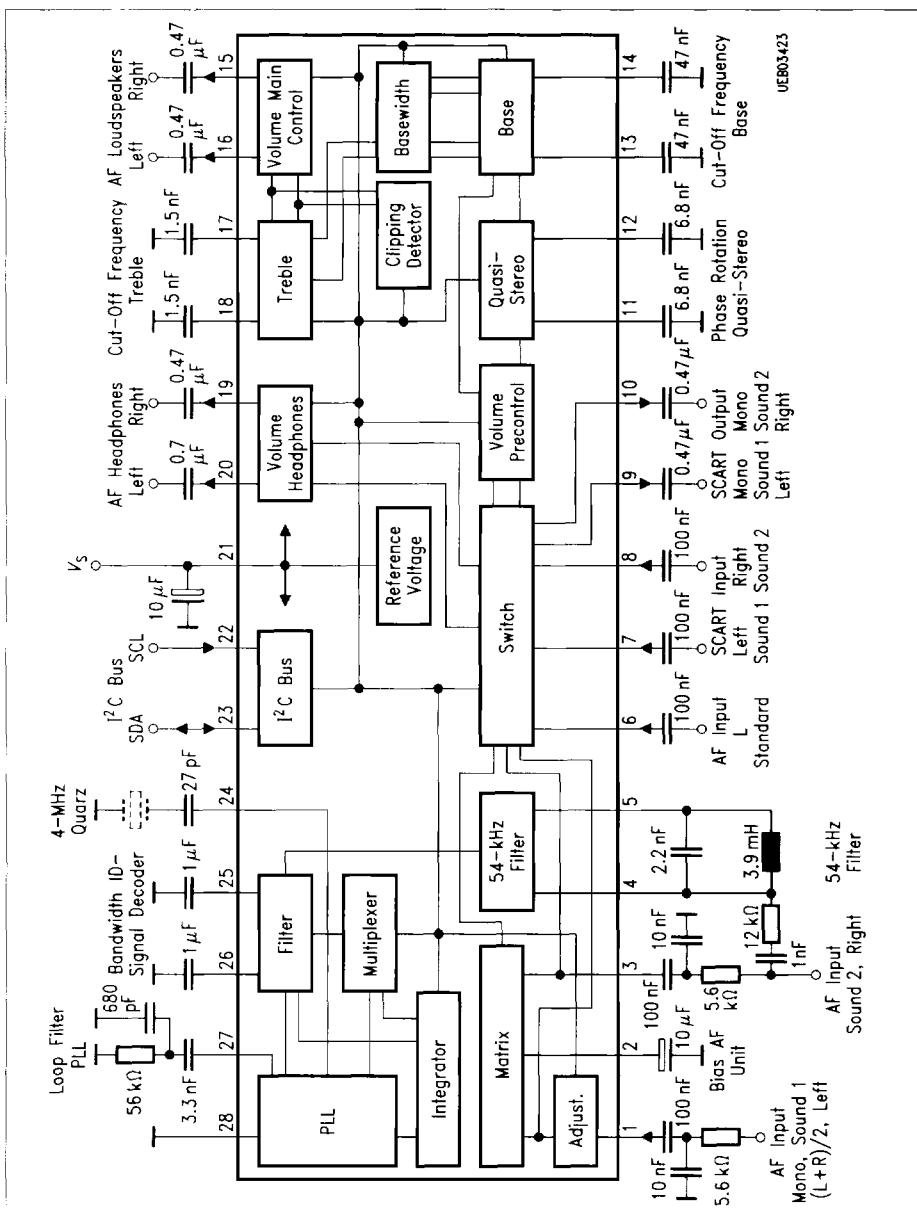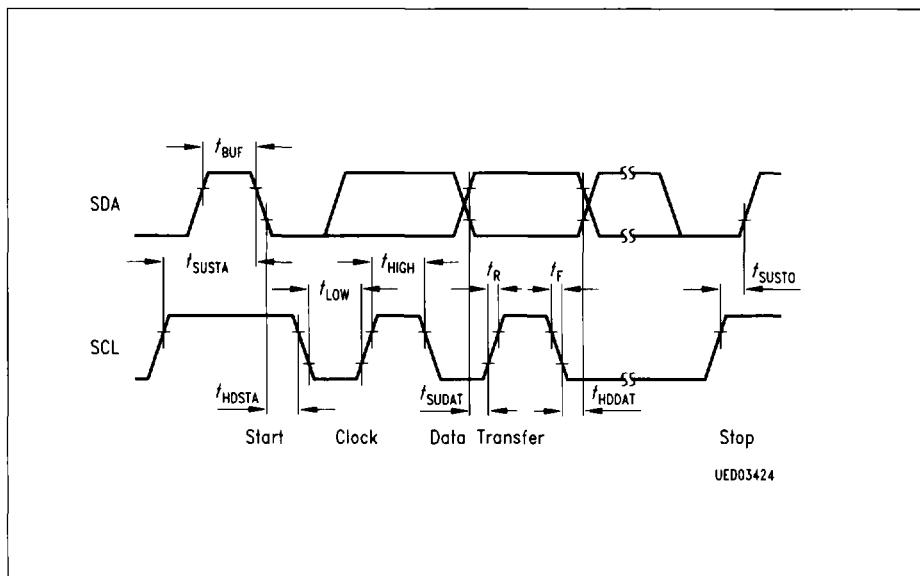
**I²C Bus Timing Diagram**

| | |
|---|---|
| $t_{SUSTA}$ | Setup time (start) |
| $t_{HDSTA}$ | Hold time (start) |
| $t_{HIGH}$ | H-pulse width (clock) |
| $t_{LOW}$ | L-pulse width (clock) |
| $t_{SUDAT}$ | Setup time (data transfer) |
| $t_{HDDAT}$ | Hold time (data transfer) |
| $t_{SUSTO}$ | Setup time (stop) |
| $t_{BUF}$ | Bus free time |
| $t_F$ | Fall time |
| $t_R$ | Rise time |

All times referred to $V_{IH}$ and $V_{IL}$ values.

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**Package Outlines**

**Plastic Package, P-DIP-28-1**
(Plastic Dual In-Line Package)



Index Marking
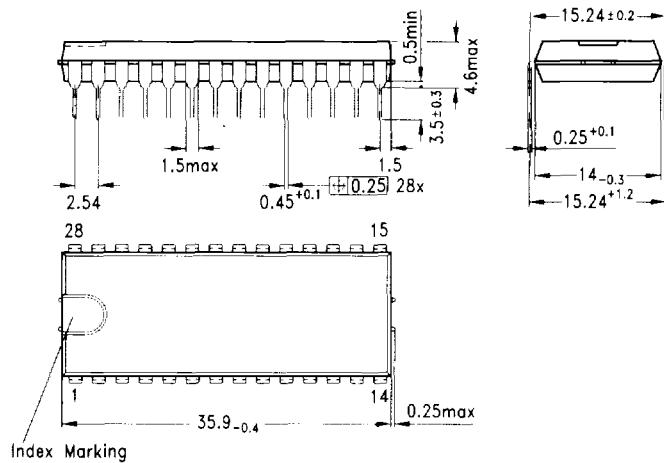
GPD05037

**Plastic Package, P-DSO-28.350 (SMD)**
(Plastic Dual Small Outline)



Index Marking
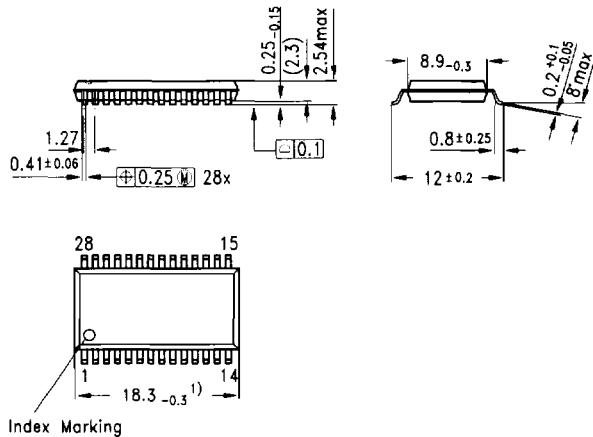
1) Does not include plastic or metal protrusions of 0.25 max per side

GPS05182

**Sorts of Packing**
Package outlines for tubes, trays etc. are contained in our
Data Book "Package Information"
SMD = Surface Mounted Device

Dimensions in mm

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