XR-T6164/65/66 Evaluation System

GENERAL DESCRIPTION

This application note describes the XR-T6164/65/66 evaluation kit. This two chip set performs the 64kBPS co-directional interface function as defined in CCITT G.703 recommendations. The newly developed adaptation unit (DAU 64) provide access to a time slot of the PCM frame.

Primary PCM CH-30 has been used originally for voice transmission. The increasing need for high-speed data transmission has lead to the development of equipment which allows the user to multiplex data and digitized voice information into a common 2048kBPS PCM channel. With the XR-T6164/65/66 chip set, a data adaptation unit (DAU) can be realized with minimal components. Various application areas using T6164/65/66 chip set are shown in figure 3 and 4. The main function of a DAU is to provide access to any time slot of a PCM frame in both transmit and receive directions.

BASIC OPERATION

The T6164 is a 16 pin analog device. It consists of both a line driver and a line receiver to interface to the twisted pair cable via external transformers. The T6165 or T6166 are digital CMOS ICs which perform the necessary data format and rate conversions between G.703 64kBPS and PCM 2048kBPS data.

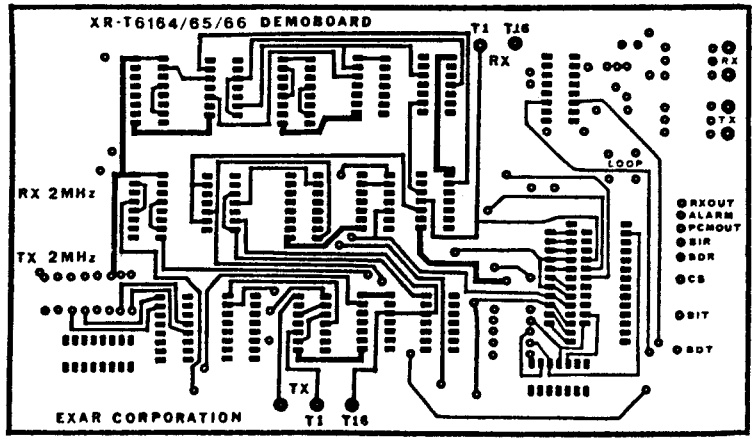
DATA EXTRACTION FROM THE FRAME

To extract 64kBPS data from a PCM CH-30 system, the 2048kBPS signal is applied to the input of the digital transmitter together with synchronous 2.048MHz and 256KHz clocks. When a time slot pulse goes high (8 clock pulses derived externally) the information present will be clocked into the transmitter. Four periods are dedicated to each bit of 64kbit/s data in order to code "0" as 0101 and "1" as 0011. The binary signal is then converted into a modified bipolar signal by alternating the polarity of the consecutive blocks, and output as "T+R" and "T-R" to the line driver portion of the T6164 for transmission. The final bit of each input word is coded with a bipolar violation producing the necessary octet timing information.

DATA INSERTION INTO THE PCM FRAME

Incoming bipolar signals at the secondary of the input transformer are fed to the receiver portion of the T6164, which consists of a peak detector and two data comparators for positive and negative data retrieval. The receiver has adequate sensitivity to accurately extract data which has been attenuated by cable losses of up to 10dB at 128KHz.

Receiving data is converted into LSTTL compatible signals and output as "S+R" and "S-R" to the T6165 or T6166 for timing extraction and formatting.



Before data can be inserted into the PCM frame, it is necessary to regenerate a 64KHz clock from the incoming signal for synchronization and data decoding. This is done with an octet locking circuit and a variable length counter which behaves like a digital phase lock-loop. Once in sync., data can be multiplexed into the PCM frame under the control of receive 2.048MHz read clock and a time slot pulse. When the time slot goes high, a burst of eight bits data at 2.048MHz rate is sent out at "PCM OUT".

TIMING AND BLOCK DIAGRAM

Figure 5 shows a typical application circuit for the T6164/6165 and their block diagrams. Pulse masks and coding for a codirectional G.703 interface are shown if figure 1 and 2.

DEMO KIT INSTRUCTIONS

The kit contains a printed circuit board which permits easy evaluation of the T6164/T6165 or T6166 parts. The board requires two external 2048KHz clocks, one for transmit and the other for receive. These clocks are TTL level clocks applied to the Rx 2MHz and Tx 2MHz BNC connectors. The rest of the timing signals are generated on-board using HCMOS logic. Power is applied to the red and black banana plugs. (red = +5V ±10%, black =0V)

OPERATION

After power up and with the two 2MHz clocks connected, check TS1 in both Tx and Rx for a stable time slot pulse. If any of these pulses cannot be synchronized by the scope, the external logic needs to be reset by disconnecting the +5V supply from the board and temporarily shorting its VCC line to ground.
The transmitter section generates two time slot pulses and an 8KHz frame clock. An 8 bit word is also generated on board whose output pattern can be selected by means of the 8 position DIP switch on the left. Depending on the position of S4, the 4th DIP switch on the right, the 8 bit word can be placed either in TS1 or TS16 of a frame. The transmit data is input to pin 15 of the XR-T6165 or pin 19 of the XR-T6166 and appears as positive and negative data at "T+R" and "T-R" respectively. This same data is then passed to the T6164 for transmission, the resulting bipolar signal can be observed at "TX O/P".

RECEIVER

The "TX O/P" data in this demo kit is looped back to the receive circuit via jumpers (Loop). With the loop broken, it is possible to evaluate the sensitivity of the receiver and other functions of the analog device by means of externally generated signals.

The XR-T6164 converts the incoming bipolar signals it receives into negative going LSTTL level data at "S+R" and "S-R". If sync. is achieved by the digital chip (this usually is not a problem as long as the Tx and Rx clock frequencies are within 2048KHz ±10KHz), the received data should appear at "PCM OUT". Figure 1 shows 8 bit data to be inserted into a PCM frame within an envelope of a time slot pulse.

The main difference between the XR-T6165 and the XR-T6166 is some added features which indicate repetitions and deletions of both received and transmitted data whenever clock skews or transients occur. An extracted receive clock output is also provided together with a receive clock loss of lock flag.

DIP 2 SWITCH SETTING

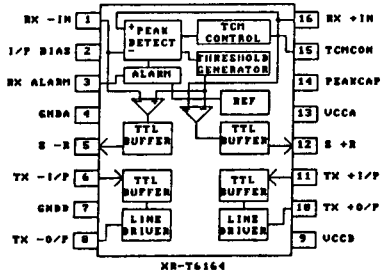
Switch 1 is intended to enable or disable the "Byte Locking" feature. When closed (active low) it causes blanking of PCMOUT under received alarm conditions.

Switch 2 forces the PCMOUT data stream to an all ones condition when closed (active low).

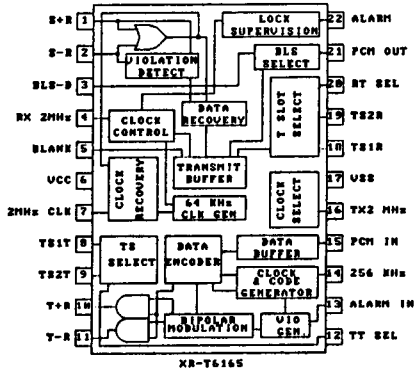
Switch 3 toggles the receiver time slot select of the XR-T6165 or 6166.

Switch 4 toggles the transmitter time slot select.

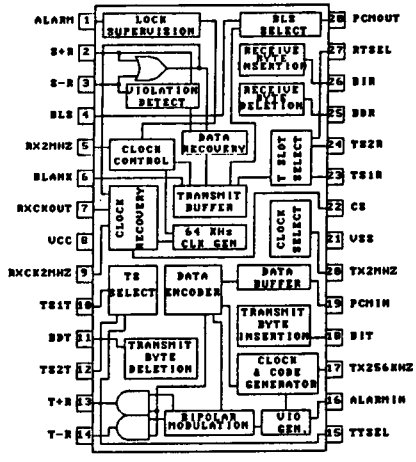
Switch 5 connects to the alarm input pin of the XR-T6165/66. When open (active high), the insertion of violations to the transmitted data is inhibited.



XR-T6164



XR-T6165



PIN DESCRIPTIONS - XR-T6164

Name	Pin	Description
RX-I/P	1	Receiver negative bipolar input.
I/P BIAS	2	Internally generated bias voltage for receive inputs.
RXALARM	3	Loss of signal alarm (<15dB) (Active Low)
GNDA	4	Analog Ground
S-R	5	Receive negative output data (Active Low)
TX-I/P	6	Transmit negative input signal (Active High)
GNDD	7	Digital Ground
TX-O/P	8	Transmit negative output data, open collector.
VCCD	9	+5V± 5% digital supply.
TX+O/P	10	Transmit positive output data, open collector.
TX+I/P	11	Transmit positive input signal (Active High).
S+R	12	Receive positive ouput data (Active Low).
VCCA	13	+5V ± 5% analog supply.
PEAKCAP	14	Receiver peak detector storage capacitor.
TCMCON	15	Time compression multiplex control pin (Active Low). When active disables Rx inputs and stores previous peak voltage.
RX+I/P	16	Receiver positive bipolar input.

PIN DESCRIPTIONS - XR-T6165

Name	Pin	Description
S+R	1	Positive AMI data to receiver (Active Low).
S-R	2	Negative AMI data to receiver (Active Low).
BLS	3	Byte locking supervision (Active Low). When active causes blanking of PCMOUT under received alarm conditions.
RX2MHZ	4	Receiver 2048KHz clock.
BLANK	5	PCMOUT data blanking (Active High). When active, forces PCMOUT data to all ones (AIS).
VCC	6	+5V ±5% power supply.
RXCK2MHZ	7	2048KHz clock recovery signal.
TS1T	8	Time slot input 1 for transmitter.
TS2T	9	Time slot input 2 for transmitter.
T+R	10	Transmit positive output AMI data (Active Low).
T-R	11	Transmit negative output AMI data (Active Low).
TTSEL	12	Transmit time slot select. When high pin 8 selected, when low pin 9 selected.
ALARMIN	13	Alarm input (Active High). When active inhibits insertionof violation into transmitted data.
TX256KHZ	14	Transmitter 256KHz clock.
PCMIN	15	Transmitter PCM input.
TX2MHZ	16	Transmitter 2048KHz clock.
VSS	17	Ground.
TS1R	18	Time slot input 1 for receiver.
TS2R	19	Time slot input 2 for receiver.
RTSEL	20	Receive time slot select. When high pin 18 selected, when low pin 19 selected.
PCMOUT	21	Received PCM output data.
ALARM	22	Alarm (Active High). When active, indicates loss of received bipolar violations.

PIN DESCRIPTION - XR-T6166

Name	Pin	Description
ALARM	1	Alarm (Active High) When active, indicates loss of received bipolar violations.
S+R	2	Positive AMI data to receiver (Active Low).
S-R	3	Negative AMI data to receiver(Active Low).
BLS	4	Byte Locking Supervision (Active Low). Causes blanking of PCMOUT under received alarm conditions.
RX2MHZ	5	Receiver 2048KHz clock.
BLANK	6	PCMOUT data blanking (Active High). When active,forces PCMOUT data to all ones (AIS).
RXCKOUT	7	128KHz extracted clock.
VCC	8	+5V power supply.
RXCK2MHZ	9	2048 KHz clock recovery signal.
TS1T	10	Time slot input 1 for transmitter
BDT	11	Transmitter data byte deletion flag (Active High).
TS2T	12	Time slot input 2 for transmitter
T+R	13	Transmit positive output AMI data (Active Low).
T-R	14	Transmit negative output AMI data (Active Low).
TTSEL	15	Transmit time slot select When high, pin 10; low pin 12
ALARMIN	16	Alarm input (Active High). When active inhibits insertion of violations into transmitted data.
TX256KHZ	17	Transmitter 256KHz clock.
BIT	18	Transmitter data byte insertionflag (Active High).
PCMIN	19	Transmitter PCM input.
TX2MHZ	20	Transmitter 2048KHz clock.
VSS	21	Ground.
CS	22	Clock seek (Active High). Indicates loss of lock with received data.

PIN DESCRIPTION - XR-T6166 *(continued)*

Name	Pin	Description
TS1R	23	Time slot input 1 for receiver.
TS2R	24	Time slot input 2 for receiver.
BDR	25	Receive data byte deletion flag (Active High).
BIR	26	Receive data byte insertion flag (Active High).
RTSEL	27	Receive time slot select. When high, pin 23; when low pin 24.
PCMOUT	28	Received PCM output data.64 kBPS data

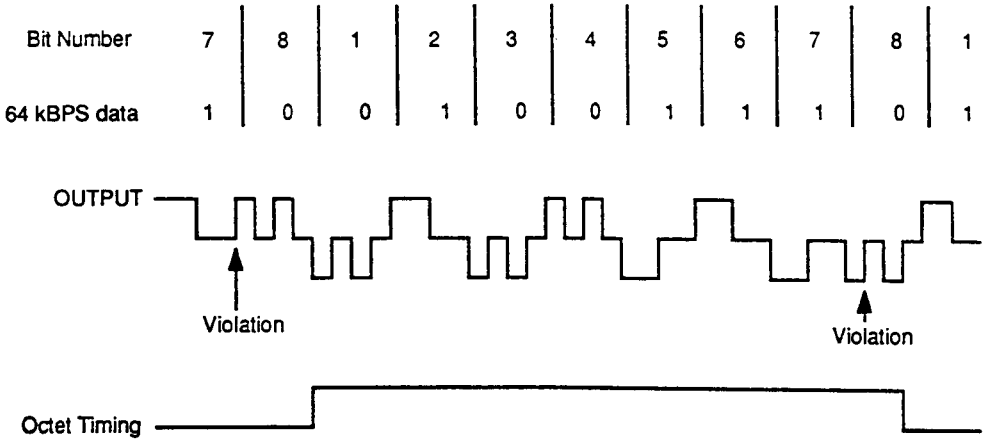
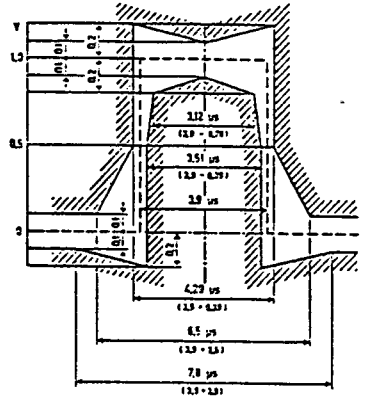


Figure 1. Transmitter Code Conversion for 64 kBPS Bipolar Line Signal.



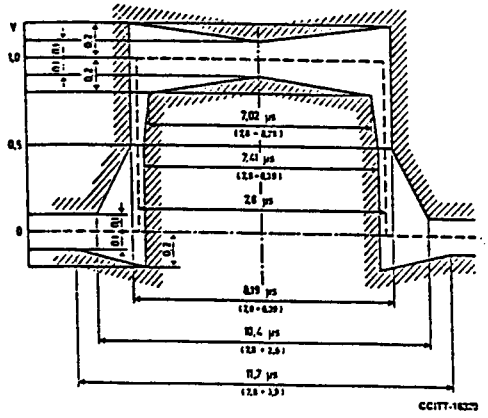


Figure 2. Pulse Masks of the 64 kBPS Codirectional Interface

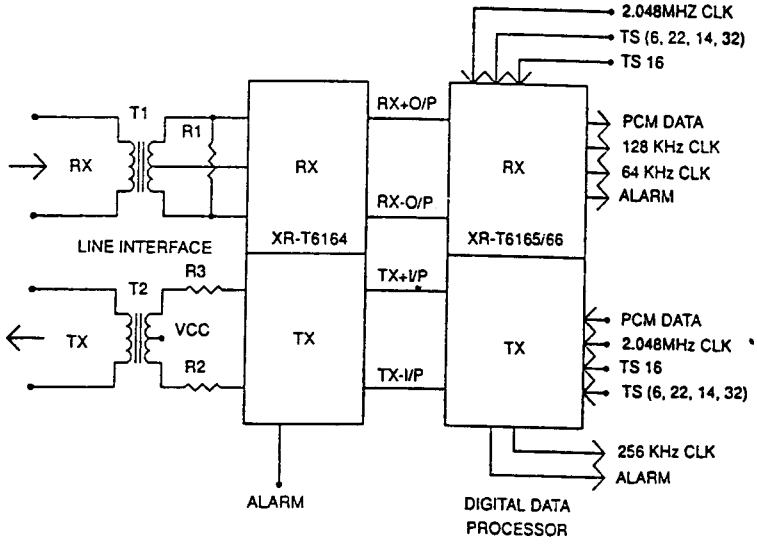


Figure 3. Digital Data Processor Application.

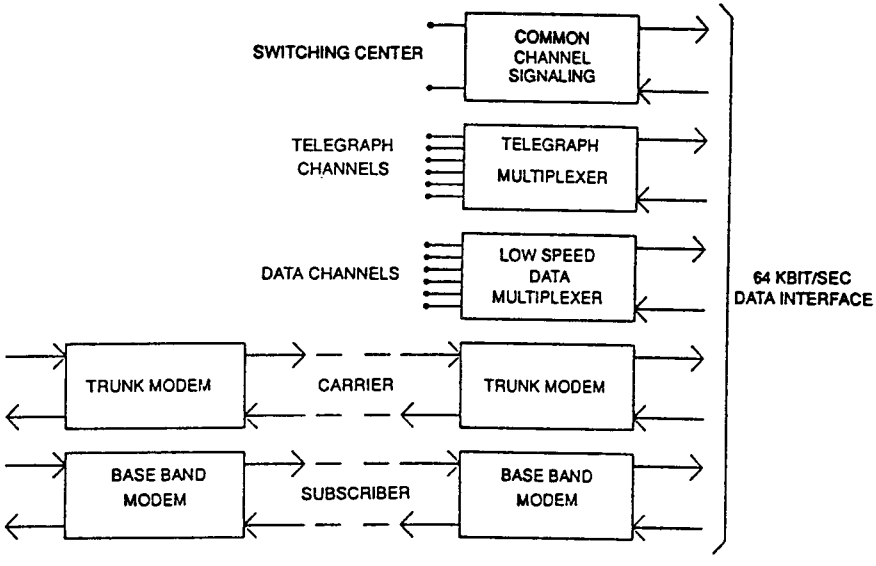


Figure 4. Digital Data Processor Application.

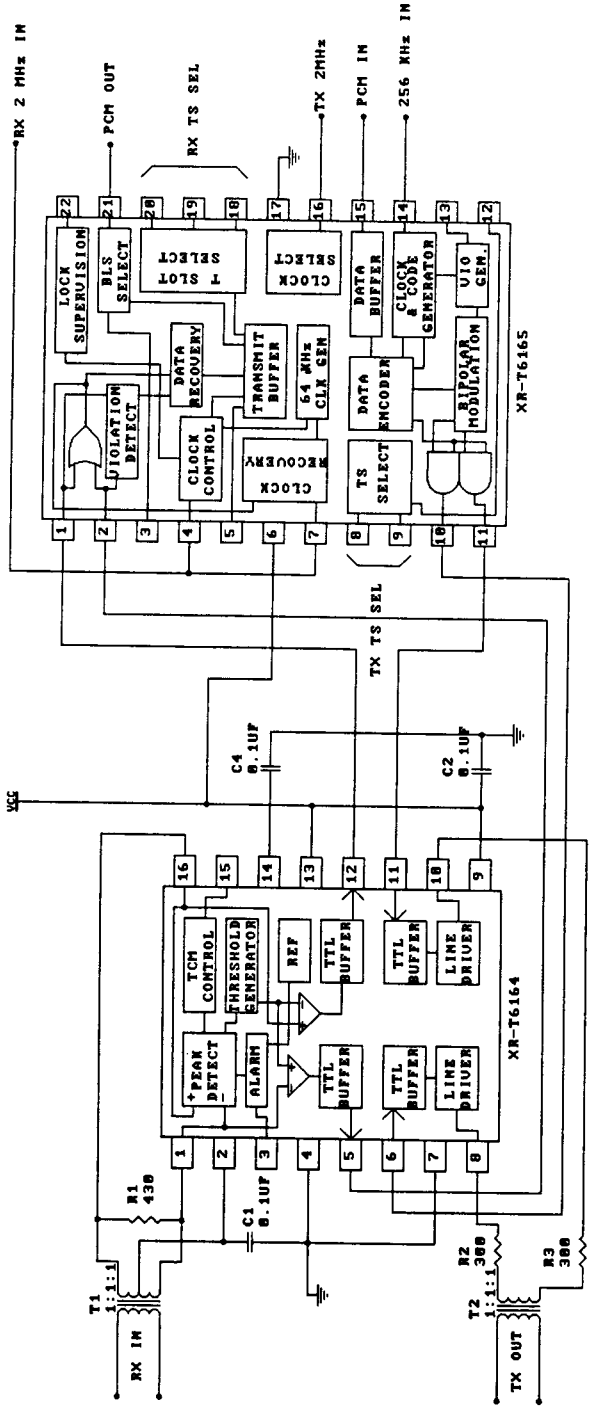


Figure 5. Typical 64 kbit/s Data Interface.

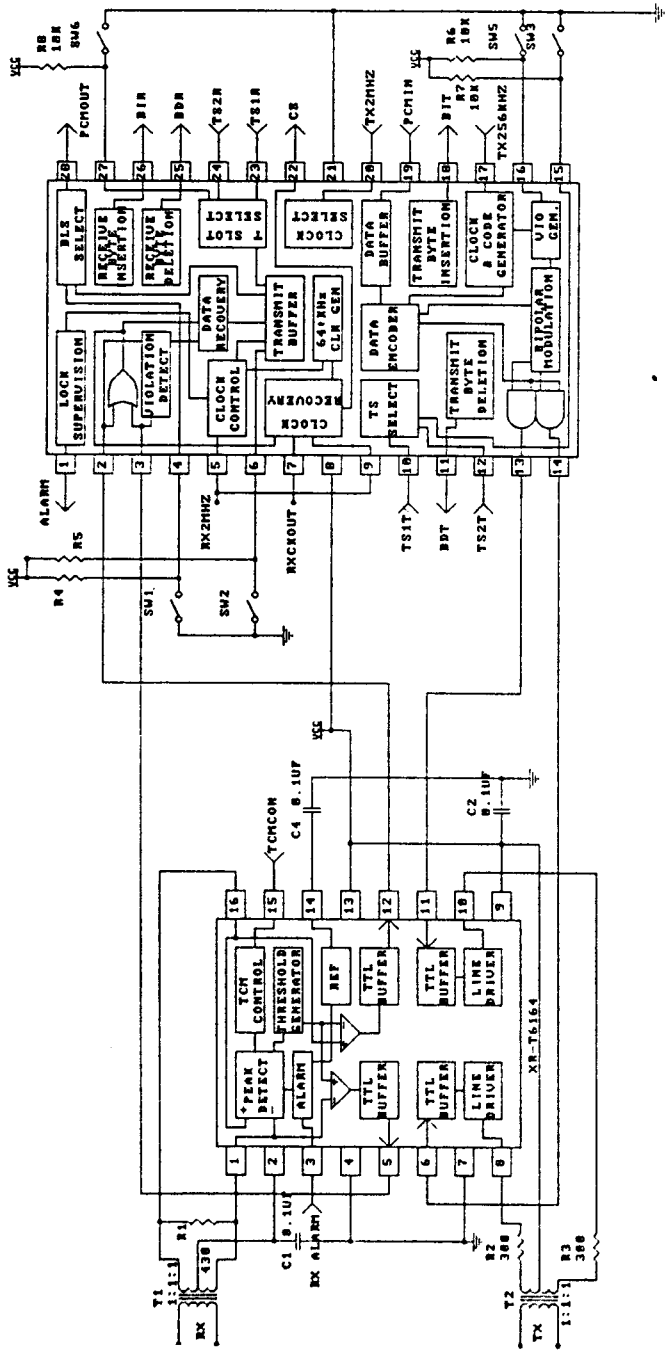


Figure 6. Typical Application Diagram for XR-T6166.