DIGITAL DELAY LINE
SERIES 0450
CMOS
DELAY MODULE
5 TAP

TECHNICAL INFORMATION

TEST CONDITIONS

Pulse Voltage	5.0 Volts
Rise Time	6.0 Nsec (10%-90%)
Pulse Width	1.2 x Total Delay
Pulse Period	4 x Pulse Width
Supply Current, I_{CCL}	10.0 Milliamps max.
Supply Voltage, V_{CC}	5.0 Volts
Ambient Temperature	25°C

PERFORMANCE CHARACTERISTICS

Delay Tolerance From Input To Tap
± 2 Nsec or 5% whichever is greater
Delay Tolerance From Tap To Tap
± 2 Nsec or 7% whichever is greater
Performance Characteristics apply at above listed Test Conditions.

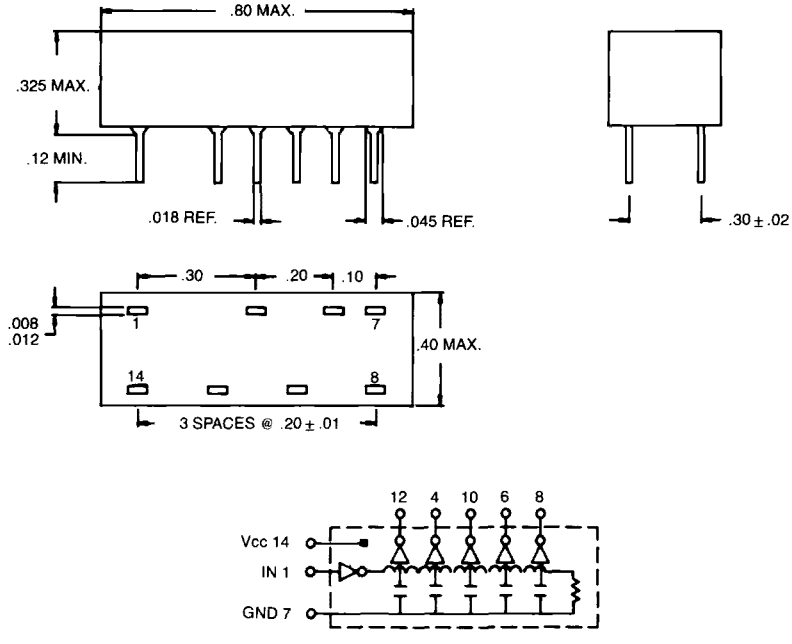
ELECTRICAL CHARACTERISTICS

Supply Voltage, V_{CC}
4.75 to 5.25 Volts
Logic 1 Output Voltage
4.0 Volts min.
Logic 0 Output Voltage
0.3 Volts max.
Input Leakage Current
± 1 Microamp max.
Operating Temperature Range
– 40°C To 85°C
Temperature Coefficient Of Total Delay
500PPM/°C Typical
Minimum Input Pulse Width
40% Of Total Delay
Maximum Duty Cycle
50%

DRIVE CAPABILITIES

10 LSTTL Loads min.

—Compatible with 5V CMOS and TTL circuits
—Diode protection on input
—Low power consumption
—Low input current
—Other delays and tolerances upon request



Part Number	Total Delay 1, 3,	Delay/Tap 1, 3	Rise Time 2, 3
0450-0075-02	75NS	15NS	6NS
0450-0100-02	100NS	20NS	6NS
0450-0125-02	125NS	25NS	6NS
0450-0150-02	150NS	30NS	6NS
0450-0175-02	175NS	35NS	6NS
0450-0200-02	200NS	40NS	6NS

1 Delays measured at 50% of the pulse on the leading edge only.
2 Rise times measured from 10% to 90% of the pulse.
3 Measured with No Load on Taps.

Specifications Subject To Change Without Notice