MOTOROLA

QUAD ANALOG SWITCH/QUAD MULTIPLEXER

The MC14066B consists of four independent switches capable of controlling either digital or analog signals. This quad bilateral switch is useful in signal gating, chopper, modulator, demodulator and CMOS logic implementation.

The MC14066B is designed to be pin-for-pin compatible with the MC14016B, but has much lower ON resistance. Input voltage swings as large as the full supply voltage can be controlled via each independent control input.

- Triple Diode Protection on All Control Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Linearized Transfer Characteristics
- Low Noise — 12 nV/$\sqrt{\text{Cycle}}$, f $\geq$ 1.0 kHz typical
- Pin-for-Pin Replacement for CD4016, CD4016, MC14016B
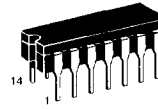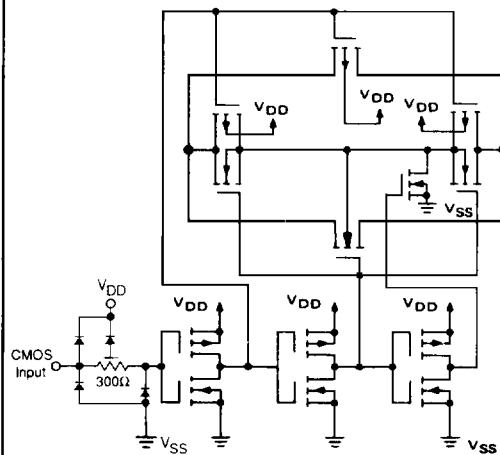- For Lower R_{ON}, Use The HC4066 High-Speed CMOS Device

L SUFFIX
CERAMIC
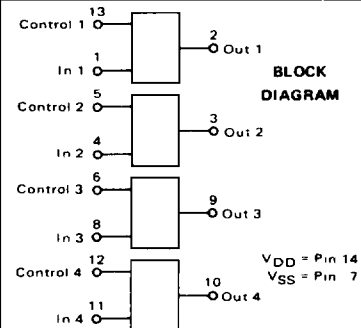CASE 632
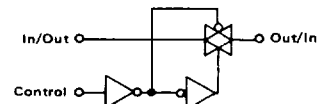
P SUFFIX
PLASTIC
CASE 646

D SUFFIX
SOIC
CASE 751A

ORDERING INFORMATION

MC14XXXBCP   Plastic
MC14XXXBCL   Ceramic
MC14XXXBD   SOIC

T_A = -55° to 125°C for all packages.

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	-0.5 to $+18.0$	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}	Input Current (DC or Transient), per Control Pin	± 10	mA
I_{sw}	Switch Through Current	± 25	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	-65 to $+150$	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P and D/DW" Packages: -7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: -12 mW/°C From 100°C To 125°C

BLOCK DIAGRAM

Control 1 (13), In 1 (1) → Out 1 (2)
Control 2 (5), In 2 (4) → Out 2 (3)
Control 3 (6), In 3 (8) → Out 3 (9)
Control 4 (12), In 4 (11) → Out 4 (10)

V_{DD} = Pin 14
V_{SS} = Pin 7

CIRCUIT SCHEMATIC
(1/4 OF DEVICE SHOWN)

LOGIC DIAGRAM AND TRUTH TABLE
(1/4 OF DEVICE SHOWN)

Control	Switch
0 = V_{SS}	OFF
1 = V_{DD}	ON

Logic Diagram Restrictions
$V_{SS} \leq V_{in} \leq V_{DD}$
$V_{SS} \leq V_{out} \leq V_{DD}$

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Test Conditions	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})											
Power Supply Voltage Range	V_{DD}	—		3.0	18	3.0	—	18	3.0	18	V
Quiescent Current Per Package	I_{DD}	5.0	Control Inputs: $V_{in} = V_{SS}$ or V_{DD}, Switch I/O: $V_{SS} \leqslant V_{I/O} \leqslant V_{DD}$, and $\Delta V_{switch} \leqslant 500$ mV**	—	0.25	—	0.005	0.25	—	7.5	μA
		10		—	0.5	—	0.010	0.5	—	15	
		15		—	1.0	—	0.015	1.0	—	30	
Total Supply Current (Dynamic Plus Quiescent, Per Package)	$I_{D(AV)}$	5.0	$T_A = 25°C$ only The channel component, $(V_{in} − V_{out})/R_{on}$, is not included.)			Typical	(0.07 μA/kHz)f + I_{DD}				μA
		10					(0.20 μA/kHz)f + I_{DD}				
		15					(0.36 μA/kHz)f + I_{DD}				
CONTROL INPUTS (Voltages Referenced to V_{SS})											
Low-Level Input Voltage	V_{IL}	5.0	R_{on} = per spec, I_{off} = per spec	—	1.5	—	2.25	1.5	—	1.5	V
		10		—	3.0	—	4.50	3.0	—	3.0	
		15		—	4.0	—	6.75	4.0	—	4.0	
High-Level Input Voltage	V_{IH}	5.0	R_{on} = per spec, I_{off} = per spec	3.5	—	3.5	2.75	—	3.5	—	V
		10		7.0	—	7.0	5.50	—	7.0	—	
		15		11	—	11	8.25	—	11	—	
Input Leakage Current	I_{in}	15	$V_{in} = 0$ or V_{DD}	—	±0.1	—	±0.00001	±0.1	—	±1.0	μA
Input Capacitance	C_{in}	—		—	—	—	5.0	7.5	—	—	pF
SWITCHES IN AND OUT (Voltages Referenced to V_{SS})											
Recommended Peak-to-Peak Voltage Into or Out of the Switch	$V_{I/O}$	—	Channel On or Off	0	V_{DD}	0	—	V_{DD}	0	V_{DD}	V_{p-p}
Recommended Static or Dynamic Voltage Across the Switch** (Figure 1)	ΔV_{switch}	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V_{OO}	—	$V_{in} = 0$ V, No Load	—	—	—	10	—	—	—	μV
ON Resistance	R_{on}	5.0	$\Delta V_{switch} \leqslant 500$ mV**, $V_{in} = V_{IL}$ or V_{IH} (Control), and $V_{in} = 0$ to V_{DD} (Switch)	—	800	—	250	1050	—	1200	Ω
		10		—	400	—	120	500	—	520	
		15		—	220	—	80	280	—	300	
ΔON Resistance Between Any Two Channels in the Same Package	ΔR_{on}	5.0		—	70	—	25	70	—	135	Ω
		10		—	50	—	10	50	—	95	
		15		—	45	—	10	45	—	65	
Off-Channel Leakage Current (Figure 6)	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	—	±100	—	±0.05	±100	—	±1000	nA
Capacitance, Switch I/O	$C_{I/O}$	—	Switch Off	—	—	—	10	15	—	—	pF
Capacitance, Feedthrough (Switch Off)	$C_{I/O}$	—		—	—	—	0.47	—	—	—	pF

#Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.
**For voltage drops across the switch (ΔV_{switch}) >600 mV (>300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

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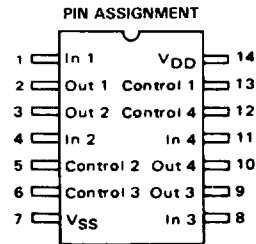**ELECTRICAL CHARACTERISTICS*** ($C_L = 50$ pF, $T_A = 25°C$ unless otherwise noted.)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ #	Max	Unit
Propagation Delay Times $\quad V_{SS} = 0$ Vdc	t_{PLH}, t_{PHL}					ns
Input to Output ($R_L = 10$ kΩ)						
$\quad t_{PLH}, t_{PHL} = (0.17$ ns/pF$) C_L + 15.5$ ns		5.0	—	20	40	
$\quad t_{PLH}, t_{PHL} = (0.08$ ns/pF$) C_L + 6.0$ ns		10	—	10	20	
$\quad t_{PLH}, t_{PHL} = (0.06$ ns/pF$) C_L + 4.0$ ns		15	—	7.0	15	
Control to Output ($R_L = 1$ kΩ) (Figure 2)						
Output "1" to High Impedance	t_{PHZ}	5.0	—	40	80	ns
		10	—	35	70	
		15	—	30	60	
Output "0" to High Impedance	t_{PLZ}	5.0	—	40	80	ns
		10	—	35	70	
		15	—	30	60	
High Impedance to Output "1"	t_{PZH}	5.0	—	60	120	ns
		10	—	20	40	
		15	—	15	30	
High Impedance to Output "0"	t_{PZL}	5.0	—	60	120	ns
		10	—	20	40	
		15	—	15	30	
Second Harmonic Distortion $\quad V_{SS} = -5$ Vdc	—	5.0	—	0.1	—	%
($V_{in} = 1.77$ Vdc, RMS Centered @ 0.0 Vdc, $R_L = 10$ kΩ, f = 1.0 kHz)						
Bandwidth (Switch ON) (Figure 3) $\quad V_{SS} = -5$ Vdc	—	5.0	—	65	—	MHz
($R_L = 1$ kΩ, $20 \log \frac{V_{out}}{V_{in}} = -3$ dB, $C_L = 50$ pF, $V_{in} = 5$ V_{p-p})						
Feedthrough Attenuation (Switch OFF) $\quad V_{SS} = -5$ Vdc	—	5.0	—	-50	—	dB
($V_{in} = 5$ V_{p-p}, $R_L = 1$ kΩ, $f_{in} = 1.0$ MHz) (Figure 3)						
Channel Separation (Figure 4) $\quad V_{SS} = -5$ Vdc	—	5.0	—	-50	—	dB
($V_{in} = 5$ V_{p-p}, $R_L = 1$ kΩ, $f_{in} = 8.0$ MHz) (Switch A ON, Switch B OFF)						
Crosstalk, Control Input to Signal Output (Figure 5) $\quad V_{SS} = -5$ Vdc	—	5.0	—	300	—	mV_{p-p}
($R_1 = 1$ kΩ, $R_L = 10$ kΩ, Control $t_{TLH} = t_{THL} = 20$ ns)						

*The formulas given are for the typical characteristics only at 25°C
#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

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This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT

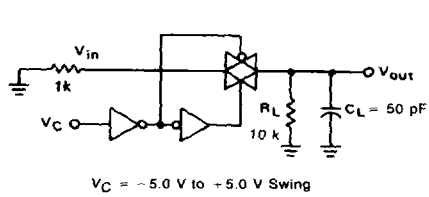|					
1	In 1		V_{DD}	14
2	Out 1		Control 1	13
3	Out 2		Control 4	12
4	In 2		In 4	11
5	Control 2		Out 4	10
6	Control 3		Out 3	9
7	V_{SS}		In 3	8

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FIGURE 1 — ΔV ACROSS SWITCH

FIGURE 2 — TURN-ON DELAY TIME TEST CIRCUIT AND WAVEFORMS

FIGURE 3 — BANDWIDTH AND FEEDTHROUGH ATTENUATION

$V_C = V_{DD}$ for Bandwidth Test
$V_C = V_{SS}$ for Feedthrough Test
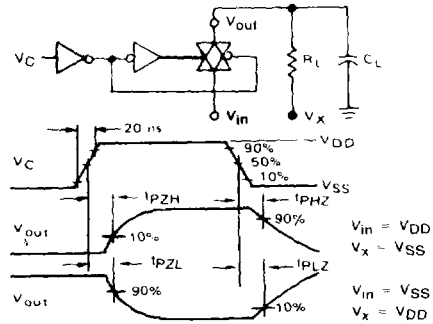
FIGURE 4 — CHANNEL SEPARATION

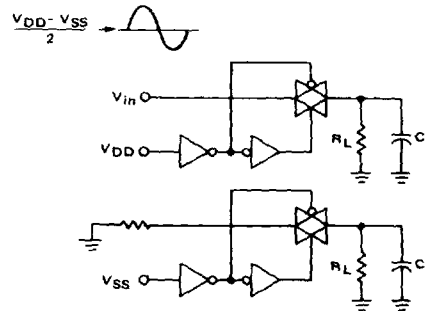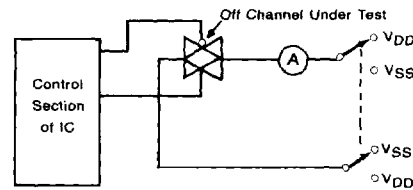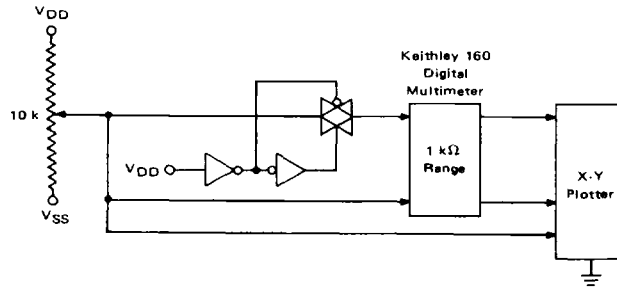FIGURE 5 — CROSSTALK, CONTROL TO OUTPUT

$V_C = -5.0$ V to $+5.0$ V Swing

FIGURE 6 — OFF CHANNEL LEAKAGE

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FIGURE 7 – CHANNEL RESISTANCE (R_ON) TEST CIRCUIT

TYPICAL RESISTANCE CHARACTERISTICS

FIGURE 8 – V_{DD} = 7.5 V, V_{SS} = -7.5 V
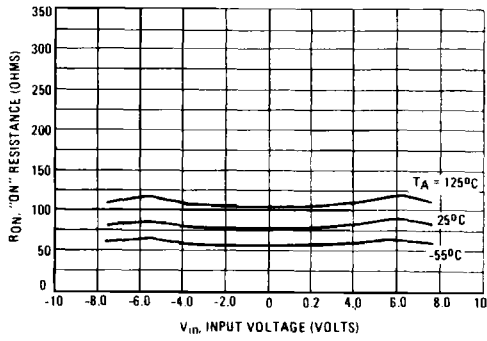
FIGURE 9 – V_{DD} = 5.0 V, V_{SS} = -5.0 V
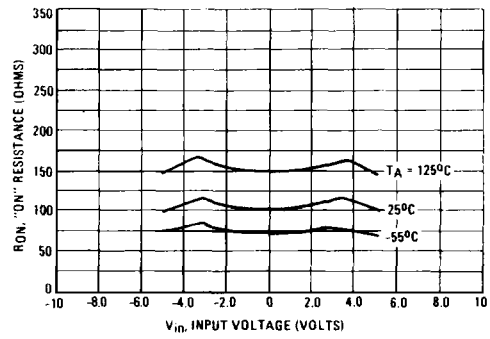
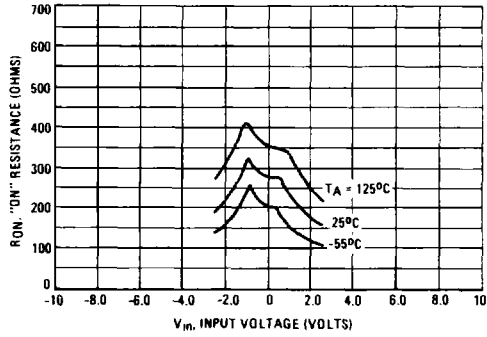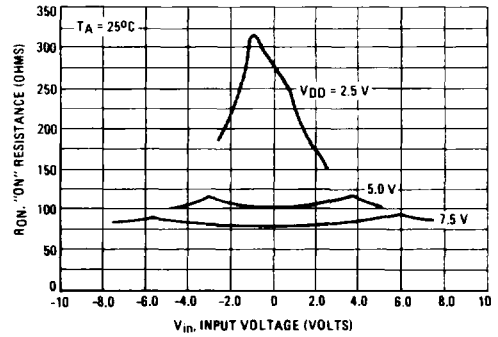FIGURE 10 – V_{DD} = 2.5 V, V_{SS} = -2.5 V

FIGURE 11 – COMPARISON AT 25°C, V_{DD} = -V_{SS}

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APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Switch. The 0-to-5 volt digital control signal is used to directly control a 5 volt peak-to-peak analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, $V_{DD} = +5$ V $=$ logic high at the control inputs; V_{SS} $=$ GND $= 0$ V $=$ logic low.

The maximum analog signal level is determined by V_{DD} and V_{SS}. The analog voltage must not swing higher than V_{DD} or lower than V_{SS}.

The example shows a 5 volt peak-to-peak signal which allows no margin at either peak. If voltage transients above V_{DD} and/or below V_{SS} are anticipated on the analog channels, external diodes (D_x) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{SS} is 18.0 volts. Most parameters are specified up to 15 volts which is the *recommended* maximum difference between V_{DD} and V_{SS}.
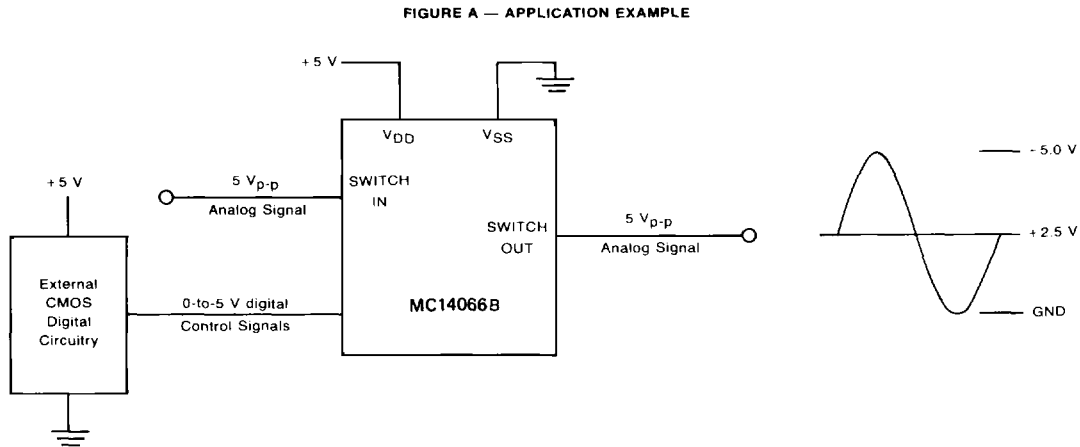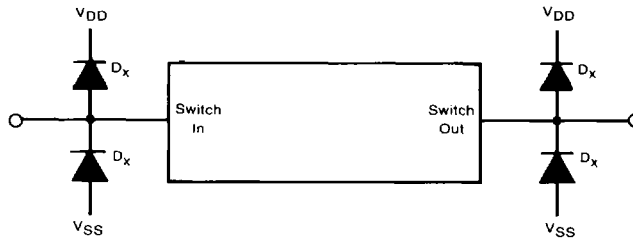
FIGURE A — APPLICATION EXAMPLE

FIGURE B — EXTERNAL GERMANIUM OR SCHOTTKY CLIPPING DIODES