3-STATE HEX INVERTING BUFFER

The HEF40098B is a hex inverting buffer with 3-state outputs. The 3-state outputs are controlled by two enable inputs ($\overline{EO}_4$ and $\overline{EO}_2$). A HIGH on $\overline{EO}_4$ causes four of the six buffer elements to assume a high impedance or OFF-state regardless of the other input conditions and a HIGH on $\overline{EO}_2$ causes the outputs of the remaining two buffer elements to assume a high impedance or OFF-state regardless of the other input conditions.

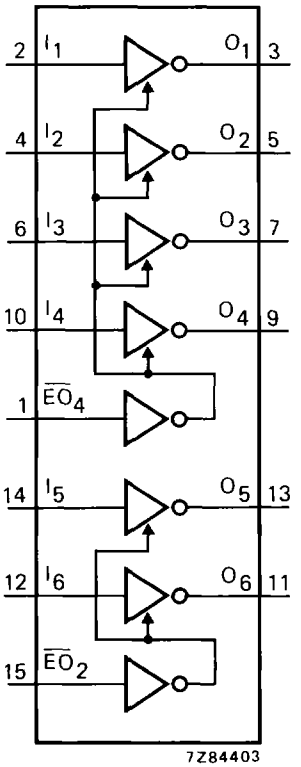

Fig. 1 Functional diagram.

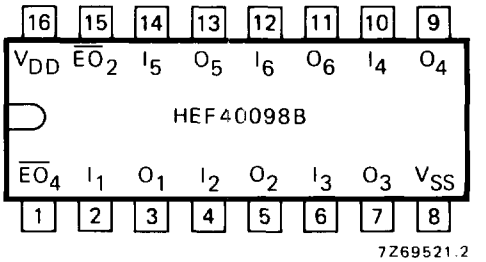

Fig. 2 Pinning diagram.

HEF40098BP(N): 16-lead DIL; plastic (SOT38-1)
HEF40098BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF40098BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

PINNING

I_1 to I_6	buffer inputs
$\overline{EO}_4$, $\overline{EO}_2$	enable inputs (active LOW)
O_1 to O_6	buffer outputs (active LOW)

FAMILY DATA

I_{DD} LIMITS category BUFFERS } see Family Specifications

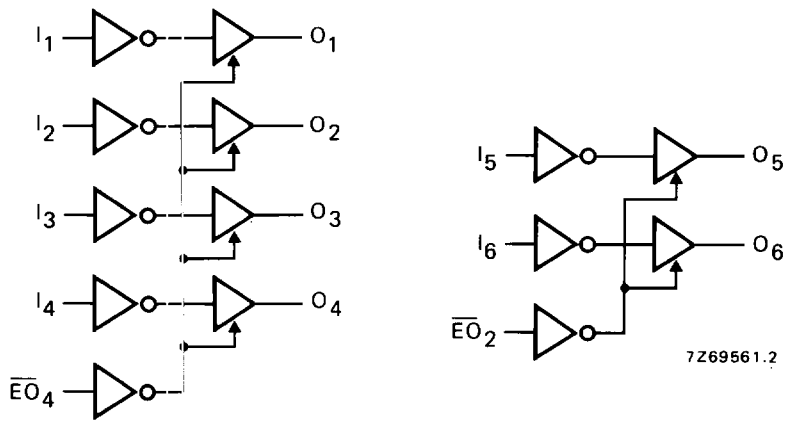

Fig. 3 Logic diagram.

D.C. CHARACTERISTICS

V_{SS} = 0 V

HEF	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C) −40 min.	−40 max.	+25 min.	+25 max.	+85 min.	+85 max.	
Output current HIGH	5	4,6			1,2		1,0		0,8		mA
	10	9,5		$-I_{OH}$	3,8		3,2		2,5		mA
	15	13,5			12,0		10,0		8,0		mA
HIGH	5	2,5		$-I_{OH}$	3,8		3,2		2,5		mA
Output current LOW	4.75		0,4		3,5		2,9		2,3		mA
	10		0,5	I_{OL}	12,0		10,0		8,0		mA
	15		1,5		24,0		20,0		16,0		mA

HEC	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C) −55 min.	−55 max.	+25 min.	+25 max.	+125 min.	+125 max.	
Output current HIGH	5	4,6			1,25		1,0		0,6		mA
	10	9,5		$-I_{OH}$	4,0		3,2		2,1		mA
	15	12,5			12,5		10,0		6,7		mA
HIGH	5	2,5		$-I_{OH}$	4,0		3,2		2,1		mA
Output current LOW	4,75		0,4		3,6		2,9		1,9		mA
	10		0,5	I_{OL}	12,5		10,0		6,7		mA
	15		1,5		25,0		20,0		13,0		mA

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ⩽ 20 ns

	V_{DD} V	symbol	typ.	max.		typical extrapolation formula
Propagation delays						
$I_n \rightarrow O_n$	5		80	160	ns	70 ns + (0,20 ns/pF) C_L
HIGH to LOW	10	t_{PHL}	35	70	ns	31 ns + (0,08 ns/pF) C_L
	15		25	50	ns	22 ns + (0,06 ns/pF) C_L
	5		65	130	ns	50 ns + (0,30 ns/pF) C_L
LOW to HIGH	10	t_{PLH}	30	60	ns	24 ns + (0,13 ns/pF) C_L
	15		25	50	ns	23 ns + (0,05 ns/pF) C_L
Output transition times	5		30	60	ns	15 ns + (0,30 ns/pF) C_L
HIGH to LOW	10	t_{THL}	15	30	ns	10 ns + (0,11 ns/pF) C_L
	15		10	20	ns	7 ns + (0,07 ns/pF) C_L
	5		35	70	ns	10 ns + (0,50 ns/pF) C_L
LOW to HIGH	10	t_{TLH}	20	40	ns	8 ns + (0,24 ns/pF) C_L
	15		15	30	ns	6 ns + (0,18 ns/pF) C_L
3-state propagation delays						
Output disable times						
$\overline{EO}_2$, $\overline{EO}_4 \rightarrow O_n$	5		45	85	ns	
HIGH	10	t_{PHZ}	35	65	ns	
	15		30	60	ns	
	5		65	135	ns	
LOW	10	t_{PLZ}	40	80	ns	
	15		35	70	ns	
Output enable times						
$\overline{EO}_2$, $\overline{EO}_4 \rightarrow O_n$	5		70	140	ns	
HIGH	10	t_{PZH}	35	75	ns	
	15		30	65	ns	
	5		90	185	ns	
LOW	10	t_{PZL}	40	85	ns	
	15		35	70	ns	

	V_{DD} V	typical formula for P (μW)	where
			f_i = input freq. (MHz)
			f_o = output freq. (MHz)
Dynamic power dissipation per package (P)	5	5 000 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	C_L = load cap. (pF)
	10	22 800 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	$\Sigma(f_o C_L)$ = sum of outputs
	15	81 000 f_i + $\Sigma(f_o C_L) \times V_{DD}^2$	V_{DD} = supply voltage (V)