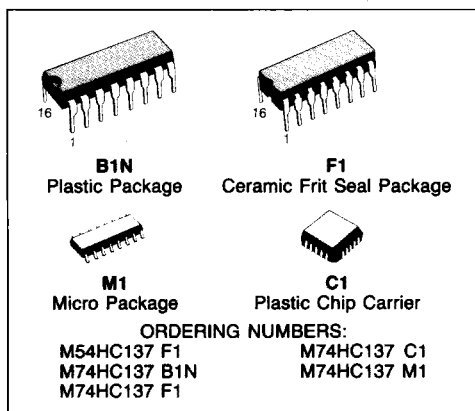


3 TO 8 LINE DECODER/LATCH (INVERTING)

- **HIGH SPEED**
 $t_{PD} = 14 \text{ ns (TYP.) at } V_{CC} = 5 \text{ V}$
- **LOW POWER DISSIPATION**
 $I_{CC} = 4 \mu\text{A (MAX.) at } T_A = 25^\circ\text{C}$
- **HIGH NOISE IMMUNITY**
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- **OUTPUT DRIVE CAPABILITY**
 10 LSTTL LOADS
- **SYMMETRICAL OUTPUT IMPEDANCE**
 $|I_{OH}| = I_{OL} = 4 \text{ mA (MIN.)}$
- **BALANCED PROPAGATION DELAYS**
 $t_{PLH} = t_{PHL}$
- **WIDE OPERATING VOLTAGE RANGE**
 $V_{CC} \text{ (OPR)} = 2 \text{ V to } 6 \text{ V}$
- **PIN AND FUNCTION COMPATIBLE**
 WITH 54/74LS137



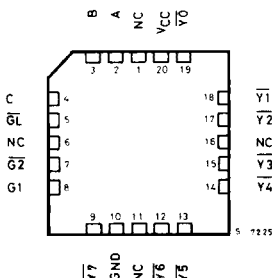
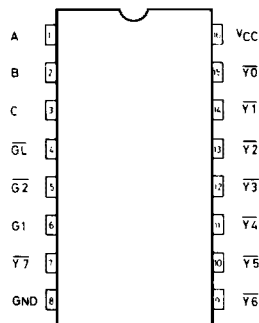
DESCRIPTION

The M54/74HC137 is a high speed CMOS 3 TO 8 LINE DECODER/LATCH (INVERTING) fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption.

This device is a 3 to 8 line decoder with latches on the three address inputs. When $\overline{G_L}$ goes from low to high, the address present at the select inputs (A, B and C) is stored in the latches. As long as $\overline{G_L}$ remains high no address changes will be recognized. Output enable pins $\overline{G_1}$ and $\overline{G_2}$, control the state of the outputs independently of the select or latch-enable inputs. All the outputs are high unless $\overline{G_1}$ and $\overline{G_2}$ are low. The HC137 is ideally suited for the implementation of glitch-free decoders in stored-address applications in bus oriented systems.

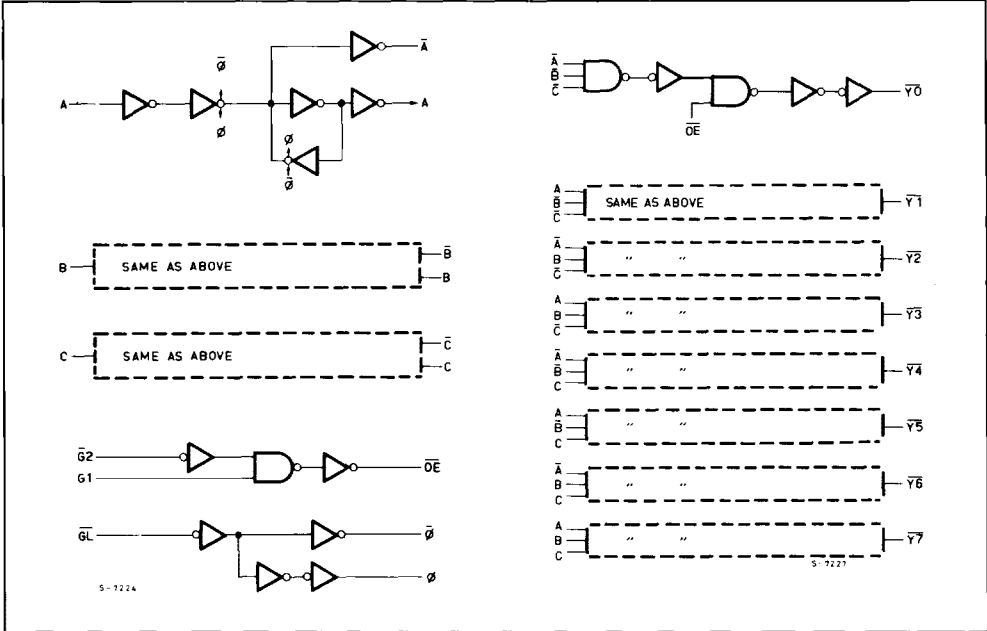
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTIONS (top view)



NC =
No Internal
Connection

LOGIC DIAGRAM



TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT										
GL	G1	G2	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Outputs corresponding to stored address L: all others H							

X: DON'T CARE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to 7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: $\approx$ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	-40 to 85 -55 to 125	°C
t_r, t_f	Input Rise and Fall Time	$V_{CC} \begin{cases} 2 \text{ V} & 0 \text{ to } 1000 \\ 4.5 \text{ V} & 0 \text{ to } 500 \\ 6 \text{ V} & 0 \text{ to } 400 \end{cases}$	ns

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0		1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2	— — —	V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0		— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	V
		4.5	V_{IH} or V_{IL}		4.4	4.5	—	4.4	—	4.4	
		6.0			5.9	6.0	—	5.9	—	5.9	
		4.5 6.0			4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	

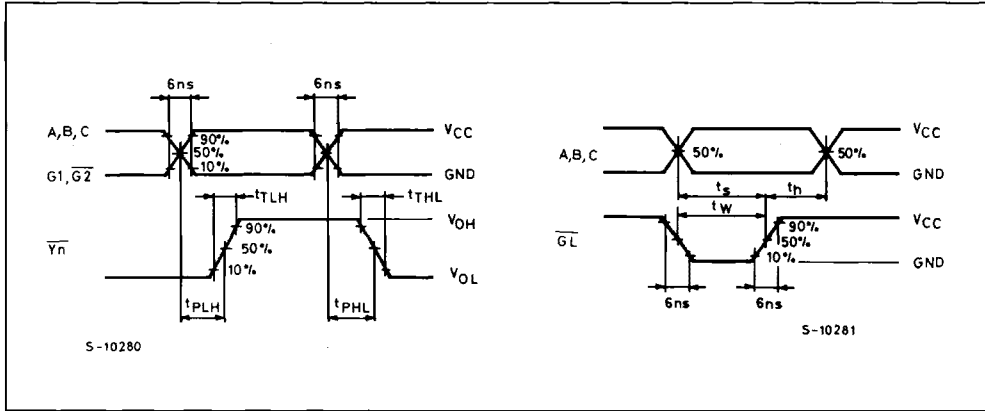
DC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	V _{CC}	Test Condition		T _A = 25°C 54HC and 74HC			– 40 to 85°C 74HC		– 55 to 125°C 54HC		Unit	
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
V _{OL}	Low Level Output Voltage	2.0	V _I	I _O	—	0.0	0.1	—	0.1	—	0.1	V	
		4.5	V _{IH} or V _{IL}	20 μA		0.0	0.1	—	0.1	—	0.1		
		6.0		0.0		0.1	—	0.1	—	0.1			
		4.5		4.0 mA		—	0.17	0.26	—	0.33	—		0.40
		6.0		5.2 mA		—	0.18	0.26	—	0.33	—		0.40
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND		—	—	±0.1	—	±1.0	—	±1.0	μA	
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND		—	—	4	—	40	—	80	μA	

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input t_r = t_f = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		Min.	Typ.	Max.	
t _{TLH} t _{THL}	Output Transition Time		4	8	ns
t _{PLH} t _{PHL}	Propagation Delay Time (G1 - Y _n)		14	23	ns
t _{PLH} t _{PHL}	Propagation Delay Time (G2 - Y _n)		17	26	ns
t _{PLH} t _{PHL}	Propagation Delay Time (G _L - Y _n)		24	38	ns
t _{PLH} t _{PHL}	Propagation Delay Time (A,B,C - Y _n)		21	34	ns

SWITCHING CHARACTERISTICS TEST WAVEFORM



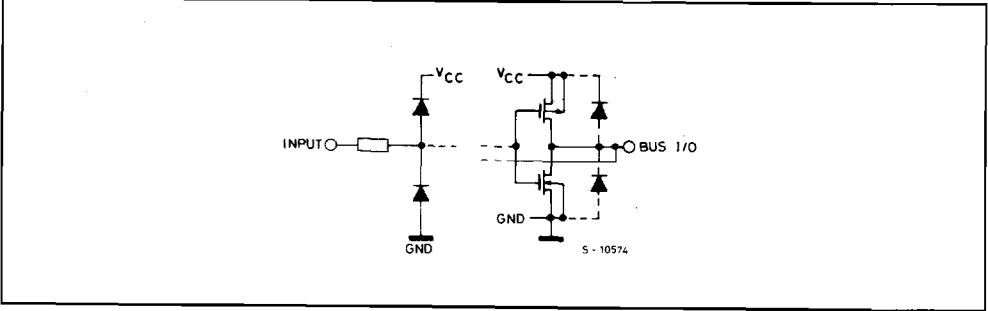
AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input t_r = t_f = 6ns)

Symbol	Parameter	V _{CC}	Test Condition	T _A = 25°C 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t _{TLH} t _{THL}	Output Transition Time	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t _{PLH} t _{PHL}	Propagation Delay Time (G1-Ȳn)	2.0 4.5 6.0		— — —	72 18 15	145 29 25	— — —	180 36 31		220 44 38	ns
t _{PLH} t _{PHL}	Propagation Delay Time (G2-Ȳn)	2.0 4.5 6.0		— — —	80 20 17	155 31 26	— — —	195 39 33		235 47 40	ns
t _{PLH} t _{PHL}	Propagation Delay Time (GL - Ȳn)	2.0 4.5 6.0		— — —	112 28 24	220 44 37	— — —	275 55 47		330 66 56	ns
t _{PLH} t _{PHL}	Propagation Delay Time (A,B,C - Ȳn)	2.0 4.5 6.0		— — —	100 25 21	195 39 33	— — —	245 49 42		295 59 50	ns
t _{W(L)}	Minimum Pulse Width (GL)	2.0 4.5 6.0		— — —	30 8 7	75 15 13	— — —	95 19 16		110 22 19	ns
t _s	Minimum Set-up Time (A,B,C GL)	2.0 4.5 6.0		— — —	10 2 2	50 10 9	— — —	65 13 11		75 15 13	ns
t _h	Minimum Hold Time (A,B,C GL)	2.0 4.5 6.0		— — —	5 0 0	25 5 5	— — —	30 6 6	— — —	40 8 7	ns
C _{IN}	Input Capacitance			—	5	10	—	10		10	pF
C _{PD} (*)	Power Dissipation Capacitance			—	65	—	—	—			pF

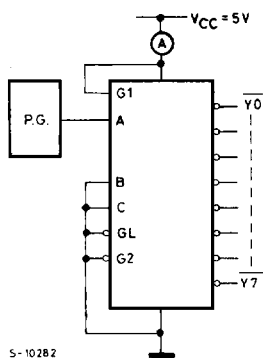
Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit)

Average operating current can be obtained by the following: I_{CC(opr)} = C_{PD} · V_{CC} · f_{IN} + I_{CC}

INPUT AND OUTPUT EQUIVALENT CIRCUIT



TEST CIRCUIT I_{CC} (Opr.)



INPUT TRANSITION TIME IS THE SAME AS THAT IN CASE OF SWITCHING CHARACTERISTICS TEST

TYPICAL APPLICATION

