PCMCIA Flash Memory Card - 256 KILOBYTE through 5 MEGABYTE (Intel/Catalyst based)

GENERAL DESCRIPTION

WEDC's FLG Series Flash memory cards offer low/medium density linear Flash solid state storage solutions for code and data storage, high performance disk emulation and execute in place (XIP) applications in mobile PC and dedicated (embedded) equipment.

FLG series cards conform to PCMCIA international standard.

The card's control logic provides the system interface and controls the internal Flash memories. Card can be read/written in byte-wide or word-wide mode which allows for flexible integration into various systems. Combined with file management software, such as Flash Translation Layer (FTL), FLG Flash cards provide removable high-performance disk emulation.

The FLG series cards contain separate 2kB EEPROM memory for Card Information Structure (CIS) which can be used for easy identification of card characteristics.

The WEDC FLG series is based on Intel/Catalyst 28F010 or 28F020 Flash memories.

Note: Standard options include attribute memory. Cards without attribute memory are available. Cards are also available with or without a hardware write protect switch.

FEATURES

- Low cost Low/Medium Density Linear Flash Card
- Supports 5V systems with 12V V_{PP}.
- Based on Intel CMOS Components
- Fast Read Performance - 150ns Maximum Access Time
- x8/ x16 Data Interface
- Quick-Pulse Programming Algorithm - typical 10µs Byte-Program
- 100,000 Erase/Program Cycles
- PC Card Standard Type I Form Factor

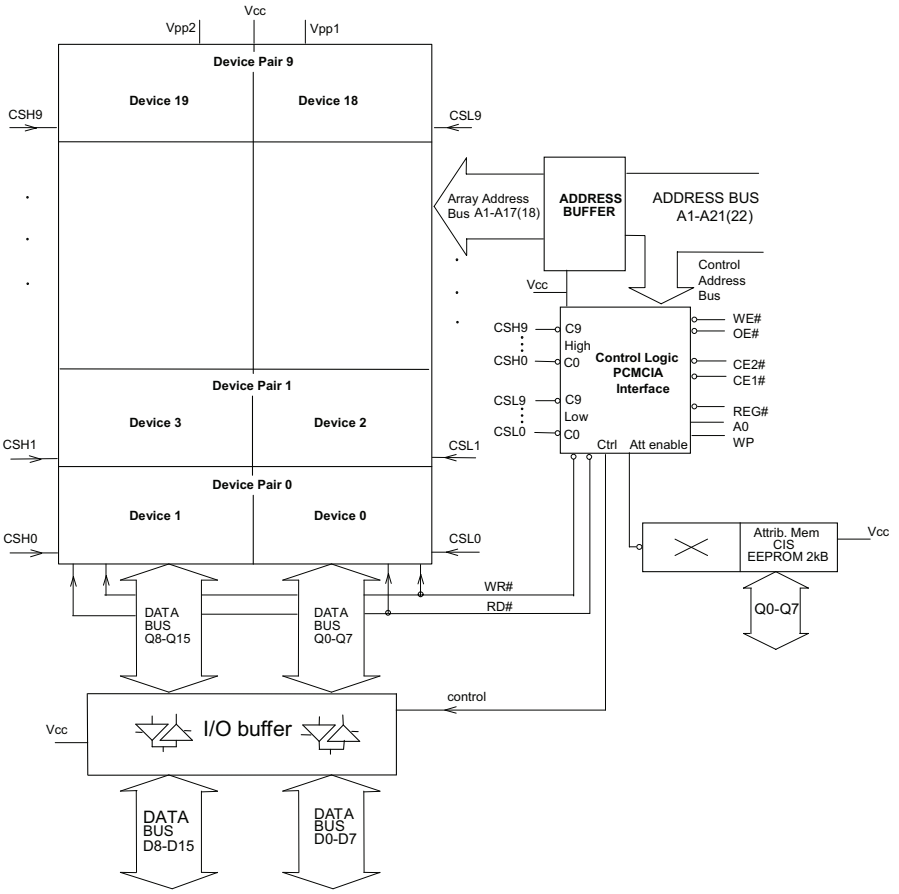
ARCHITECTURE OVERVIEW

WEDC's FLG series is designed to support from 2 to 20, 1Mb or 2MB components, providing a wide range of density options. Cards are based on the 28F010 (1Mb) or 28F020 components which work with 5V V_{CC}/12V V_{PP} applications. Device codes are **B4**h and **BD**h respectively (Manufacture ID **89** for Intel and **31** for Catalyst). Systems should be able to recognize all the codes. Cards utilizing the1Mb components provide densities ranging from 256KB to 2.5MB in 256KB increments, cards utilizing 2Mb components provide densities ranging from 512KB to 5MB in 512KB increments.

In support of the PC Card 95 standard for word wide access devices are paired. Write, read and erase operations can be performed as either a word or byte wide operation . By multiplexing A0, CE1 and CE2, 8-bit hosts can access all data on data lines DQ0 - DQ7. The FLG series cards conform to the PC Card Standard (PCMCIA) and JEIDA, providing electrical and physical compatibility. The PC Card form factor offers an industry standard pinout and mechanical outline, allowing density upgrades without system design changes.

WEDC's standard cards are shipped with WEDC's Logo. Cards are also available with blank housings (no Logo). The blank housings are available in both a recessed (for label) and flat housing. Please contact WEDC sales representative for further information on Custom artwork.

BLOCK DIAGRAM

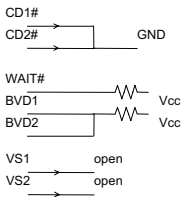


SUPPORTED COMPONENTS (max 20 X):

28F010-max 2.5MB

28F020-max 5MB

Device type	Manuf ID Intel/Catalyst	Device ID
28F010	89H / 31H	$B4_H$
28F020	89H / 31H	BD_H



PINOUT

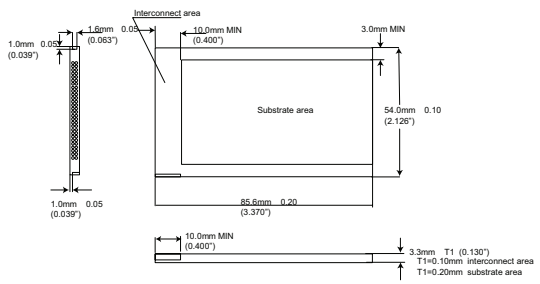
Pin	Signal name	I/O	Function	Active
1	GND		Ground	
2	DQ3	I/O	Data bit 3	
3	DQ4	I/O	Data bit 4	
4	DQ5	I/O	Data bit 5	
5	DQ6	I/O	Data bit 6	
6	DQ7	I/O	Data bit 7	
7	CE1#	I	Card enable 1	LOW
8	A10	I	Address bit 10	
9	OE#	I	Output enable	LOW
10	A11	I	Address bit 11	
11	A9	I	Address bit 9	
12	A8	I	Address bit 8	
13	A13	I	Address bit 13	
14	A14	I	Address bit 14	
15	WE#	I	Write Enable	LOW
16	RDY/BSY#	O	Ready/Busy	N.C.
17	V_{CC}		Supply Voltage	
18	$V_{PP}1$		Prog. Voltage	
19	A16	I	Address bit 16	
20	A15	I	Address bit 15	
21	A12	I	Address bit 12	
22	A7	I	Address bit 7	
23	A6	I	Address bit 6	
24	A5	I	Address bit 5	
25	A4	I	Address bit 4	
26	A3	I	Address bit 3	
27	A2	I	Address bit 2	
28	A1	I	Address bit 1	
29	A0	I	Address bit 0	
30	DQ0	I/O	Data bit 0	
31	DQ1	I/O	Data bit 1	
32	DQ2	I/O	Data bit 2	
33	WP	O	Write Potect	HIGH
34	GND		Ground	

Pin	Signal name	I/O	Function	Active
35	GND		Ground	
36	CD1#	O	Card Detect 1	LOW
37	DQ11	I/O	Data bit 11	
38	DQ12	I/O	Data bit 12	
39	DQ13	I/O	Data bit 13	
40	DQ14	I/O	Data bit 14	
41	DQ15	I	Data bit 15	
42	CE2#	I	Card Enable 2	LOW
43	VS1	O	Voltage Sense 1	N.C.
44	RFU		Reserved	
45	RFU		Reserved	
46	A17	I	Address bit 17	256KB(2)
47	A18	I	Address bit 18	512KB(2)
48	A19	I	Address bit 19	1MB(2)
49	A20	I	Address bit 20	2MB(2)
50	A21	I	Address bit 21	4MB(2,3)
51	V_{CC}		Supply Voltage	
52	$V_{PP}2$		Prog. Voltage	
53	A22	I	Address bit 22	8MB(2,3)
54	A23	I	Address bit 23	N.C.
55	A24	I	Address bit 24	N.C.
56	A25	I	Address bit 25	N.C.
57	VS2	O	Voltage Sense 2	N.C.
58	RST	I	Card Reset	N.C.
59	Wait#	O	Extended Bus cycle	LOW(1)
60	RFU		Reserved	
61	REG#	I	Attrib Mem Select	
62	BVD2	O	Bat. Volt. Detect 2	(1)
63	BVD1	O	Bat. Volt. Detect 1	(1)
64	DQ8	I/O	Data bit 8	
65	DQ9	I/O	Data bit 9	
66	DQ10	O	Data bit 10	
67	CD2#	O	Card Detect 2	LOW
68	GND		Ground	

Notes:

1. WAIT#, BVD1 and BVD2 are driven high for compatibility
2. Shows density for which specified address bit is MSB. Higher order address bits are no connects (i.e. 4MB A21 is MSB A22 - A25 are NC).
3. For the 3MB card the memory will wrap at the 4MB boundary, for the 5MB card the memory will wrap at the 8MB boundary.

MECHANICAL



CARD SIGNAL DESCRIPTION

Symbol	Type	Name and Function
A_0 - A_{25}	INPUT	**ADDRESS INPUTS:** A_0 through A_{25} enable direct addressing of up to 64MB of memory on the card. Signal A_0 is not used in word access mode. The memory will wrap at the card density boundary (see PINOUT, note 3). The system should not try to access memory beyond the card density. A_{25} is the most significant bit. A_{23} - A_{25} are not connected.
DQ_0 - DQ_{15}	INPUT/OUTPUT	**DATA INPUT/OUTPUT:** DQ_0 THROUGH DQ_{15} constitute the bi-directional databus. DQ_0 - Dq_7 constitute the lower (even) byte and DQ_8 - DQ_{15} the upper (odd) byte. DQ_{15} is the MSB.
$CE_{1\#}$, $CE_{2\#}$	INPUT	**CARD ENABLE 1 AND 2:** CE_1 enables even byte accesses, CE_2 enables odd byte accesses. Multiplexing A_0, CE_1 and CE_2 allows 8-bit hosts to access all data on DQ_0 - DQ_7.
OE#	INPUT	**OUTPUT ENABLE:** Active low signal gating read data from the memory card.
WE#	INPUT	**WRITE ENABLE:** Active low signal gating write data to the memory card.
RDY/BSY#	N.C.	**READY/BUSY OUTPUT:** Indicates status of internally timed erase or program algorithms. This signal is not connected.
$CD_{1\#}$, $CD_{2\#}$	OUTPUT	**CARD DETECT 1 and 2:** Provide card insertion detection. These signals are connected to ground internally on the memory card. The host shall monitor these signals to detect card insertion (pulled-up on host side).
WP	OUTPUT	**WRITE PROTECT:** Write protect reflects the status of the Write Protect switch on the memory card. WP set to high = write protected, providing internal hardware write lockout to the Flash array.If card does not include optional write protect switch, this signal will be pulled low internally indicating write protect = "off".
V_{PP1}		**PROGRAM/ERASE POWER SUPPLY:** Provides programming voltages 12.0V for lower byte (D_0 - D_7) memory components.
V_{PP2}		**PROGRAM/ERASE POWER SUPPLY:** Provides programming voltages 12.0V for lower byte (D_8 - D_{15}) memory components.
V_{CC}		**CARD POWER SUPPLY:** 5.0V
GND		**CARD GROUND**
REG#	INPUT	**ATTRIBUTE MEMORY SELECT : Active low signal, enables access to Attribute Memory Plane, occupied by Card Information Structure and Card Registers.**
RST#	N.C.	**RESET:** Active high signal for placing card in Power-on default state. This signal is not connected.
WAIT#	OUTPUT	**WAIT:** This signal is pulled high internally for compatibility. No wait states are generated.
BVD_1, BVD_2	OUTPUT	**BATTERY VOLTAGE DETECT:** These signals are pulled high to maintain SRAM card compatibility.
VS_1, VS_2	OUTPUT	**VOLTAGE SENSE:** Notifies the host socket of the card's V_{CC} requirements. VS_1 and VS_2 are open to indicate a 5V card has been inserted.
RFU		RESERVED FOR FUTURE USE
N.C.		**NO INTERNAL CONNECTION TO CARD:** pin may be driven or left floating

FUNCTIONAL TRUTH TABLE

READ function						**Common Memory**			**Attribute Memory**		
Function Mode	$CE_{2\#}$	$CE_{1\#}$	A_0	OE#	WE#	**REG#**	**D_{15}-D_8**	**D_7-D_0**	**REG#**	**D_{15}-D_8**	**D_7-D_0**
Standby Mode	H	H	X	X	X	X	High-Z	High-Z	X	High-Z	High-Z
Byte Access (8 bits)	H	L	L	L	H	H	High-Z	Even-Byte	L	High-Z	Even-Byte
	H	L	H	L	H	H	High-Z	Odd-Byte	L	High-Z	Not Valid
Word Access (16 bits)	L	L	X	L	H	H	Odd-Byte	Even-Byte	L	Not Valid	Even-Byte
Odd-Byte Only Access	L	H	X	L	H	H	Odd-Byte	High-Z	L	Not Valid	High-Z
WRITE function*											
Standby Mode	H	H	X	X	X	X	X	X	X	X	X
Byte Access (8 bits)	H	L	L	H	L	H	X	Even-Byte	L	X	Even-Byte
	H	L	H	H	L	H	X	Odd-Byte	L	X	X
Word Access (16 bits)	L	L	X	H	L	H	Odd-Byte	Even-Byte	L	X	Even-Byte
Odd-Byte Only Access	L	H	X	H	L	H	Odd-Byte	X	L	X	X

* Require proper programming voltages ($V_{pp}1$, $V_{pp}2$). Program or Erase with an invalid V_{pp} should not be attempted.

ABSOLUTE MAXIMUM RATINGS(2)

Operating Temperature TA (ambient)	
Commercial	0°C to +60 °C
Industrial	-40°C to +85 °C
Storage Temperature	
Commercial	-30°C to +80 °C
Industrial	-40°C to +85 °C
Voltage on any pin relative to V_{SS}	-0.5V to V_{CC}+0.5V
V_{CC} supply Voltage relative to V_{SS}	-0.5V to +7.0V

Note: Stress greater than those listed under "Absolute Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS(1)

Sym	Parameter	Density	Notes	Typ(4)	Max	Units	Test Conditions
I_{CCR}	V_{CC} Read Current	All		10	30	mA	V_{CC} = V_{CC} max tcycle = 150ns, CMOS levels
I_{CCW}	V_{CC} Program Current	All	V_{PP} = 12V	1.0	10	mA	Programming in Progress
I_{PPW}	V_{CC} Program Current	All	V_{PP} = 12V	8.0	30	mA	V_{PP}=V_{PP}H Programming in Progress
I_{CCE}	V_{CC} Erase Current	All	V_{PP} = 12V	5.0	15	mA	Erasure in Progress
I_{PPE}	V_{PP} Erase Current	All	V_{PP} = 12V	10	30	mA	V_{PP}=V_{PP}H Erasure in Progress
I_{CCS} (CMOS)	V_{CC} Standby Current	256KB				µA	V_{CC} = V_{CC}max Control Signals = V_{CC} CMOS levels
		512KB		100			
		1MB					
		2MB					
		3MB					
		4MB					
		5MB					

CMOS TEST Conditions: V_{CC} = 5V ± 5%, V_{IL} = V_{SS} ± 0.2V, V_{IH} = V_{CC} ± 0.2V

Notes:
1. All currents are RMS values unless otherwise specified. I_{CCR}, I_{CCW} and I_{CCE} are based on Byte wide operations. For 16 bit operation values are double
2. Control Signals: $CE_{1\#}$, $CE_{2\#}$, OE#, WE#, REG#.
3. Typical: V_{CC} = 5V, T = +25°C.

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
I_{LI}	Input Leakage Current	1		±10	µA	V_{CC} = V_{CC}MAX V_{IN} =V_{CC} or V_{SS}
I_{LO}	Output Leakage Current	1		±10	µA	V_{CC} = V_{CC}MAX V_{OUT} =V_{CC} or V_{SS}
V_{IIL}	Input Low Voltage	1	0	0.8	V	
V_{IH}	Input High Voltage	1	0.7V_{CC}	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage	1		0.4	V	I_{OL} = 3.2mA
V_{OH}	Output High Voltage	1	V_{CC}-0.4	V_{CC}	V	I_{OH} = -2.0mA
V_{LKO}	V_{CC} Erase/Program Lock Voltage	1	2.5		V	

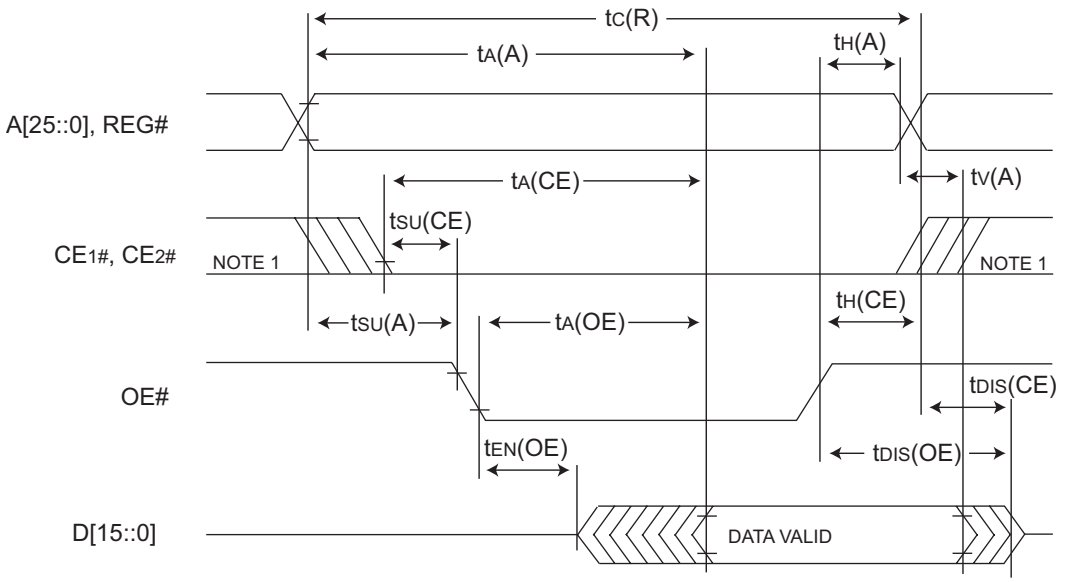
Notes:
1. Values are the same for byte and word wide modes for all card densities.
2. Exceptions: Leakage currents on $CE_{1\#}$, $CE_{2\#}$, OE#, REG# and WE# will be < 500 µA when V_{IN} = GND due to internal pull-up resistors.

AC CHARACTERISTICS
Read Timing Parameters

SYM (PCMCIA)	Parameter	150ns		200ns		Unit
		Min	Max	Min	Max	
t_C(R)	Read Cycle Time	150				ns
t_a(A)	Address Access Time		150	200	200	ns
t_a(CE)	Card Enable Access Time		150		200	ns
t_a(OE)	Output Enable Access Time		75		100	ns
t_{su}(A)	Address Setup Time		20		20	ns
t_{su}(CE)	Card Enable Setup Time		0		0	ns
t_h(A)	Address Hold Time		20		20	ns
t_h(CE)	Card Enable Hold Time		20		20	ns
t_v(A)	Output Hold from Address Change		0		0	ns
t_{dis}(CE)	Output Disable Time from CE#		60		60	ns
t_{dis}(OE)	Output Disable Time from OE#		60	5	60	ns
t_{en}(CE)	Output Enable Time from CE#	5				ns
t_{en}(OE)	Output Enable Time from OE#	5		5		ns

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

READ TIMING DIAGRAM



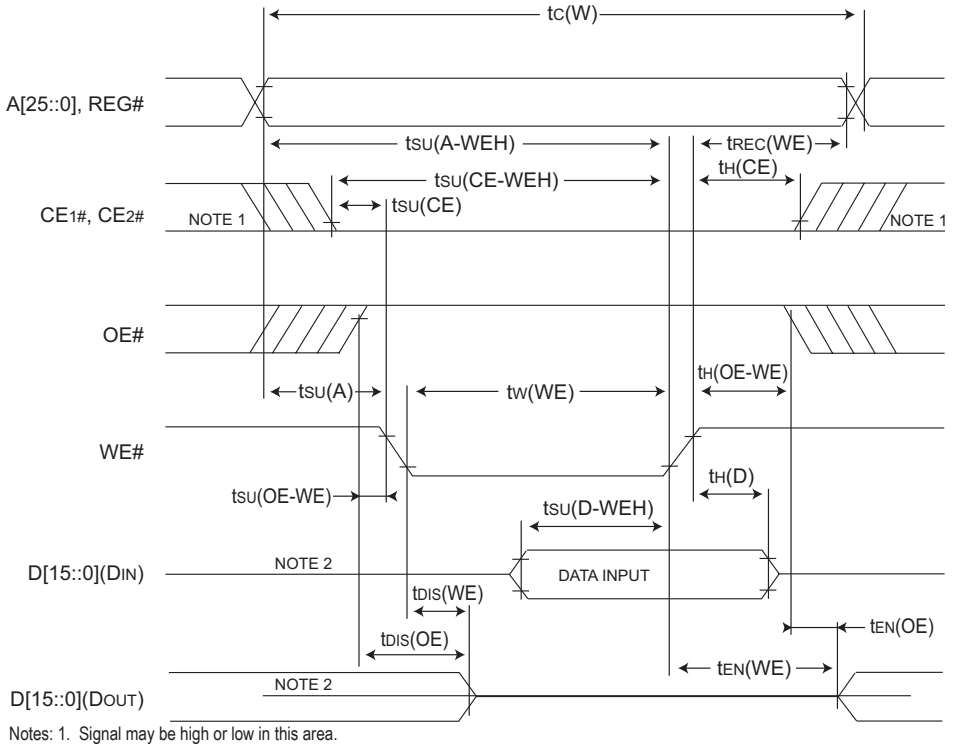
Note: Signal may be high or low in this area.

WRITE TIMING PARAMETERS

SYM (PCMCIA)	Parameter	150ns		200ns		Unit
		Min	Max	Min	Max	
t_CW	Write Cycle Time	150		200		ns
t_w(WE)	Write Pulse Width	80		120		ns
t_{su}(A)	Address Setup Time	20		20		ns
t_{su}(A-WEH)	Address Setup Time for WE#	100		100		ns
t_{su}(CE-WEH)	Card Enable Setup Time for WE#	100		100		ns
t_{su}(D-WEH)	Data Setup Time for WE#	50		50		ns
t_h(D)	Data Hold Time	20		20		ns
t_{rec}(WE)	Write Recover Time	20		20		ns
t_{dis}(WE)	Output Disable Time from WE#		60		60	ns
t_{dis}(OE)	Output Disable Time from OE#		60		60	ns
t_{en}(WE)	Output Enable Time from WE#	5		5		ns
t_{en}(OE)	Output Enable Time from OE#	5		5		ns
t_{su}(OE-WE)	Output Enable Setup from WE#	10		10		ns
t_h(OE-WE)	Output Enable Hold from WE#	10		10		ns
t_{su}(CE)	Card Enable Setup Time from OE#	0		0		ns
t_h(CE)	Card Enable Hold Time	20		20		ns

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

WRITE TIMING DIAGRAM



Notes: 1. Signal may be high or low in this area.
2. When the data I/O pins are in the output state, no signals shall be applied to the data pins (D15 - D0) by the host system.

Data Write and Erase Performance[1,3]
V_{CC} = 5V ± 5%, T_A = 0°C to + 60°C

Parameter	Notes	Min	Typ[1]	Max	Units
Chip Program Time	28F010 1,2,4		2	12.5	sec
	28F020 1,2,4		4	25	
Chip Erase Time	28F010 1,3,4		1	10	sec
	28F020 1,3,4		2	30	

Notes:

1. Typical: Nominal voltages and T_A = 25ºC.
2. Minimum byte programming time excluding system overhead is 16 µs (10µs program + 6µs write recovery), while maximum is 400µs/byte (16 µs x 25 loops allowed by algorithm). Max chip programming time is specified lower than the worst case allowed by the programming algorithm since most bytes program significantly faster than the worst case byte.
3. Excludes 00H Programming prior to Erasure.
4. Excludes System-Level Overhead.

CIS INFORMATION FOR FLD SERIES CARDS

ADDRESS	VALUE	DESCRIPTION
00H	01H	CISTPL_DEVICE
02H	03H	TPL_LINK
04H	53H 52H	FLASH = 150ns (device writable) FLASH = 200ns (device writable)
06H	0CH 05H 0DH 06H 2DH 0EH 4DH	CARD SIZE: 256KB 512KB 1MB 2MB 3MB 4MB 5MB
08H	FFH	END OF DEVICE
0AH	18H	CISTPL_JEDEC_C
0CH	02H	TPL_LINK
0EH	89H	INTEL - ID
10H	B4H BDH	INTEL 28F010 - ID INTEL 28F020 - ID
12H	17H	CISTPL_DEVICE_A
14H	03H	TPL_LINK
16H	42H	EEPROM - 200ns
18H	01H	Device Size = 2KBytes
1AH	FFH	END OF TUPLE
1CH	1EH	CISTPL_DEVICEGEO
1EH	06H	TPL_LINK
20H	02H	DGTPL_BUS
22H	11H	DGTPL_EBS
24H	01H	DGTPL_RBS
26H	01H	DGTPL_WBS
28H	01H	DGTPL_PART
2AH	01H	FLASH DEVICE NON-INTERLEAVED
2CH	20H	CISTPL_MANFID
2EH	04H	TPL_LINK(04H)
30H	F6H	EDI TPLMID_MANF: LSB
32H	01H	EDI TPLMID_MANF: MSB

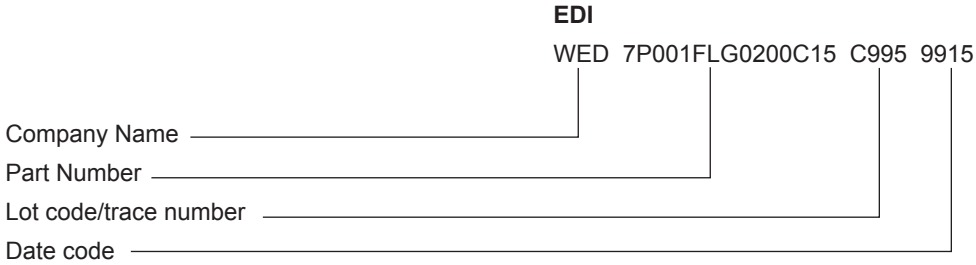
ADDRESS	VALUE	DESCRIPTION
34H	00H	LSB: Number Not Assigned
36H	00H	MSB: Number Not Assigned
38H	15H	CISTPL_VERS1
3AH	47H	TPL_LINK
3CH	04H	TPLLV1_MAJOR
3EH	01H	TPLLV1_MINOR
40H	45H	E
42H	44H	D
44H	49H	I
46H	37H	7
48H	50H	P
4AH 4CH 4EH	32H 35H 36H	2 5 6
	35H 31H 32H	5 1 2
	30H 30H 31H	0 0 1
	30H 30H 32H	0 0 2
	30H 30H 33H	0 0 3
	30H 30H 34H	0 0 4
	30H 30H 35H	0 0 5
50H	46H	F
52H	4CH	L
54H	47H	G

CIS INFORMATION FOR FLD SERIES CARDS (CONT.)

ADDRESS	VALUE	DESCRIPTION
56H	30H	0
58H	32H	2
	30H	0
	36H	6
5AH	2DH	-
5CH	2DH	-
5EH	2DH	-
60H	31H	1
62H	35H	5
64H	20H	SPACE
66H	00H	END TEXT
68H	43H	C
6AH	4FH	O
6CH	50H	P
6EH	59H	Y
70H	52H	R
72H	49H	I
74H	47H	G
76H	48H	H
78H	54H	T
7AH	20H	SPACE
7CH	45H	E
7EH	4CH	L
80H	45H	E
82H	43H	C
84H	54H	T
86H	52H	R
88H	4FH	O
8AH	4EH	N
8CH	49H	I
8EH	43H	C

ADDRESS	VALUE	DESCRIPTION
90H	20H	SPACE
92H	44H	D
94H	45H	E
96H	53E	S
98H	49H	I
9AH	47H	G
9CH	4EH	N
9EH	53H	S
A0H	20H	SPACE
A2H	49H	I
A4H	4EH	N
A6H	43H	C
A8H	4FH	O
AAH	52H	R
ACH	50H	P
AEH	4FH	O
B0H	52H	R
B2H	41H	A
B4H	54H	T
B6H	45H	E
B8H	44H	D
BAH	20H	SPACE
BCH	00H	END TEXT
BEH	31H	1
C0H	39H	9
C2H	39H	9
C4H	37H	7
C6H	00H	END TEXT
C8H	FFH	END OF LIST
CAH	FFH	CISTPL_END
DCH	00H	INVALID ADDRESS

PRODUCT MARKING



PART NUMBERING

7 P 001 FLG02 00 C 15

CARD TECHNOLOGY
- 7 FLASH
- 8 SRAM

PC CARD
- P Standard PCMCIA
- R Ruggedized PCMCIA

CARD CAPACITY
- 001 1MB

CARD FAMILY AND VERSION
- See Card Family and Version Info. for details (next page)

PACKAGING OPTION
- 00 Standard, type 1

TEMPERATURE RANGE
- C = Commercial 0°C to +70°C
- I = Industrial -40°C to +85°C

CARD ACCESS TIME
- 15 150ns
- 20 200ns

The shaded area (addresses 56H 58H) represents just some of the family versions. For all the versions see the Card Family and Version information.

CARD FAMILY AND VERSION INFORMATION

FLG 01-FLG04 Intel* Based on **28F010**

FLG 11-FLG14 Catalyst

FLG11 No Attribute memory, no Write Protect
FLG12 With Attribute Memory, no Write Protect
FLG13 No Attribute memory, with Write Protect
FLG14 With Attribute Memory, with Write Protect

Example P/N **7P XXX FLG 12 SS T ZZ**

FLG 05-FLG08 Intel* Based on **28F020**

FLG 15-FLG18 Catalyst

FLG15 No Attribute memory, no Write Protect
FLG16 With Attribute Memory, no Write Protect
FLG17 No Attribute memory, with Write Protect
FLG18 With Attribute Memory, with Write Protect

Example P/N **7P XXX FLG 06 SS T ZZ** *discontinued – memory components not available

ORDERING INFORMATION

7P XXX FLGYY SS T ZZ

XXX

256 [1]	256KB	
512		512KB
001		1MB
002		2MB
003 [2]	3MB	
004 [2]	4MB	
005 [2]	5MB	

[1] availalbe only with 28F010
[2] availalbe only with 28F020

FLGYY

Card version (see card family and version information)

SS

00	WEDC Silkscreen
01	Blank Housing, Type I
02	Blank Housing, Type I Recessed

T

C	=	Commercial
I**	=	Industrial

ZZ

15	150ns
20	200ns

Notes: Options with intermediate memory capacities, without attribute memory and with hardware write protect switch are available.
** Denotes advanced information.