



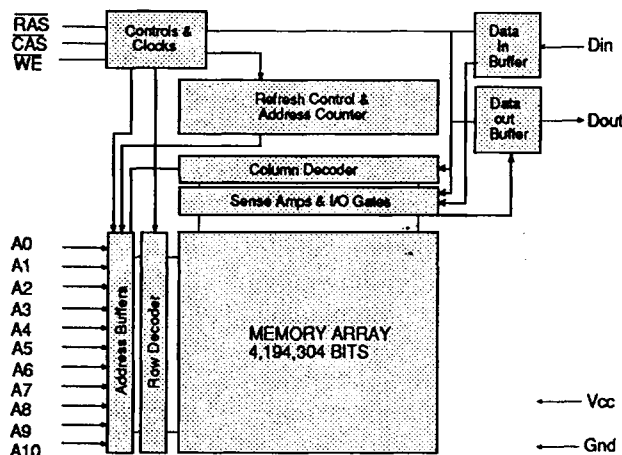
Mosaic
Semiconductor
Inc.

4,194,304 x 1 CMOS High Speed Dynamic RAM

Features

Row Access Time of 80,100,120 ns
Available in 20 Pin DIP, 20 & 24 Pin VIL
5 Volt Supply $\pm 10\%$
1024 Refresh Cycles (16 ms)
CAS before RAS Refresh
RAS only Refresh
Hidden Refresh
Fast Page Mode Capability
Test Function Available
Directly TTL Compatible
May Be Processed to MIL-STD-883 Class B.
Fully Compliant Version Available

Block Diagram



4Meg x 1 Monolithic DRAM

MDM14000-80/10/12

Issue 3.2 : September 1993

Pin Definition

Package Type: 'K','V','G', 'W','J'

Din	1		20	GND
$\overline{WE}$	2		19	Dout
$\overline{RAS}$	3		18	$\overline{CAS}$
NC	4		17	NC
A10	5		16	A9
A0	6		15	A8
A1	7		14	A7
A2	8		13	A6
A3	9		12	A5
V_{cc}	10		11	A4

Package Type: 'VX' - Page 9.

Pin Functions

A0-A10	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
Din	Data Input
Dout	Data Output
$\overline{WE}$	Read/Write Input
V_{cc}	Power (+5V)
GND	Ground
NC	No Connect

Package Details Dimensions in inches(mm). Tolerance on all dimensions $\pm 0.010(.254)$.

Pin Count	Description	Package Type	Material	Pinout
20	400 mil Dual-in-Line(DIP)	K	Ceramic	JEDEC
20	100 mil Vertical-in-Line(VIL)	V	Ceramic	JEDEC
24	100 mil Vertical-in-Line(VIL)	VX	Ceramic	ASIC
20	Leadless Chip Carrier(LCC)	W	Ceramic	JEDEC
20	Ceramic Flatpack	G	Ceramic	JEDEC
20	Leaded CSOJ	J	Ceramic	JEDEC

Package Dimensions and details on page 9,10.

VIL is a trademark of Mosaic Semiconductor Inc., Patent No. D316251.

Absolute Maximum Ratings

Voltage on any pin relative to V_{ss}	V_i	-1 to +7	V
Power Dissipation	P_i	1.0	W
Storage Temperature	T_{slg}	-65 to +150	°C
Short circuit output current	I_{osc}	50	mA

Recommended Operating Conditions

		min	typ	max	
Supply Voltage	V_{CC}	4.50	5.0	5.50	V
Input High Voltage	V_{IH}	2.4	-	6.5	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AL}	-40	-	85	°C (14000I)
	T_{AL}	-55	-	125	°C (14000M,MB,MC)

Capacitance ($V_{CC}=5V \pm 10\%$, $T_A=25^\circ\text{C}$)

Parameter		Symbol	typ	max	Unit	Notes
Input Capacitance:	Address	C_{I1}	-	6	pF	1
Input Capacitance:	Clocks	C_{I2}	-	7	pF	1
I/O Capacitance:	Data-in/out	C_{IO}	-	7	pF	1,2

Notes: 1. Capacitance calculated, not measured.
 2. $CAS = V_{IH}$ to disable Dout.

DC Electrical Characteristics

Parameter	Symbol	Test Condition	-80		-10		-12		Unit	Notes
			min	max	min	max	min	max		
Operating Current	I_{CC1}	RAS,CAS Cycling: $t_{RC} = \text{min.}$	-	90	-	80	-	70	mA	1,2
Refresh Current	I_{CC3}	RAS only Refresh, $t_{RC} = \text{min.}$	-	90	-	80	-	70	mA	
Refresh Current	I_{CC6}	CAS before RAS Refresh $t_{RC} = \text{min}$	-	90	-	80	-	70	mA	
Page Mode Supply Current	I_{CC7}	RAS= V_{IL} , CAS Cycling, $t_{RC} = \text{min.}$	-	90	-	80	-	70	mA	
Standby Current	I_{CC2} I_{CC4}	RAS,CAS= V_{IH} , Dout Disabled RAS,CAS, $\geq V_{CC}-0.2V$, Dout Disabled, CMOS Levels	-	3	-	3	-	3	mA	2
Input Leakage	I_{LI}	$V_{IN}=0$ to +7V	-10	10	-10	10	-10	10	μA	2
Output Leakage	I_{LO}	$V_{OUT}=0$ to +7V, Dout is disabled.	-10	10	-10	10	-10	10	μA	2
Output Levels	V_{OH}	$I_{OUT} = -5\text{mA}$	2.4	-	2.4	-	2.4	-	V	2
	V_{OL}	$I_{OUT} = 4.2\text{mA}$	-	0.4	-	0.4	-	0.4	V	2

Notes: 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max. is specified at the output open condition.
 2. These parameters are 100% tested.

AC Test Conditions

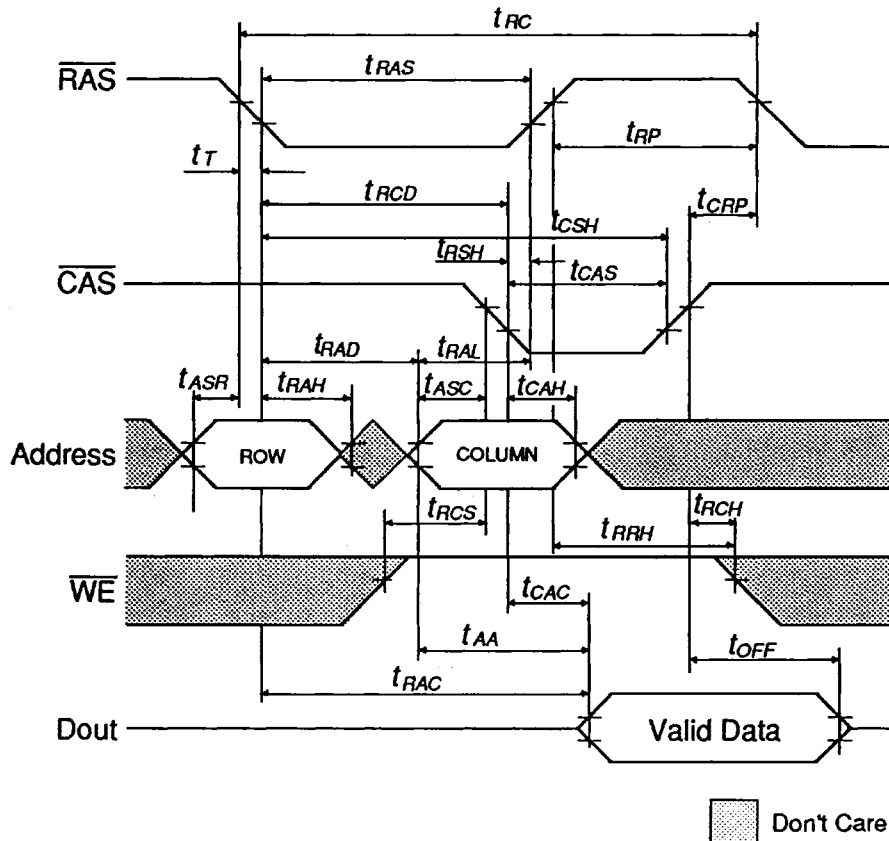
- * Input pulse levels: 0.8 to 2.4V
- * Input rise and fall times: 5ns
- * Input and Output timing reference levels: 1.5V
- * Output load: 2 TTL gates + 100pF

Electrical Characteristics & Recommended AC Operating Conditions (1,9)

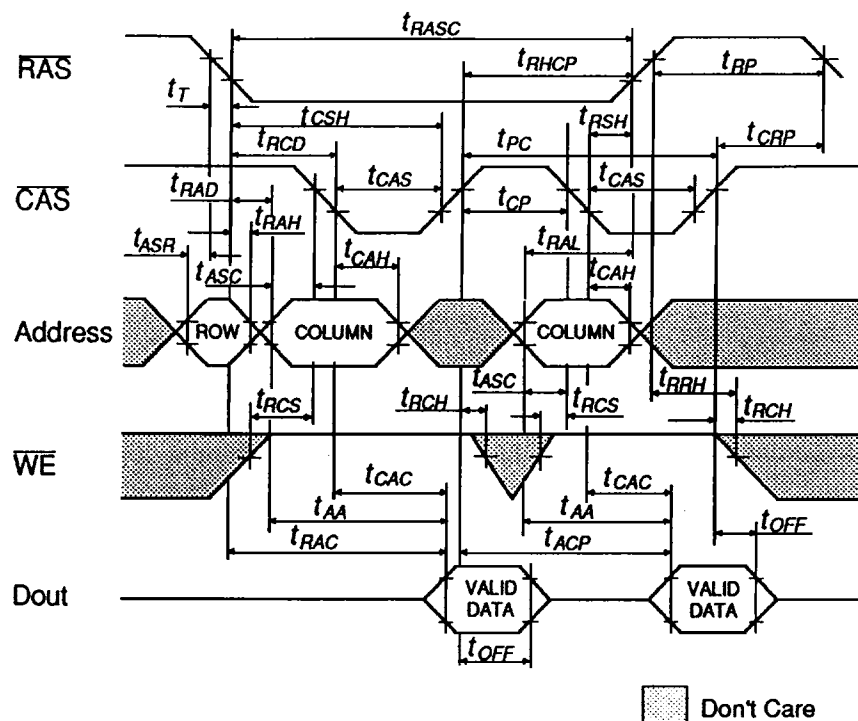
Parameter	Symbol	-80		-10		-12		Unit	Note
		min	max	min	max	min	max		
Access Time from $\overline{\text{RAS}}$	t_{RAC}	-	80	-	100	-	120	ns	2,3,12
Access Time from $\overline{\text{CAS}}$	t_{CAC}	-	25	-	25	-	30	ns	3,4,12
Output Buffer Turn-off Delay	t_{OFF}	0	20	0	25	0	30	ns	5,13
Transition Time (Rise & Fall)	t_{T}	3	50	3	50	3	50	ns	6,13
Random Read or Write Cycle Time	t_{RC}	150	-	180	-	210	-	ns	12
$\overline{\text{RAS}}$ Precharge Time	t_{RP}	60	-	70	-	80	-	ns	12
$\overline{\text{RAS}}$ Pulse Width	t_{RAS}	80	100000	100	100000	120	100000	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CAS}	25	100000	25	100000	30	100000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RCD}	22	55	25	75	25	90	ns	7
$\overline{\text{RAS}}$ Hold Time	t_{RSH}	25	-	25	-	30	-	ns	
$\overline{\text{CAS}}$ Hold Time	t_{CSH}	80	-	100	-	120	-	ns	
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RAD}	17	40	20	50	20	65	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{RAL}	40	-	50	-	60	-	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CRP}	5	-	10	-	10	-	ns	13
Row Address Setup Time	t_{ASR}	0	-	0	-	0	-	ns	12
Row Address Hold Time	t_{RAH}	12	-	15	-	15	-	ns	
Column Address Setup Time	t_{ASC}	0	-	0	-	0	-	ns	12
Column Address Hold Time	t_{CAH}	15	-	20	-	25	-	ns	
Access Time From Address	t_{AA}	-	40	-	50	-	60	ns	
Write Command Setup Time	t_{WCS}	0	-	0	-	0	-	ns	8,12
Write Command Hold Time	t_{WCH}	15	-	20	-	25	-	ns	
Write Command Pulse Width	t_{WP}	15	-	20	-	25	-	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{RWL}	25	-	25	-	30	-	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{CWL}	25	-	25	-	30	-	ns	
Data in Setup Time	t_{DS}	0	-	0	-	0	-	ns	
Data in Hold Time	t_{DH}	15	-	20	-	25	-	ns	12
Read Command Setup Time	t_{RCS}	0	-	0	-	0	-	ns	13
Read Command Hold Time referenced to $\overline{\text{CAS}}$	t_{RCH}	0	-	0	-	0	-	ns	10
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t_{RRH}	10	-	10	-	10	-	ns	10
Refresh Period (1024 Cycles)	t_{REF}	-	16	-	16	-	16	ms	
Read-Modify-Write Cycle Time	t_{RWC}	180	-	210	-	245	-	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t_{RWD}	80	-	100	-	120	-	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	t_{CWD}	25	-	25	-	30	-	ns	
Column Address to $\overline{\text{WE}}$ Delay Time	t_{AWD}	40	-	45	-	55	-	ns	
$\overline{\text{CAS}}$ Setup Time	t_{CSR}	10	-	10	-	10	-	ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t_{CHR}	20	-	20	-	25	-	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time	t_{RPC}	10	-	10	-	10	-	n	
Fast Page Mode Cycle Time	t_{PC}	55	-	55	-	65	-	ns	
$\overline{\text{CAS}}$ Precharge Time, Page Cycle	t_{CP}	12	-	12	-	15	-	ns	
Fast Page Mode $\overline{\text{RAS}}$ Pulse Width	t_{RASC}	-	100000	-	100000	-	100000	ns	11
Access Time From $\overline{\text{CAS}}$ Precharge	t_{ACP}	-	50	-	50	-	60	ns	
$\overline{\text{RAS}}$ Hold Time From $\overline{\text{CAS}}$ Precharge	t_{RHCP}	50	-	50	-	60	-	ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PCM}	85	-	115	-	140	-	ns	
Test Mode $\overline{\text{WE}}$ Setup Time	t_{WS}	0	-	0	-	0	-	ns	13
Test Mode $\overline{\text{WE}}$ Hold Time	t_{WH}	20	-	20	-	20	-	ns	13
$\overline{\text{CAS}}$ Precharge in Counter Test Cycle	t_{CPT}	40	-	50	-	60	-	ns	13

Notes:

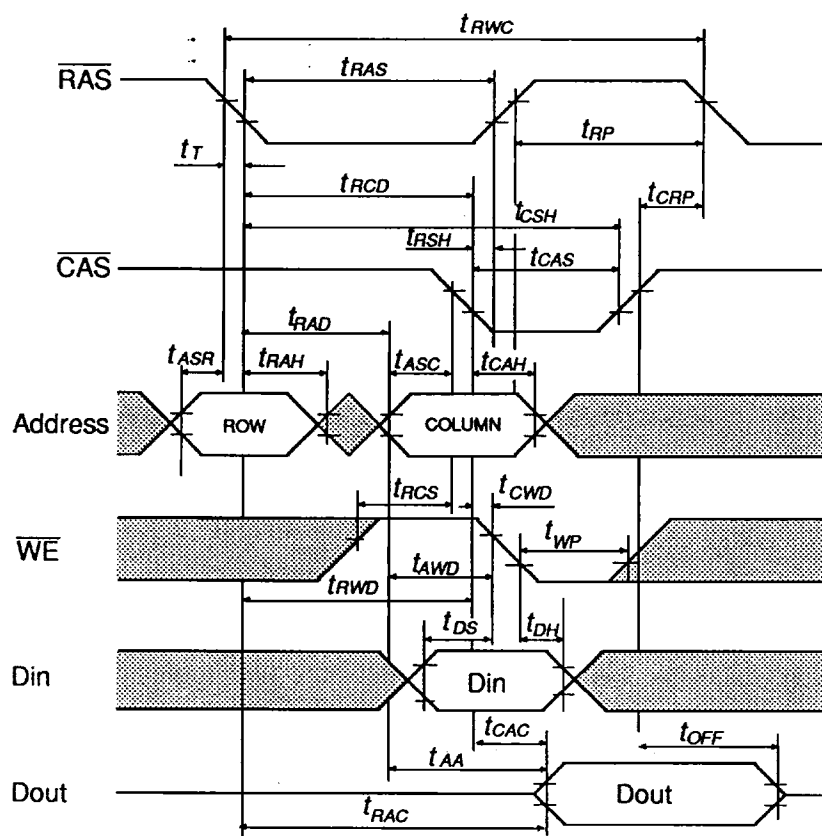
1. AC measurements assume $t_f=5\text{ns}$.
2. Assumes that t_{RCD} is less than or equal to $t_{\text{RCD}}(\text{max.})$. If t_{RCD} is greater than the max. recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load current equivalent to two TTL loads and 100pF.
4. Assumes that t_{RCD} is greater than or equal to $t_{\text{RCD}}(\text{max.})$.
5. $t_{\text{OFF}}(\text{max.})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. $V_{\text{IH}}(\text{min.})$ and $V_{\text{IL}}(\text{max.})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
7. Operation with the $t_{\text{RCD}}(\text{max.})$ limit insures that $t_{\text{RAC}}(\text{max.})$ can be met, $t_{\text{RCD}}(\text{max.})$ is specified as a reference point only, if $t_{\text{RCD}}(\text{max.})$ limit, then access time is controlled exclusively by t_{CAC} .
8. t_{WCS} is not a restrictive operating parameter. It is included in the Data Sheet as Electrical Characteristics only.
9. An initial pause of 200 μs is required after power-up. Then execute at least 8 initialisation (RAS) cycles.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. t_{RASC} defines RAS pulse width in the fast page mode cycles.
12. These parameters are 100% tested.
13. These parameters are not tested.
14. Testmode parameters are for reference only

Timing Waveforms**Read Cycle**

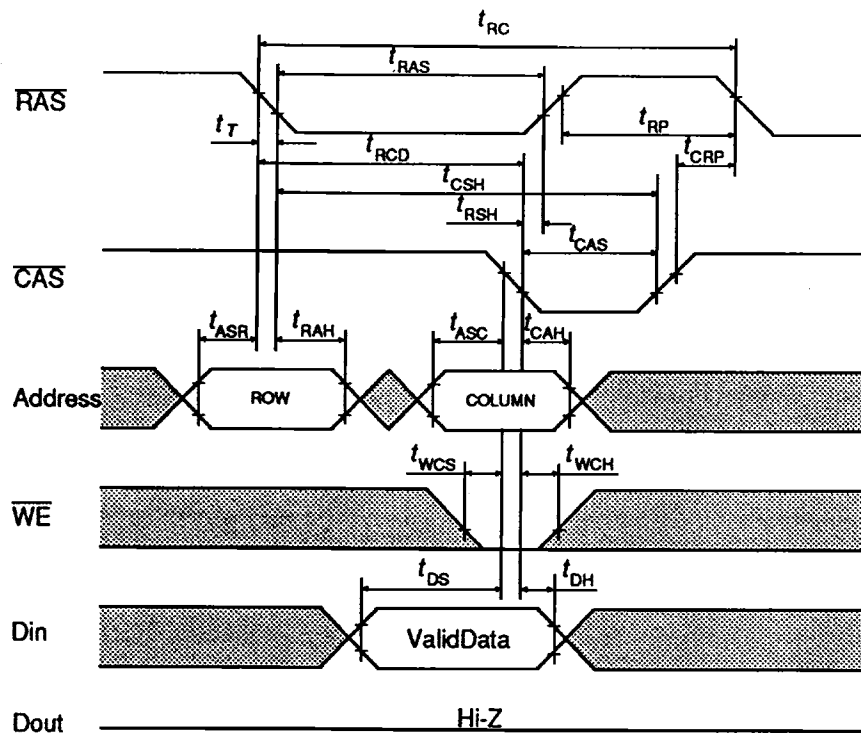
Page Mode Read Cycle



Read-Modify-Write Cycle Timing Diagram

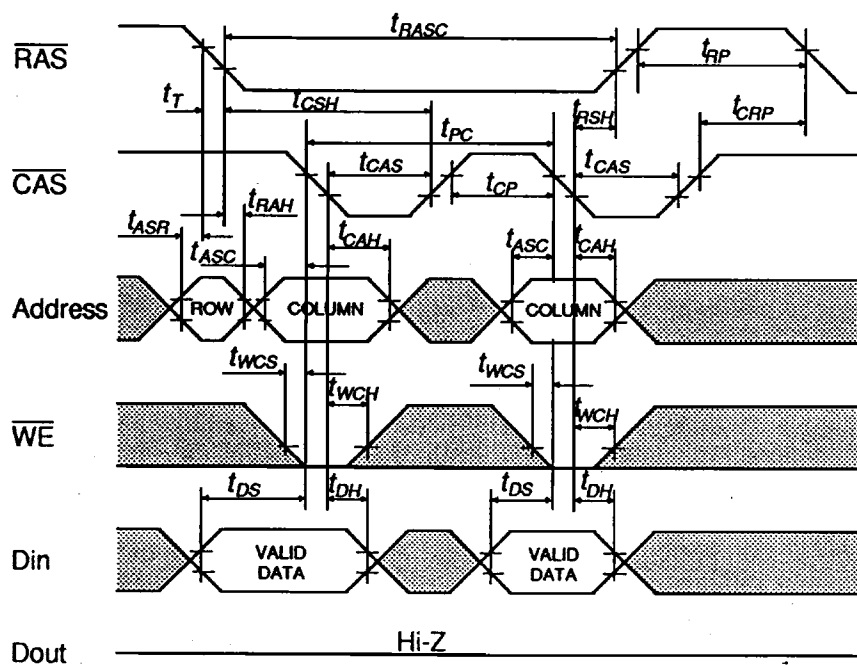


Early Write Cycle



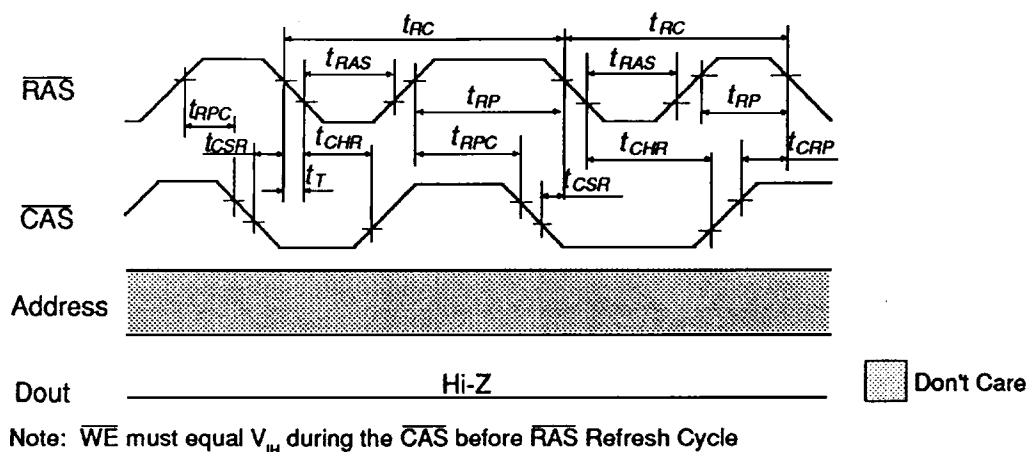
□ Don't Care

Page Mode Early Write Cycle

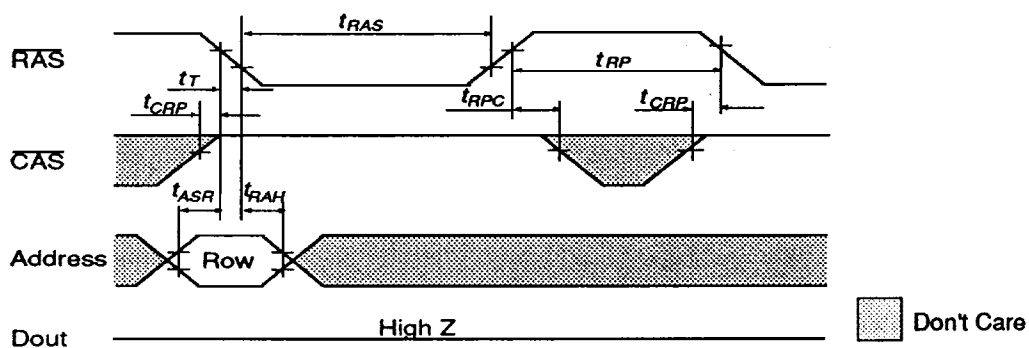


□ Don't Care

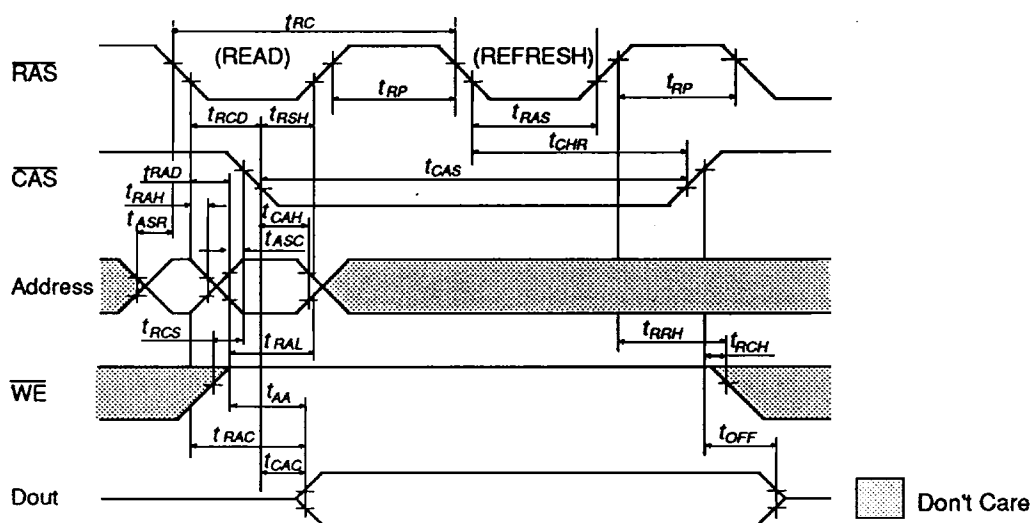
CAS Before RAS Refresh Cycle

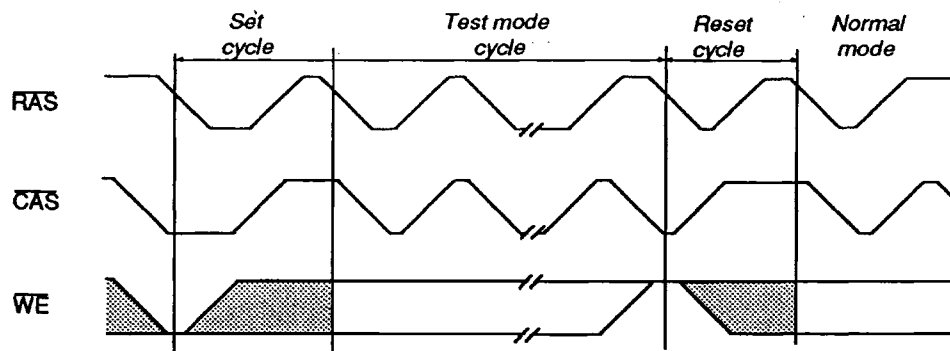
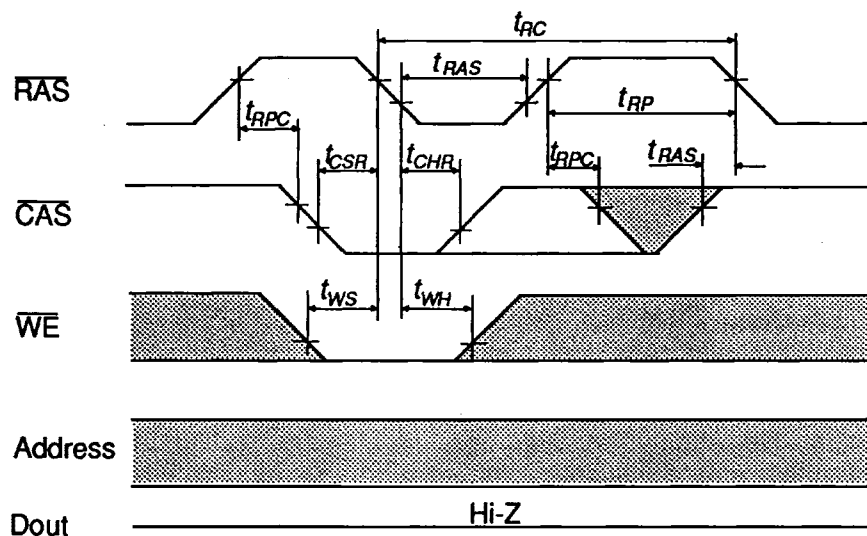
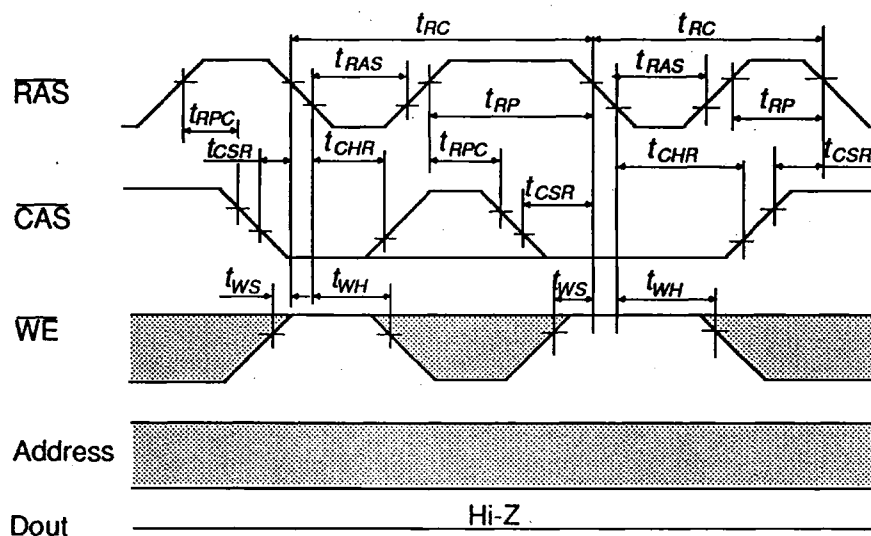


RAS Only Refresh Cycle



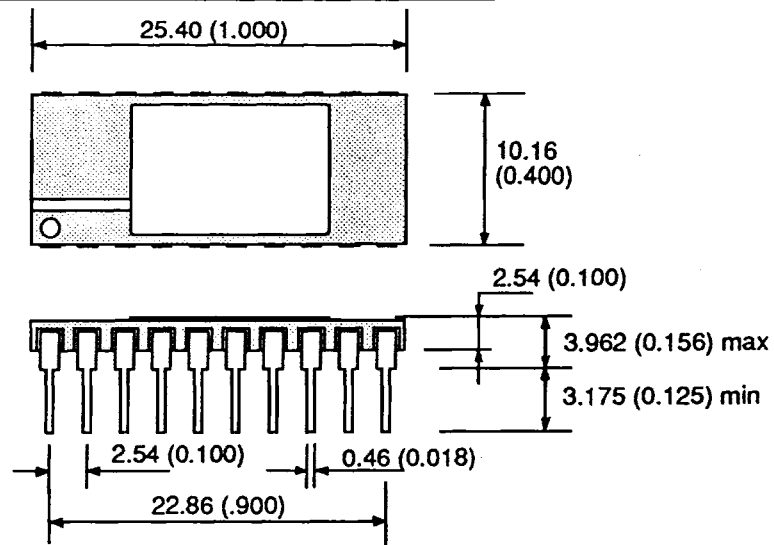
Hidden Refresh Cycle



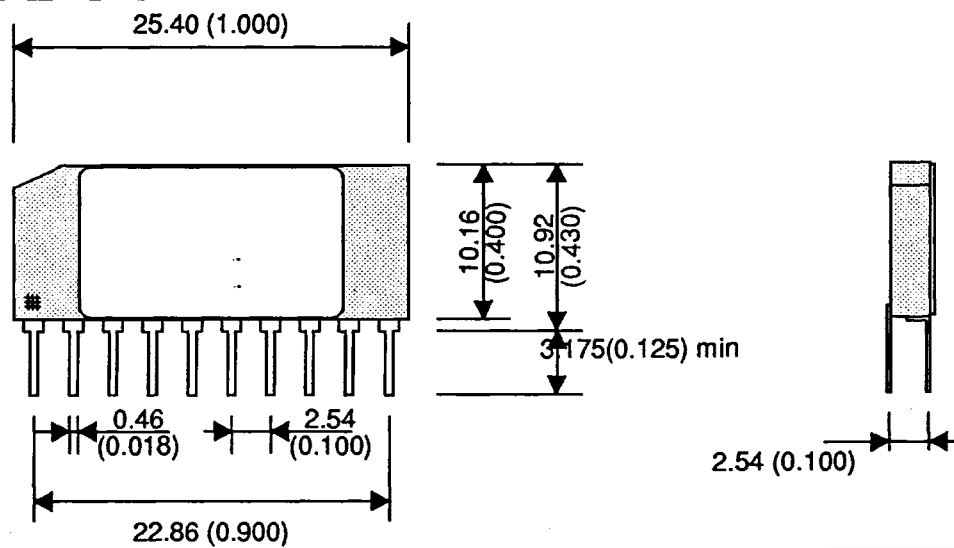
Test Mode Cycle (NOTE: Test mode information is for reference only)

Test Mode Set Cycle

Test Mode Reset Cycle: $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle


Package Details Dimensions in mm (inches). Tolerance on all dimensions $\pm 0.254(0.010)$.

20 Pin Dual-In-Line ('K' Package)

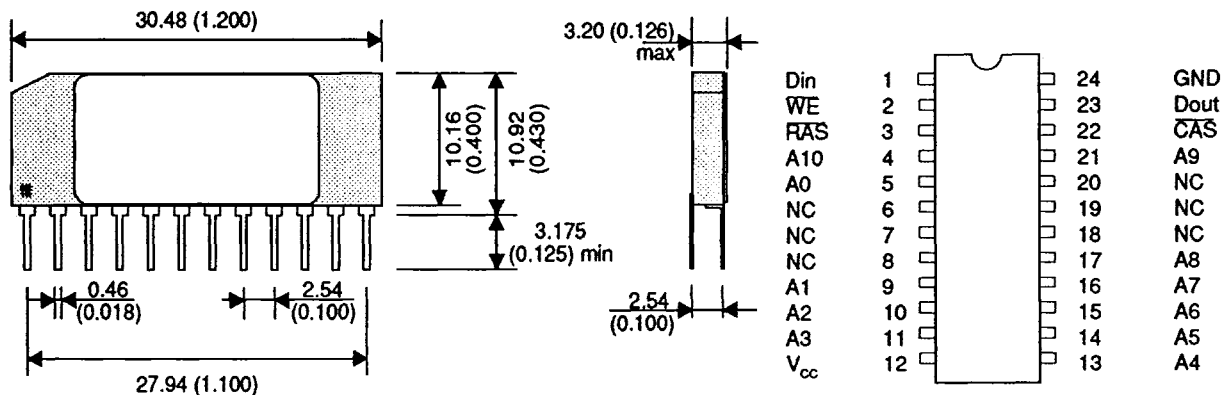


20 Pin Vertical-In-Line (VIL) ('V' Package)

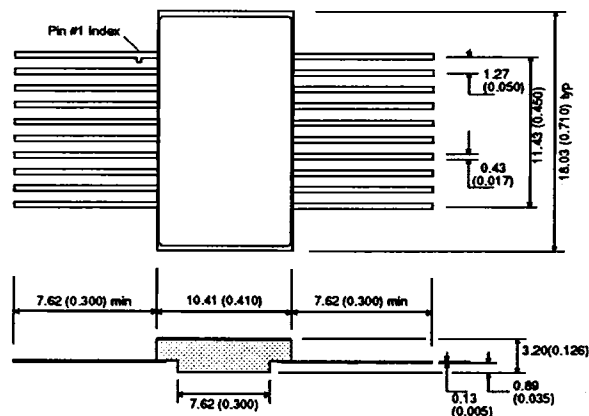


24 Pin Vertical-In-Line (VIL™) ('VX' Package)

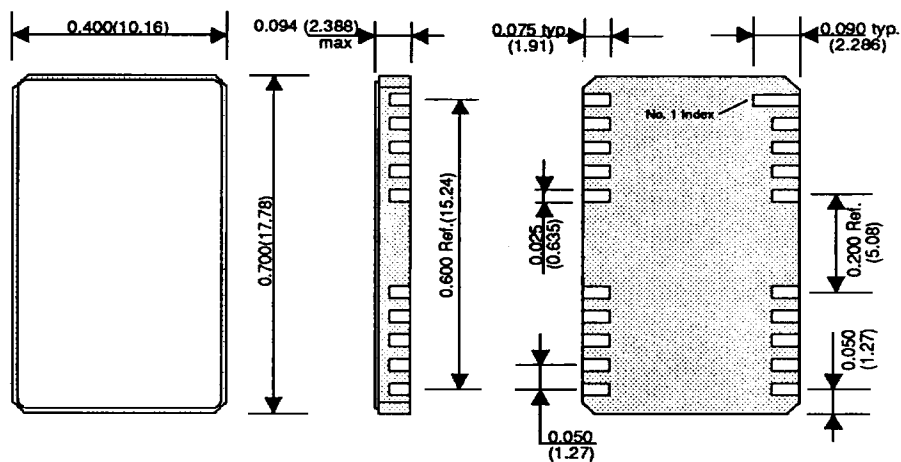
Pin Definition



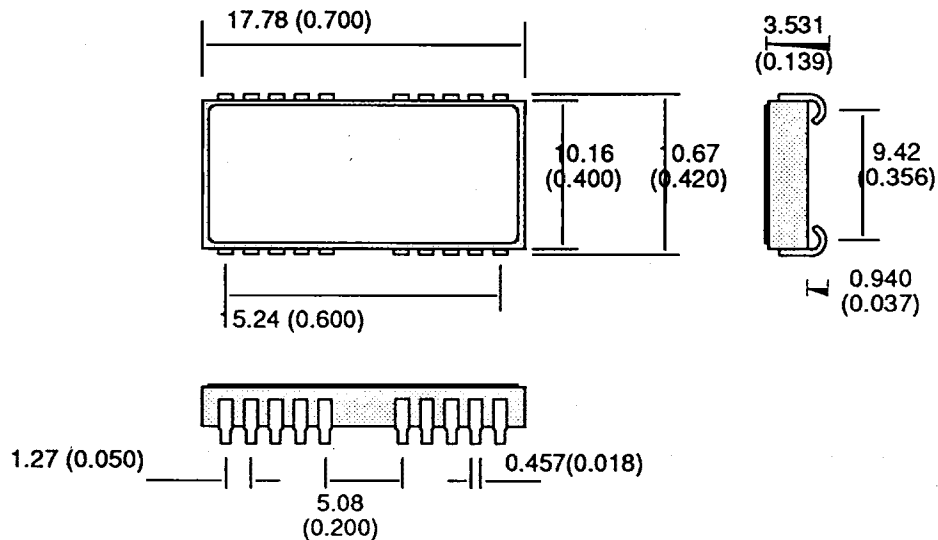
20 Pin Ceramic Flatpack ('G' Package)



20 Pad Ceramic Leadless Chip Carrier ('W' Package)



20 Pin Ceramic Leaded CSOJ ('J' Package)



Ordering Information

MDM14000VMB-10

Speed	80,100,120 ns
Temp. range/screening	Blank = Commercial Temp. I = Industrial Temp. M = Military Temp. MB = Processed to MIL-STD-883 Method 5004, non-compliant. MC = MIL-STD-883 Compliant
Power	Blank = Standard Power Part
Package	K = 20 Pin 400 mil DIP V = 20 Pin 100 mil Vertical-in-Line VX = 24 Pin 100 mil Vertical-in-Line G = 20 Pin Ceramic Flatpack W = 20 Pad Ceramic LCC J = 20 Pin Ceramic SOJ

Note: For more information regarding screening flows contact Mosaic Semiconductor Inc. for a 'Screening Flow Applications Note.'

The policy of the company is one of continuous development and while the information presented in this data sheet is believed to be accurate, no liability is assumed for any data contained within. The company reserves the right to make changes without notice at any time.

© 1988 This design is the property of Mosaic Semiconductor, Inc.



Mosaic
Semiconductor
Inc.

7420 Carroll Road
San Diego, CA 92121
Tel: (619) 271 4565
FAX: (619) 271 6058