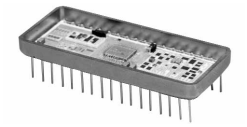


SYNCHRO-TO-DIGITAL CONVERTERS

DESCRIPTION

The SD-14590/91/92 series are high reliability synchro- or resolver-to-digital converters with 14-bit-only, 16-bit-only, or 14- or 16-bit programmable resolution. This series of converters feature high quality velocity output and hermetically sealed packages. In addition, the SD-14591 and SD-14592 are pin-for-pin replacements for the Natel 1024 and 1026, respectively.

User-programmable resolution has been designed into the SD-14590 to increase the capabilities of modern motion control systems. The precise positioning attained at 16 bits of resolution and fast tracking of a 14-bit device are now available from one 36-pin double DIP hybrid. Velocity output (VEL) from the SD-14590/91/92 is a V-based voltage of 0 to ±3.5 VDC with a linearity to 2.0%. Output voltage is positive for an increasing angle.

The digital angle output from the SD-14590/91/92 is a natural binary code, parallel positive logic and is TTL/CMOS compatible. Synchronization to a computer is accomplished via a converter busy (CB) and an inhibit ($\overline{\text{INH}}$) input.

APPLICATIONS

Because of its high reliability, accuracy, small size, and low power consumption, the SD-14590/91/92 is ideal for the most stringent and severe industrial and military ground or avionics applications. All models are available with MIL-PRF-38534 processing as a standard option.

Designed with three-state output, the SD-14590/91/92 is especially well-suited for use with computer based systems. Among the many possible applications are radar and navigation systems, fire control systems, flight instrumentation, and flight trainers or simulators.

FEATURES

- ***Replacement for NATEL'S 1024 and 1026***
- ***High Quality Velocity Output***
- ***Eliminates Tachometer***
- ***Accuracy to ±1.3 Arc Minutes***
- ***Small Size***
- ***Synchro or Resolver Input***
- ***Synthesized Reference Eliminates 180° Lock-Up***

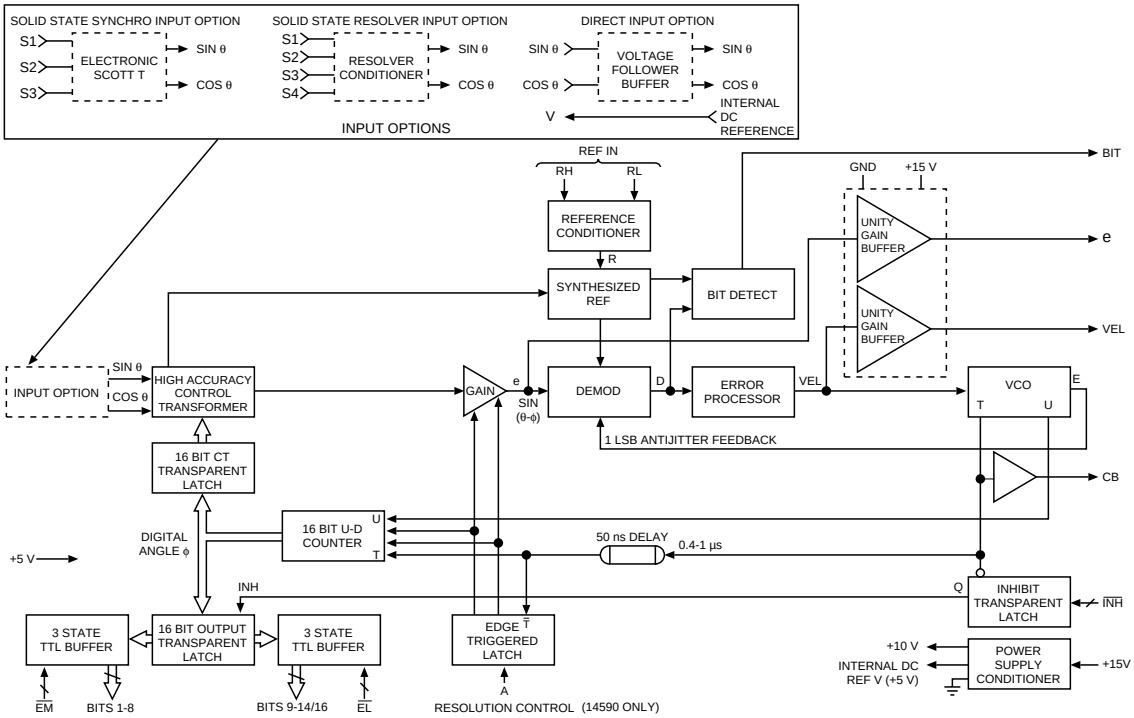


FIGURE 1. SD-14590/91/92 BLOCK DIAGRAM

TABLE 1. SD-14590/91/92 SPECIFICATIONS

Apply over temperature range, power supply range, reference, frequency and amplitude ranges; 10% signal amplitude variation; and up to 10% harmonic distortion in the reference.

PARAMETER	UNIT	VALUE
RESOLUTION(1)	Bits	14, 16, 14 / 16
ACCURACY(2)	Min	±4, ±2, or ±1 +1 LSB
REPEATABILITY	LSB	1 max
DIFFERENTIAL LINEARITY	LSB	1 max in the 16th bit
REFERENCE INPUT CHARACTERISTICS		
Carrier Frequency Ranges		
Nominal 400 Hz Units	Hz	360-1000
Nominal 60 Hz Units	Hz	47-1000
Voltage Range	Vrms	4-130
Input Impedance		
Single Ended	Ohm	250k min
Differential	Ohm	500k min
Common Mode Range	V	210 peak max 500 transient peak
SIGNAL INPUT CHARACTERISTICS (voltage options and minimum input impedance balanced)		
Synchro	V	11.8 V_{L-L} 90 V_{L-L}
Zin Line to Line	Ohm	17.5k 130k
Zin Each Line to Gnd	Ohm	11.5k 85k
Resolver	V	11.8 V_{L-L} 26 V_{L-L}
Zin Single Ended	Ohm	23k 50k
Zin Differential	Ohm	46k 100k
Zin Each Line to Gnd	Ohm	23k 50k
Common Mode Range	V	25 max 60 max
Direct (1 V_{L-L})		
Input Signal Type		Sin and Cos resolver signals referenced to converter internal DC reference V.
Sin/Cos Voltage Range	Vrms	1 V nominal, 1.15 V max
Max Voltage w/o Damage		15 V continuous 100 V Peak Transient
Input Impedance	Ohm	Zin > 20M//10 pF voltage follower
REFERENCE SYNTHESIZER		
±Sig/Ref Phase Shift	Deg	45 typ, 60 max
DIGITAL INPUT/OUTPUT		
Logic Type		TTL/CMOS compatible
Inputs		Logic 0 = 0.8 V max Logic 1 = 2.0 V min Loading = 30 µA max P.U. current source to +5 V//5 pF max CMOS transient protected
Inhibit ($\overline{INH}$)		Logic 0 inhibits Data stable after 0.5 µs
Enable MSB's ($\overline{EM}$)(3)		Logic 0 enables Logic 1 High Z
Pull down		30µA
Enable LSB's ($\overline{EL}$)(3)		Logic 0 enables Logic 1 High Z
Pull down		30µA
Resolution Control (A) (SD-14590 only) (Unused Output Data Bits Are Set to 0)		1 14 bits 0 16 bits

TABLE 1. SD-14590/91/92 SPECIFICATIONS (contd)

PARAMETER	UNIT	VALUE
Output Parallel Data	bits	14 or 16 parallel lines; natural binary angle, positive logic
Converter Busy (CB)		0.4 to 2 µs positive pulse; leading edge initiates counter update.
BIT		Logic 1 for fault.
Drive Capability		50 pF plus rated logic drive. Logic 0; 1 TTL load, 1.6 mA at 0.4 Vmax Logic 1; 10 TTL loads 0.4 mA at 2.8 V min High Z; 10 µA//5 pF max Logic 0; 100 mV max driving CMOS Logic 1; +5 V supply minus 100 mV min driving CMOS
ANALOG OUTPUTS		
Velocity (VEL)		See TABLES 3 and 4
AC error (e)	mV rms	3.125 16 bit mode 6.130 14 bit mode
Bias Voltage (V)		1/3 Vs ±10%
Load	kOhm	3 min
DYNAMIC CHARACTERISTICS		See TABLE 3.
POWER SUPPLY CHARACTERISTICS		
Nominal Voltage		+15 V +5 V
Voltage Range	±%	5 10
Max Voltage w/o Damage	V	+18 +8
Current	mA max	25 10
TEMPERATURE RANGES		
Operating		
-30X	°C	0 to +70
-10X	°C	-55 to +125
Storage	°C	-65 to +150
PHYSICAL CHARACTERISTICS		
Size	in. (mm)	1.9 x 0.78 x 0.21 (48.3 x 19.8 x 5.3) 36 Pin Double Dip
Weight	oz	0.7 max (20 g)
TRANSFORMERS CHARACTERISTICS (See ordering information for list of Transformers. Reference Transformers are Optional for Both Solid-State and Voltage Follower Input Options.)		
400 Hz TRANSFORMERS		
Reference Transformer		
Carrier Frequency Range		360 - 1000 Hz
Voltage Range		18 - 130 V
Input Impedance		40 kΩ min
Breakdown Voltage to GND		1200 V peak

TABLE1. SD-14590/91/92 SPECIFICATIONS (contd)

PARAMETER	UNIT	VALUE
TRANSFORMERS CHARACTERISTICS (Cont'd)		
Signal Transformer		
Carrier Frequency Range		360-1000 Hz
Breakdown Voltage to GND		700 V peak
Minimum Input Impedances (Balanced)		Synchro $Z_{IN}(Z_{SO})$ | Resolver Z_{IN}
90 V $_{L-L}$		180 Ω | 100k Ω
26 V $_{L-L}$		- | 30k Ω
11.8 V $_{L-L}$		20k Ω | 30k Ω
60 Hz TRANSFORMERS		
Reference Transformer		
Carrier Frequency Range		47 - 440 Hz
Input Voltage Range		80 - 138 V rms; 115 V rms nominal resistive
Input Impedance		600 kΩ min resistive
Input Common Mode Voltage		500 V rms transformer isolated
Output Description		+R (in phase with RH-RL) and - R (in phase with RL- RH) derived from op-amps. Short-Circuit proof.
Output Voltage		3.0 V nominal riding on ground reference V. Output Voltage level tracks input level.
Power Required		4 mA typ, 7 mA max from +15 V supply.
Signal Transformer		
Carrier Frequency Range		47 - 440 Hz
Input Voltage Range		10 - 100 V rms L-L; 90 V rms L-L nominal
Input Impedance		148 kΩ min L-L balanced resistive
Input Common Mode Voltage		±500 V rms transformer isolated
Output Description		Resolver output: - sine (- S) + cosine (+C) derived from op-amps. Short-circuit proof.
Output Voltage		1.0 V rms nominal riding on ground reference V. Output voltage level tracks input level.
Power Required		4 mA typ, 7 mA max from +15 V supply.

Notes:
(1) Pin programmable for SD-14590 only; SD-14591 is 14 bits and SD-14592 is 16 bits.
(2) See TABLE 6.
(3) See Logic Input/Output section.

INTRODUCTION

The circuit shown in FIGURE 1, the SD-14590/91/92 block diagram, consists of three main parts: the signal input; a feedback loop whose elements are the control transformer, demodulator, error processor, VCO and up-down counter; and digital interface circuitry including various latches and buffers.

SIGNAL INPUTS

The SD-14590/91/92 series offer three input options: synchro, resolver, and direct. In a synchro or resolver mode, shaft angle data is transmitted as the ratio of carrier amplitudes across the input terminals. Synchro signals, which are of the form sinθ cosωt, sin(θ + 120°)cosωt, and sin(θ + 240°)cosωt are internally converted to resolver format; sinθcosωt and cosθcosωt. Direct inputs accept 1 Vrms inputs in resolver form, (sinθcosωt and cosθcosωt) and are buffered prior to conversion. FIGURE 2 illustrates synchro and resolver signals as a function of the angle θ.

The solid-state signal and reference inputs are true differential inputs with high AC and DC common mode rejection. *Input impedance is maintained with power off.*

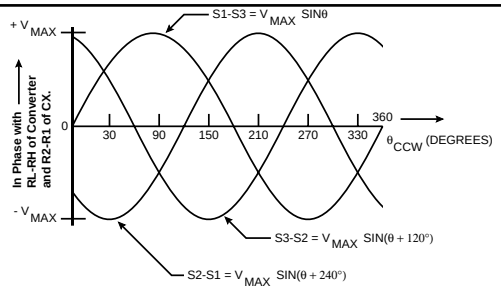
SOLID-STATE BUFFER INPUT PRODUCTION: TRANSIENT VOLTAGE SUPPRESSION

The solid-state signal and reference inputs are true differential inputs with high AC and DC common rejection so most applications will not require units with isolation transformers. Input impedance is maintained with power off. The current AC peak +DC common mode voltage should not exceed the values in TABLE 1.

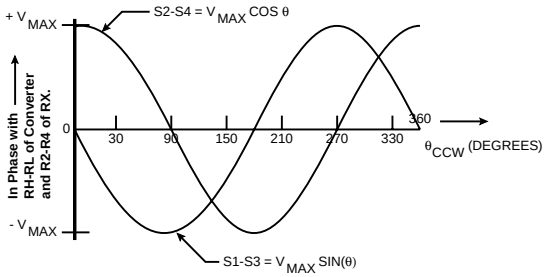
90 V line-to-line systems may have voltage transients which exceed the 500 V specification. These transients can destroy the thin-film input resistor network in the hybrid. Therefore, 90 V_{L-L} solid-state input modules may be protected by installing voltage suppressors as shown. Voltage transients are likely to occur whenever synchro or resolver are switched on and off. For instance, a 1000 V transient can be generated when the primary of a CX or TX driving a synchro or resolver input is opened. See FIGURE 3.

FEEDBACK LOOP

The feedback loop produces a digital angle ϕ which tracks the analog input angle θ to within the specified accuracy of the con-

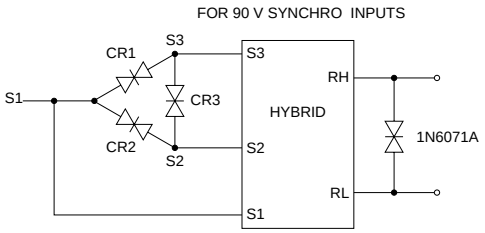


Standard Synchro Control Transmitter (CX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ).

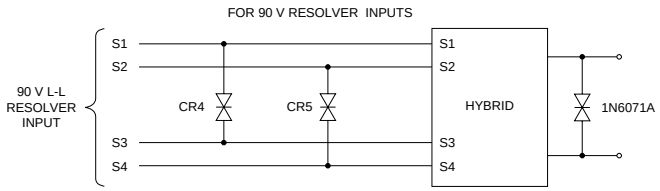


Standard Resolver Control Transmitter (RX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ) With R2-R4 Excited.

FIGURE 2. SYNCHRO AND RESOLVER SIGNALS



CR1, CR2, and CR3 are 1N6068A, bipolar transient voltage suppressors or equivalent.



CR4 and CR5 are 1N6068A, bipolar transient voltage suppressors or equivalent.

FIGURE 3. CONNECTIONS FOR VOLTAGE TRANSIENT SUPPRESSORS

verter. The control transformer performs the following trigonometric computation:

$$\sin(\theta - \phi) = \sin\theta\cos\phi - \cos\theta\sin\phi$$

where θ is the angle representing the resolver shaft position, and ϕ is the digital angle contained in the up/down counter. The tracking process consists of continually adjusting ϕ to make $(\theta - \phi) = 0$, so that ϕ will represent the shaft position θ. The output of the demodulator is an analog DC level proportional to $\sin(\theta - \phi)$. The error processor receives its input from the demodulator and integrates this $\sin(\theta - \phi)$ error signal which then drives a Voltage Controlled Oscillator (VCO). The VCO's clock pulses are accumulated by the up/down counter. The velocity voltage accuracy, linearity and offset are determined by the quality of the VCO. Functionally, the up/down counter is an incremental integrator. Therefore, there are two stages of integration which make the converter a Type II tracking servo. In a Type II servo, the VCO always settles to a counting rate which makes $d\phi/dt$ equal to $d\theta/dt$ without a lag. The output data will always be fresh and available as long as the maximum tracking rate of the converter is not exceeded.

SYNTHESIZED REFERENCE

The synthesized reference section of the SD-14590 eliminates errors caused by quadrature voltage. Due to the inductive nature of synchros and resolvers, their signals lead the reference signal (RH and RL) by about 6°. When an uncompensated reference signal is used to demodulate the control transformer's output, quadrature voltages are not completely eliminated. In a 14-bit converter it is not necessary to compensate for the reference signal's phase shift. A 6° phase shift will, however, cause problems for the one minute accuracy converters. As shown in FIGURE 1, the converter synthesizes its own $\cos(\omega t + \alpha)$ reference signal from the $\sin\theta\cos(\omega t + \alpha)$, $\cos\theta\cos(\omega t + \alpha)$ signal inputs and from the $\cos\omega t$ reference input. The phase angle of the synthesized reference is determined by the signal input. The reference input is used to choose between the +180° and -180° phases. The synthesized reference will always be exactly in phase with the signal input, and quadrature errors will therefore be eliminated. The synthesized reference circuit also eliminates the 180° false error null hangup.

Quadrature voltages in a resolver or synchro are by definition the resulting 90° fundamental signal in the nulled out error voltage (e) in the converter. A digital position error will result due to the interaction of this quadrature voltage and a reference phase shift between the converter signal and reference inputs. The magnitude of this error is given by the following formula:

$$\text{Error} = \text{Quad/Full Scale (FS) signal} * \tan(\alpha)$$

Where: Error is in radians
Quad/FS signal is per unit quadrature input level.
α = signal to reference phase shift in degrees.

A typical example of the magnitude of this source of error is as follows:

Quad/FS signal = .001
α = 6
Error = 0.35 min ≈1 LSB in the 16th bit.

Note: Quad/FS is composed of static quadrature which is specified by the resolver or synchro supplier plus the speed voltage which is given by:

$$\text{Speed Voltage} = \text{rotational speed/carrier frequency}$$

Where: Speed Voltage is the per unit ratio of electrical rotational speed in RPS divided by carrier frequency in Hz.

This error is totally negligible for 14-bit converters. For 16-bit converters where the highest accuracy possible is needed and where the quadrature and phase shift specifications can be higher, this source of error could be significant. The reference synthesizer circuit in the converter which derives the reference from the input signal essentially sets α to zero resulting in complete rejection of the quadrature.

DIGITAL INTERFACE

The digital interface circuitry has three main functions: to latch the output bits during an inhibit command so that the stable data can be read; to furnish both parallel and three-state data formats; and to act as a buffer between the internal CMOS logic and the external TTL logic.

In the SD-14590, applying an inhibit command will lock the data in the transparent latch without interfering with the continuous tracking of the feedback loop. Therefore, the digital angle is always updated, and the inhibit can be applied for an arbitrary amount of time. The inhibit transparent latch and the 50 ns delay are part of the inhibit circuitry. The inhibit circuitry is described in detail in the logic input/output section.

LOGIC INPUT/OUTPUT

Logic angle outputs consist of 14 or 16 parallel data bits and CONVERTER BUSY (CB). All logic outputs are short-circuit proof to ground and +5 Volts. The CB output is a positive, 0.4 to 2.0 µs pulse. Data changes about 50 ns after the leading edge of the pulse because of an internal delay. Data is valid 0.2 µs after the leading edge of CB, the angle is determined by the sum of the bits at logic "1." Digital outputs are three-state and two bytes wide. For 14 bit only: 1-6 (MSB's) are enabled by signal $\overline{EM}$, bits 7-14 (LSB's) are enabled by the signal $\overline{EL}$; for 14/16 program-

mable: 1-8 (MSB's) are enabled by signal $\overline{EM}$, 9-14 (LSB's 14 bit) or 9-16 (LSB's 16 bit) are enabled by the signal $\overline{EL}$. Outputs are valid (logic "1" or "0") 150 ns max after setting $\overline{EM}$ or $\overline{EL}$ low, and are high impedance within 100 ns max of setting $\overline{EM}$ or $\overline{EL}$ high. Both $\overline{EM}$ and $\overline{EL}$ are internally pulled-down to +5 V at 30 µA max.

The inhibit ($\overline{INH}$) input locks the transparent latch so the bits will remain stable while data is being transferred (See FIGURE 1). The output is stable 0.5 µs after $\overline{INH}$ is driven to logic "0," see FIGURE 4. A logic "0" at the T input latches the data, and a logic "1" applied to T will allow the bits to change. The inhibit transparent latch prevents the transmission of invalid data when there is an overlap between CB and $\overline{INH}$. While the counter is not being updated, CB is at logic "0" and the $\overline{INH}$ latch is transparent.

When CB goes to logic "1," the $\overline{INH}$ latch is locked. If CB occurs after $\overline{INH}$ has been applied, the latch will remain locked and its data will not change until CB returns to logic "0." If $\overline{INH}$ is applied during CB, the latch will not lock until the CB pulse is over. The purpose of the 50 ns delay is to prevent a race condition between CB and $\overline{INH}$ where the up-down counter begins to change as an $\overline{INH}$ is applied. Whenever an input angle change occurs, the converter changes the digital angle in 1 LSB steps and generates a converter busy pulse. Output data change is initiated by the leading edge of the CB pulse, delayed by 50 ns, nominal. Valid data is available at the outputs 0.2 µs after the leading edge of CB, see FIGURE 5.

RESOLUTION CONTROL

Resolution control is via one logic input A. The SD-14590 (not the SD-14591 or SD-14592) has programmable resolution.

BUILT-IN-TEST

The Built-In-Test output (BIT) monitors the level of error (D) from the demodulator. D represents the difference in the input and output angles and ideally should be zero. If it exceeds approximately 65 LSBs (of the selected resolution), the logic level at BIT will change from a logic 0 to logic 1. This condition will occur during a large step and reset after the converter settles out. BIT will also change to logic 1 for an over-velocity condition, because the converter loop cannot maintain input-output and/or if the converter malfunctions where it cannot maintain the loop at a null. BIT will also be set if a total Loss-of-Signal (LOS) and/or a Loss-of-Reference (LOR) occurs.

TABLE 2. DIGITAL ANGLE OUTPUTS

BIT	DEG/BIT	MIN/BIT
1 MSB	180	10,800
2	90	5,400
3	45	2,700
4	22.5	1,350
5	11.25	675
6	5.625	387.5
7	2.813	168.75
8	1.405	84.38
9	0.7031	42.19
10	0.3516	21.09
11	0.1758	10.55
12	0.0879	5.27
13	0.0439	2.64
14	0.0220	1.32
15	0.0110	0.66
16	0.0055	0.33

Note: $\overline{EM}$ enables the MSBs and $\overline{EL}$ enables the LSBs.

DYNAMIC PERFORMANCE

A Type II servo loop (Kv = ∞) and very high acceleration constants give the SD-14590 superior dynamic performance, as listed in TABLE 3. If the power supply voltages are not the ±15 VDC nominal values, the specified input rates will increase or decrease in proportion to the fractional change in voltage. A Control Loop Block Diagram is shown in FIGURE 6, and an Open Loop Bode Plot is shown in FIGURE 7. The values of the transfer function coefficients are shown in TABLE 3.

An inhibit input, regardless of its duration, does not affect the converter update. A simple method of interfacing to a computer asynchronously to CB is: (A) apply the inhibit, (B) wait 0.5 µs minimum, (C) transfer the data and (D) release the inhibit.

As long as the converter maximum tracking rate is not exceeded, there will be no lag in the converter output. If a step input

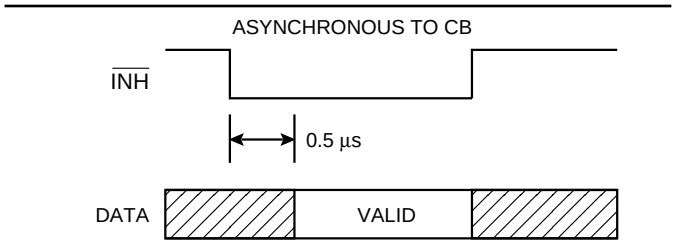


FIGURE 4. INHIBIT TIMING DIAGRAM

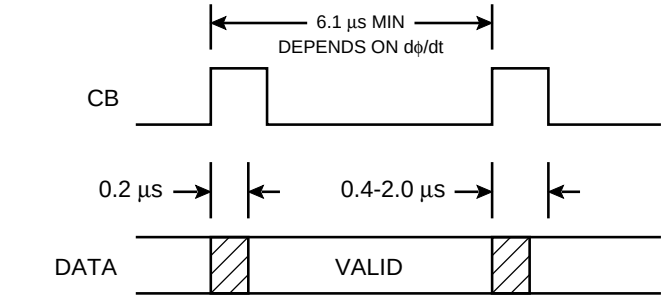


FIGURE 5. CONVERTER BUSY TIMING DIAGRAM

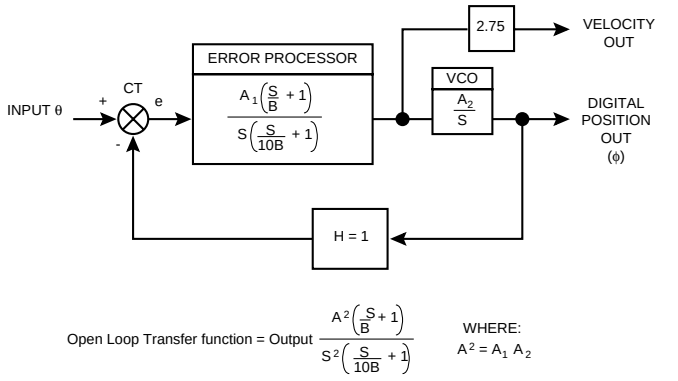


FIGURE 6. CONTROL LOOP BLOCK DIAGRAM

TABLE 3. DYNAMIC CHARACTERISTICS					
PARAMETER	UNITS	BANDWIDTH			
		400 HZ		60 HZ	
RESOLUTION	BITS	14	16	14	16
Input Frequency	Hertz	360-1000		47-1000	
Tracking Rate	RPS min	10	2.5	2.5	0.61
Bandwidth	Hertz	54	*	14	*
K_a	1/sec^2 nom	12500	*	780	*
A1	1/sec nom	0.31	*	0.078	*
A2	1/sec nom	40k	*	10k	*
A	1/sec nom	112	*	28	*
B	1/sec nom	52	*	13	*
acc-1 LSB lag	Deg/sec^2 nom	275k	69	17	4.3
Settling Time	ms max	300	800	1400	3400

Note: * means the same as value to the left.

occurs, as when the power is initially applied, the response will be critically damped. FIGURE 8 shows the response to a step input.

After initial slewing at the maximum tracking rate of the converter, there is one overshoot (which is inherent in a Type II servo). The overshoot settling to final value is a function of the small signal settling time. For Velocity output, the simple filter shown in FIGURE 9 will eliminate the one overshoot for step velocity input and will filter the carrier frequency ripple.

ANALOG OUTPUTS

The analog outputs are velocity (VEL) and AC error (e). Both outputs can swing ±3.5 V min. with respect to V.

The AC error, e, is proportional to the error (θ - ϕ) with a scaling of 6.310 mV/LSB (14-bit mode), and 3.125 mV/LSB (16-bit mode). Velocity output characteristics are listed in TABLE 4.

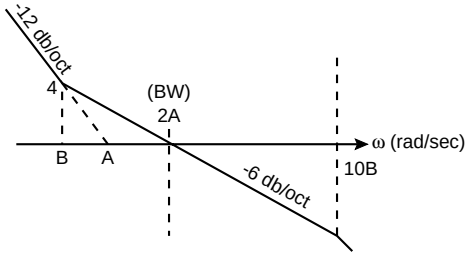


FIGURE 7. OPEN LOOP BODE PLOT

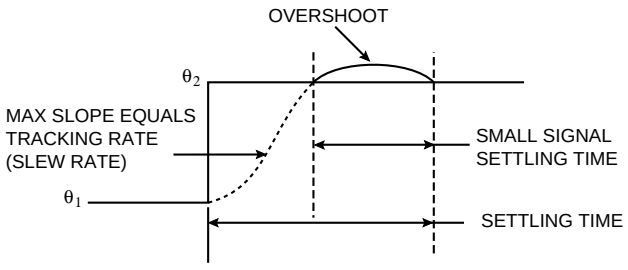


FIGURE 8. RESPONSE TO A STEP INPUT

TABLE 4. VELOCITY CHARACTERISTICS			
PARAMETER	UNITS	STANDARD	
		TYP	MAX
Polarity		Positive for increasing angle.	
Output Voltage	V	3.5	
Voltage Scaling	RPS	See Voltage Scaling Table 5.	
Scale Factor	%	10	15
Scale Factor TC	PPM/°C	100	200
Reversal Error	%	1	2
Reversal Error TC	PPM/°C	25	50
Linearity	% output	1	2
Linearity TC	PPM/°C	25	50
Zero Offset	mV	15	35
Zero Offset TC	µV/°C	25	50
Load	k Ohm	-	3 min

TABLE 5. VELOCITY VOLTAGE SCALING		
BW	RESOLUTION (values in RPS/Volt)	
	14	16
HI	2.8	0.71
LO	0.71	0.17
Note: If the resolution is changed while the input is changing, then the velocity output voltage and the digital output will have a transient until it settles to the new velocity scaling at a speed determined by the bandwidth. If additional information is required, consult the factory.		

VELOCITY OUTPUT

The Velocity output (VEL) from the SD-14590 is a DC voltage proportional to angular velocity $d\theta/dt = d\phi/dt$. The velocity input is the second integrator, as shown in FIGURE 6. Its linearity is dependent solely on the linearity of the voltage controlled oscillator (VCO). Due to the highly linearized VEL output, the electromechanical tachometer can now be eliminated from motion control systems. Bandwidth (BW) and the acceleration constant (Ka) can be determined from the formula shown:

$$BW(Hz) = BW(rad/sec)/2\pi$$

$$Ka = A^2$$

Outputs e and VEL are not required for normal operation of the converter. V is used as an internal DC reference with the direct input option. Maximum loading on V is 40k ohm; maximum loading for e and VEL is 3k ohm. The velocity characteristics are shown in TABLES 4 and 5. Output e is not closely controlled or characterized. Consult the factory for further information.

FIGURES 10, 11, 12 are the synchro, resolver, and direct input connection diagrams respectively.

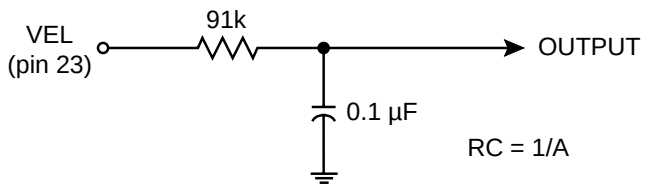


FIGURE 9. VELOCITY FILTER

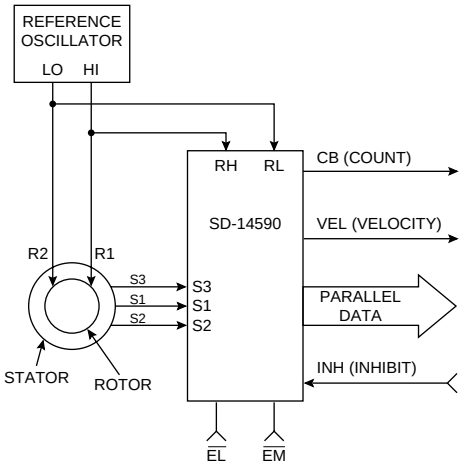


FIGURE 10. SYNCHRO INPUT CONNECTION DIAGRAM

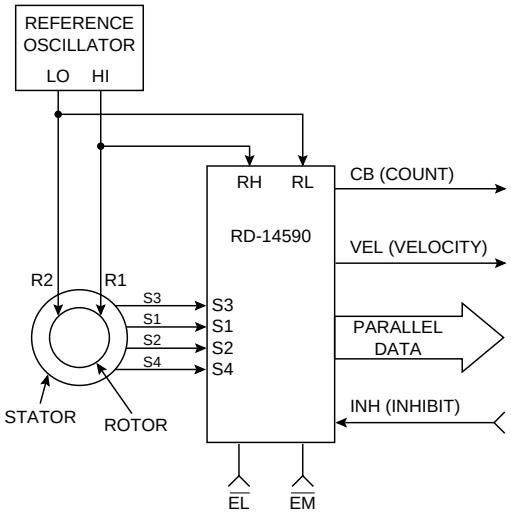


FIGURE 11. RESOLVER INPUT CONNECTION DIAGRAM

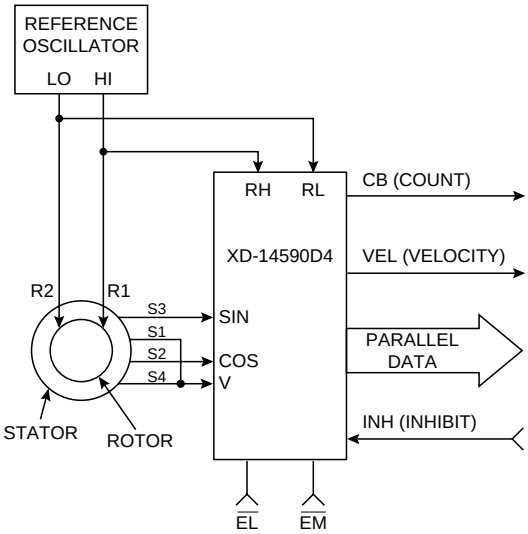
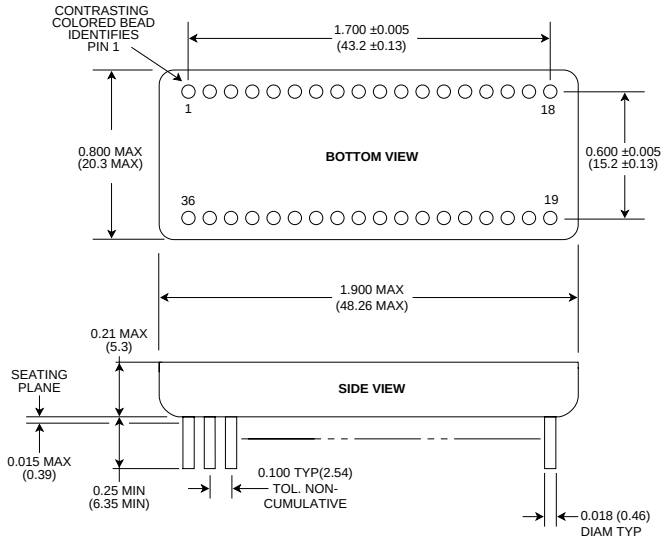


FIGURE 12. DIRECT INPUT CONNECTION DIAGRAM

TABLE 6. OVERALL ACCURACY (MIN.) VS. RESOLUTION		
ACCURACY GRADE (MINUTES)	RESOLUTION PROGRAMMED TO:	
	14 BIT	16 BIT
±1 +1 LSB	2.3	1.3
±2 + 1 LSB	3.3	2.3
±4 + 1 LSB	5.3	4.3

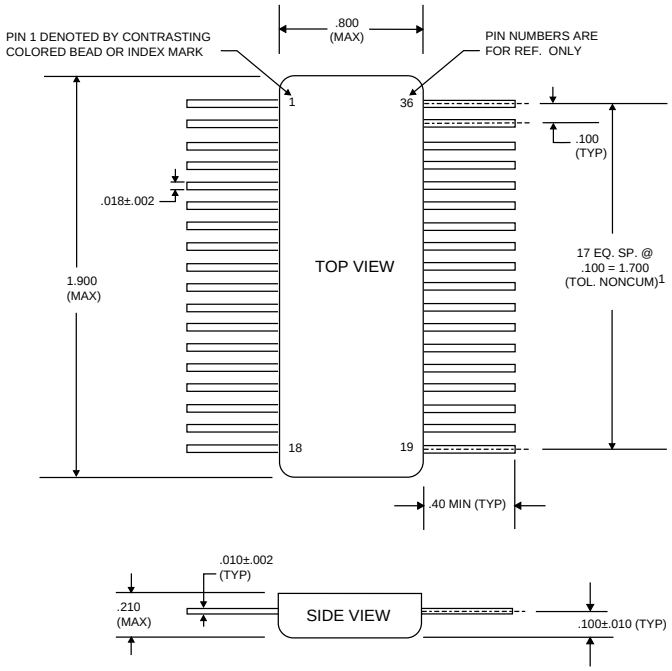
TABLE 7. SD-14590/91/92 PIN CONNECTION/FUNCTIONS			
PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	S1(R) S1(S) -	36	NC
2	S2(R) S2(S) +C(X)	35	NC (A for SD-14590)
3	S3(R) S3(S) +S(X)	34	$\overline{V}$
4	S4(R) - -	33	$\overline{INH}$
5	1 (MSB)	32	+15 V (Vs)
6	2	31	NC
7	3	30	BIT
8	4	29	GND
9	5	28	+5 V (VL)
10	6	27	$\overline{e}$
11	7	26	$\overline{EM}$
12	8	25	$\overline{EL}$
13	9	24	CB
14	10	23	VEL (θ)
15	11	22	*16 (LSB-16 BIT MODE)
16	12	21	*15
17	13	20	RL
18	14 (LSB-14 BIT MODE)	19	RH

Note:
1. "(R)" means resolver, "(S)" means synchro, and "(X)" means direct.
2. * - No Connection for 14-bit mode or SD-14591.



NOTES:
1. Dimensions shown are in inches (millimeters).
2. Lead identification numbers are for reference only.
3. Lead cluster shall be centered within ±0.01(0.25) of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements to MIL-STD-202E, Method 208C
5. Case is electrically floating.

FIGURE 13. SD-14590/91/92 MECHANICAL OUTLINE 36-PIN DDIP (KOVAR)



NOTES:
1. Dimensions are in inches.
2. Metric equivalents are given for information only.
3. Unless otherwise specified , tolerance is ± .005 inch (0.13mm).
4. Lead identification numbers are for reference only.
(Consult factory for availability.)

FIGURE 14. SD-14590/91/92 MECHANICAL OUTLINE 36-PIN FLAT PACK (CERAMIC)

TRANSFORMERS

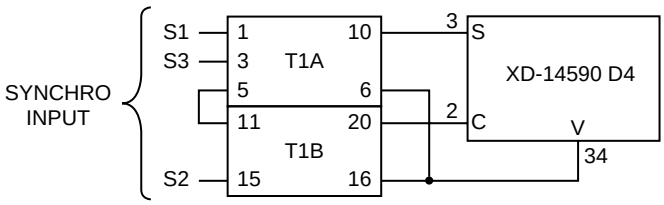
FIGURE 15 illustrates the Transformer Connection Diagram. These transformers are designed for the voltage follower buffer input option to the SD-14590 (XD-14590 D4 or XD-14590 D5). However, the reference transformers may also be used with the solid-state buffer input options.

Passive transformers are considerably larger in size for 60 Hz than for 400 Hz. To minimize size, active transformers are utilized over passive devices for 60 Hz. These active 60 Hz transformers have op-amp outputs and require connection to a +15 V power supply.

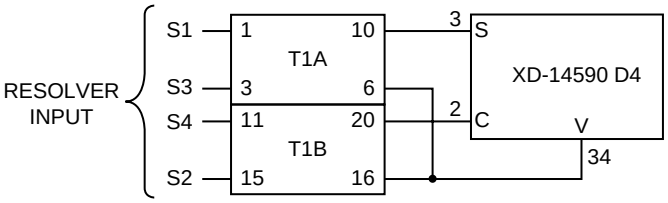
---

400 Hz MODELS

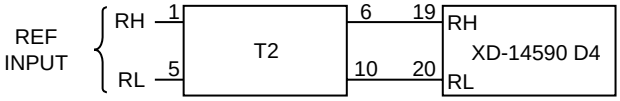
400 Hz SYNCHRO TRANSFORMER T1 21044 OR 21045



400 Hz RESOLVER TRANSFORMER T1 21046 OR 21047 OR 21048

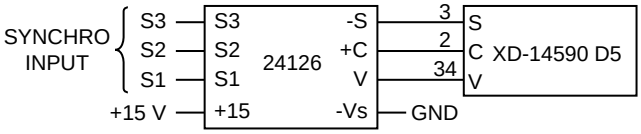


400 Hz REF TRANSFORMER 21049



60 Hz MODELS

60 Hz SYNCHRO TRANSFORMER 24126



60 Hz REF TRANSFORMER 24133

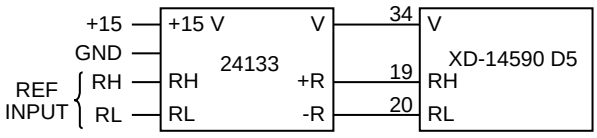


FIGURE 15. TRANSFORMER CONNECTION DIAGRAM

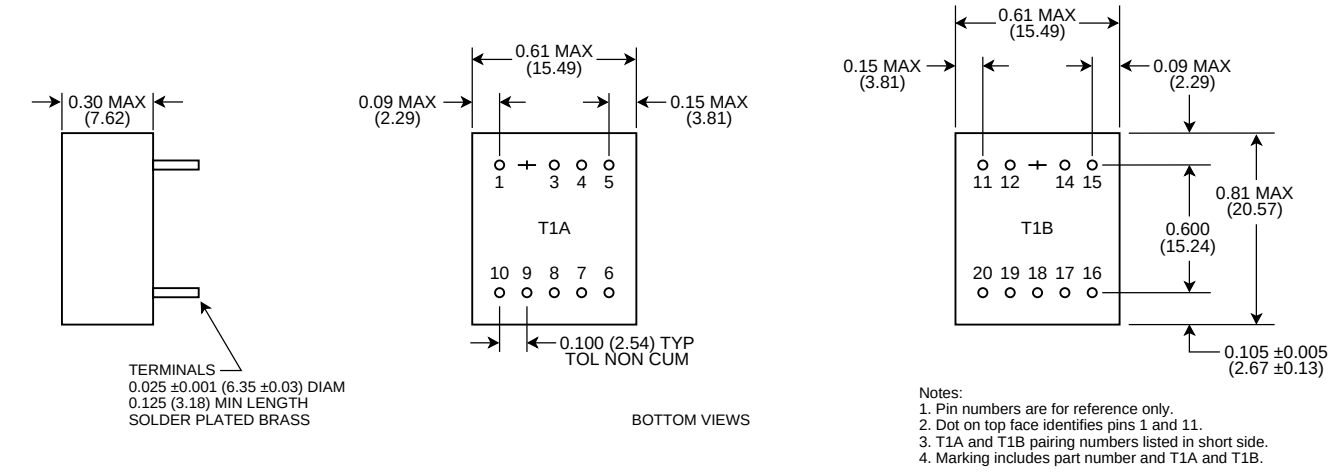
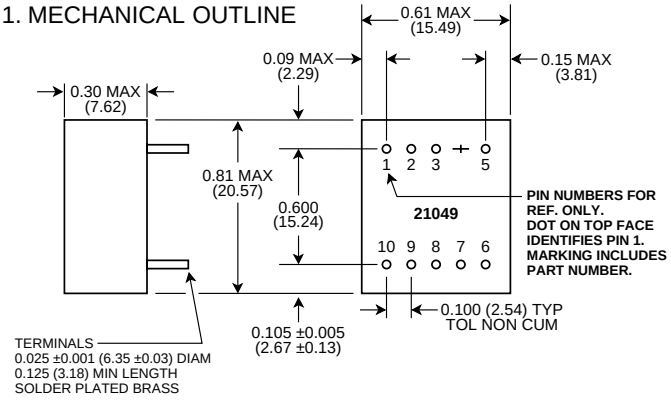


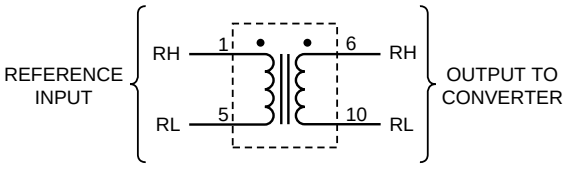
FIGURE 16A. 400 HZ SYNCHRO AND RESOLVER TRANSFORMER MECHANICAL OUTLINES AND ELECTRICAL SCHEMATICS

400 Hz REFERENCE TRANSFORMER DIAGRAMS (T2)

1. MECHANICAL OUTLINE



2. SCHEMATIC DIAGRAM



60 Hz SYNCHRO AND REFERENCE TRANSFORMER DIAGRAMS

The mechanical outline is the same for the synchro input transformer (24126) and the reference input transformer (24133), except for the pins. Pins for the reference transformer are shown in parenthesis ( ) below. An asterisk (*) indicates that the pin is omitted.

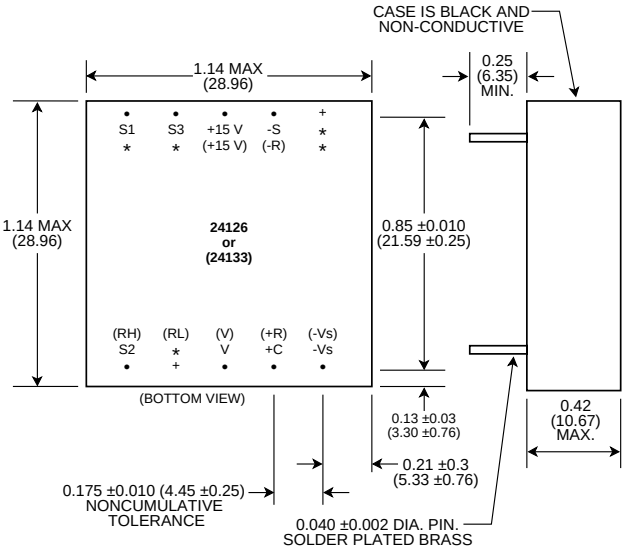


FIGURE 16B. TRANSFORMER MECHANICAL OUTLINES

ORDERING INFORMATION

XX-1459XXX-XXXX

Supplemental Process Requirements:
- S = Pre-Cap Source Inspection
- L = Pull Test
- Q = Pull Test and Pre-Cap Inspection
- Blank = None of the Above

Accuracy:
- 2 = ±5.2 Minutes
- 4 = ±2.6 Minutes
- 5 = ±1.3 Minutes (16 Bit only)

Process Requirements:
- 0 = Standard DDC Processing, no Burn-In (See table below.)
- 1 = MIL-PRF-38534 Compliant
- 2 = B*
- 3 = MIL-PRF-38534 Compliant with PIND Testing
- 4 = MIL-PRF-38534 Compliant with Solder Dip
- 5 = MIL-PRF-38534 Compliant with PIND Testing and Solder Dip
- 6 = B* with PIND Testing
- 7 = B* with Solder Dip
- 8 = B* with PIND Testing and Solder Dip
- 9 = Standard DDC Processing with Solder Dip, no Burn-In (See table below.)

Temperature Grade/Data Requirements:
- 1 = -55°C to +125°C
- 2 = -40°C to +85°C
- 3 = 0°C to +70°C
- 4 = -55°C to +125°C with Variables Test Data
- 5 = -40°C to +85°C with Variables Test Data
- 8 = 0°C to +70°C with Variables Test Data

Input:
- 1 = 11.8/400 Hz
- 2 = 90/400 Hz
- 3 = 90/60 Hz
- 4 = Direct/400 Hz
- 5 = Direct/60 Hz

Package:
- D = DIP
- F = Flat Pack (Consult factory for availability.)

Resolution:
- 0 = Programmable (14 or 16 Bits)
- 1 = 14 Bit
- 2 = 16 Bit

Input Type:
- RD = Resolver Input
- SD = Synchro Input
- XD = Direct Input

*Standard DDC Processing with burn-in and full temperature test — see table below.

STANDARD DDC PROCESSING		
TEST	**MIL-STD-883**	
	METHOD(S)	**CONDITION(S)**
INSPECTION	2009, 2010, 2017, and 2032	—
SEAL	1014	A and C
TEMPERATURE CYCLE	1010	C
CONSTANT ACCELERATION	2001	A
BURN-IN	1015, Table 1	—

TRANSFORMER ORDERING INFORMATION

Reference and signal transformers for the voltage follower buffer input converters must be ordered separately from the following table:

TYPE	FREQ.	REF. VOLTAGE	L-L VOLTAGE	PART NUMBERS	
				REF. XFMR	SIGNAL XFMR
Synchro	400 Hz	115 V	90 V	21049	21045*
Synchro	400 Hz	26 V	11.8 V	21049	21044*
Resolver	400 Hz	115 V	90 V	21049	21048*
Resolver	400 Hz	26 V	26 V	21049	21047*
Resolver	400 Hz	26 V	11.8 V	21049	21046*
Synchro†	60 Hz	115 V	90 V	24133-1 24133-3	24126-1 24126-3

* The part number for each 400 Hz synchro or resolver isolation transformer includes two separate modules as shown in the outline drawings.

† 60 Hz synchro transformers are available in two temperature ranges:
1 = -55°C to +105°C
3 = 0°C to +70°C

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