TOSHIBA Field-Effect Transistor Silicon N-Channel MOS Type

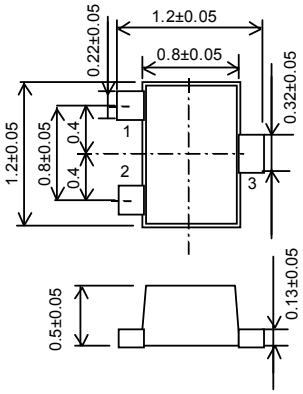
# SSM3K35MFV

○ High-Speed Switching Applications

○ Analog Switch Applications

- 1.2 V drive
- Low ON-resistance : $R_{on}$ = 20 Ω (max) (@$V_{GS}$ = 1.2 V)
  : $R_{on}$ = 8 Ω (max) (@$V_{GS}$ = 1.5 V)
  : $R_{on}$ = 4 Ω (max) (@$V_{GS}$ = 2.5 V)
  : $R_{on}$ = 3 Ω (max) (@$V_{GS}$ = 4.0 V)

Unit: mm




1.Gate
2.Source
3.Drain

VESM

| | |
|---|---|
| JEDEC | - |
| JEITA | - |
| TOSHIBA | 2-1L1B |

Weight: 1.5 mg (typ.)

## Absolute Maximum Ratings (Ta = 25˚C)

| Characteristic | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Drain–source voltage | | $V_{DSS}$ | 20 | V |
| Gate–source voltage | | $V_{GSS}$ | ±10 | V |
| Drain current | DC | $I_D$ | 180 | mA |
| | Pulse | $I_{DP}$ | 360 | |
| Drain power dissipation | | $P_D$ (Note 1) | 150 | mW |
| Channel temperature | | $T_{ch}$ | 150 | °C |
| Storage temperature | | $T_{stg}$ | −55~150 | °C |

Note 1: Mounted on an FR4 board
(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 0.585 $mm^2$)

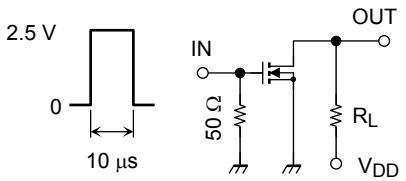
## Electrical Characteristics (Ta = 25°C)

| Characteristic | | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Gate leakage current | | $I_{GSS}$ | $V_{GS}$ = ±10 V, $V_{DS}$ = 0 V | — | — | ±10 | μA |
| Drain–source breakdown voltage | | $V_{(BR)\ DSS}$ | $I_D$ = 0.1 mA, $V_{GS}$ = 0 V | 20 | — | — | V |
| Drain cutoff current | | $I_{DSS}$ | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V | — | — | 1 | μA |
| Gate threshold voltage | | $V_{th}$ | $V_{DS}$ = 3 V, $I_D$ = 1 mA | 0.4 | — | 1.0 | V |
| Forward transfer admittance | | $\|Y_{fs}\|$ | $V_{DS}$ = 3 V, $I_D$ = 50 mA (Note 2) | 115 | — | — | mS |
| Drain–source ON-resistance | | $R_{DS\ (ON)}$ | $I_D$ = 50 mA, $V_{GS}$ = 4 V (Note 2) | — | 1.5 | 3 | Ω |
| | | | $I_D$ = 50 mA, $V_{GS}$ = 2.5 V (Note 2) | — | 2 | 4 | |
| | | | $I_D$ = 5 mA, $V_{GS}$ = 1.5 V (Note 2) | — | 3 | 8 | |
| | | | $I_D$ = 5 mA, $V_{GS}$ = 1.2 V (Note 2) | — | 5 | 20 | |
| Input capacitance | | $C_{iss}$ | $V_{DS}$ = 3 V, $V_{GS}$ = 0 V, f = 1 MHz | — | 9.5 | — | pF |
| Reverse transfer capacitance | | $C_{rss}$ | | — | 4.1 | — | |
| Output capacitance | | $C_{oss}$ | | — | 9.5 | — | |
| Switching time | Turn-on time | $t_{on}$ | $V_{DD}$ = 3 V, $I_D$ = 50 mA, $V_{GS}$ = 0 to 2.5 V | — | 115 | — | ns |
| | Turn-off time | $t_{off}$ | | — | 300 | — | |
| Drain–source forward voltage | | $V_{DSF}$ | $I_D$ = - 180 mA, $V_{GS}$ = 0 V (Note 2) | — | -0.9 | -1.2 | V |

Note 2: Pulse test

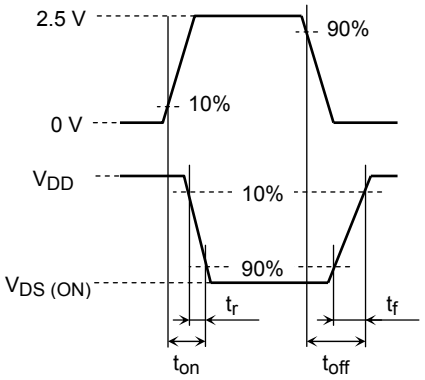
## Switching Time Test Circuit

### (a) Test Circuit



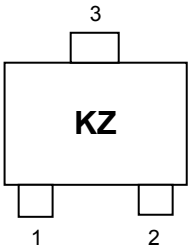

$V_{DD}$ = 3 V
D.U. ≦ 1%
$V_{IN}$: $t_r$, $t_f$ < 5 ns
($Z_{out}$ = 50 Ω)
Common Source
Ta = 25°C

### (b) $V_{IN}$

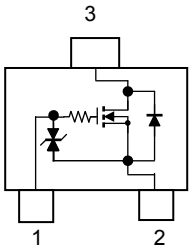



### (c) $V_{OUT}$

## Marking




## Equivalent Circuit (top view)




## Notice on Usage

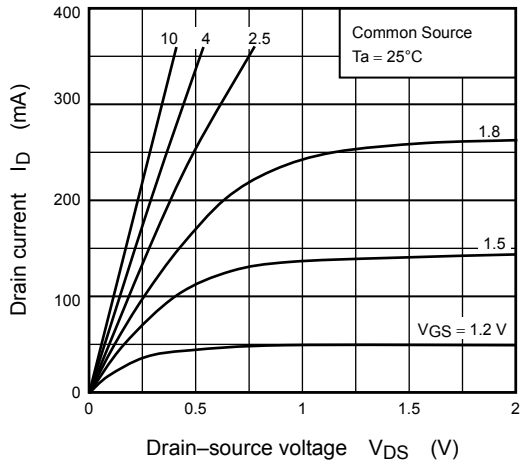
$V_{th}$ can be expressed as the voltage between gate and source when the low operating current value is $I_D$ = 1 mA for this product. For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than $V_{th}$ and $V_{GS\ (off)}$ requires a lower voltage than $V_{th}$. (The relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$.)

Take this into consideration when using the device.

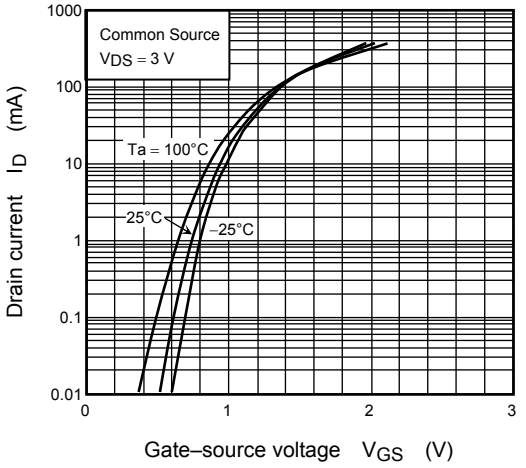
## Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

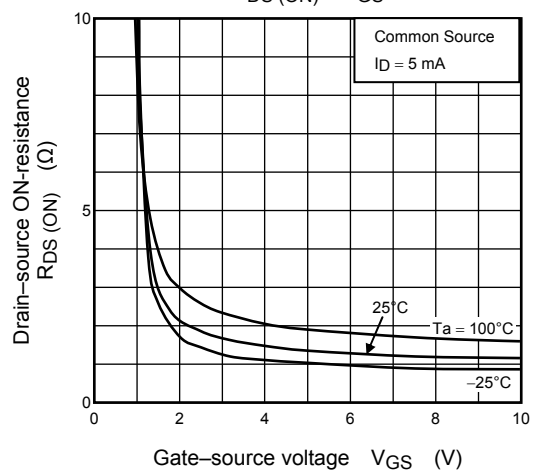
$I_D - V_{DS}$



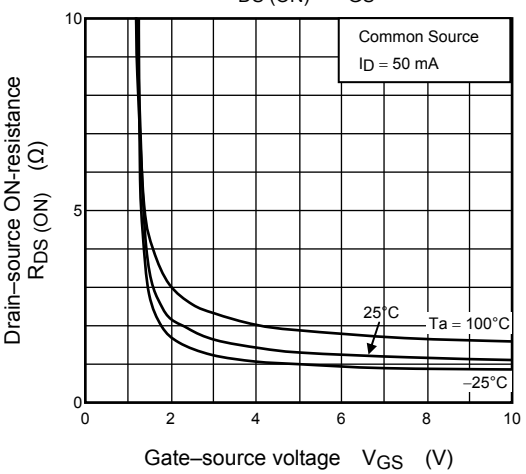

$I_D - V_{GS}$



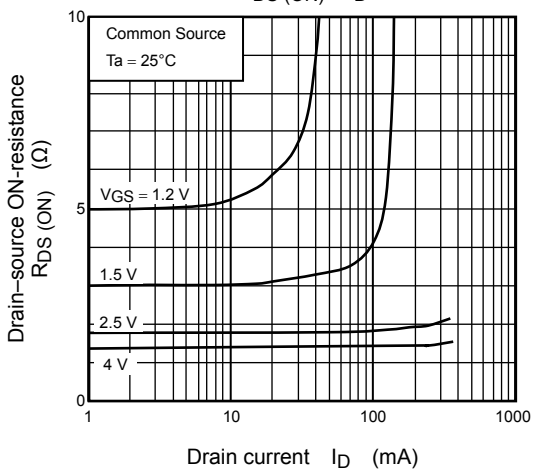

$R_{DS\ (ON)} - V_{GS}$



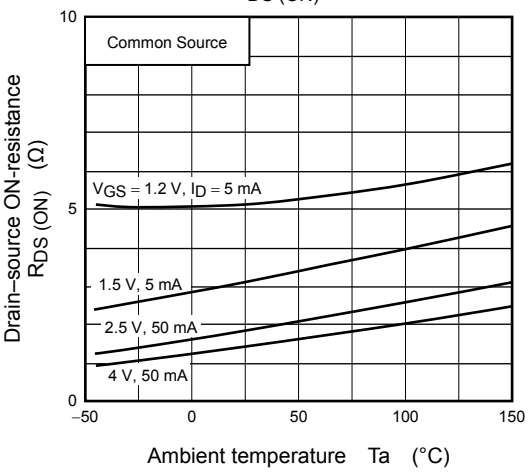

$R_{DS\ (ON)} - V_{GS}$



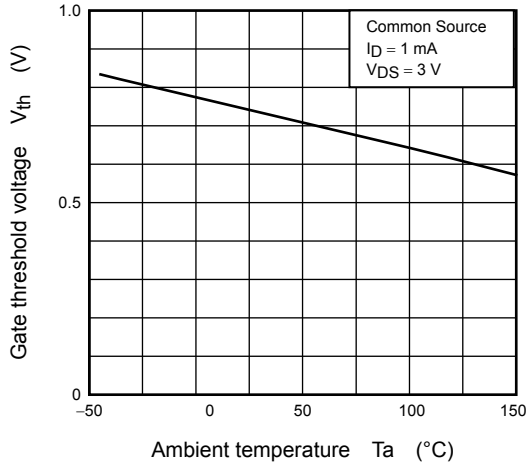

$R_{DS\ (ON)} - I_D$



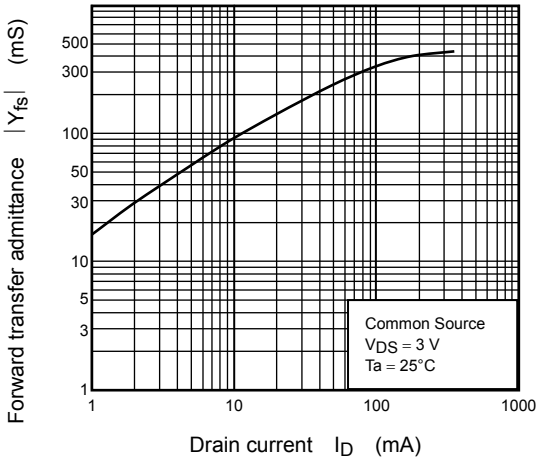

$R_{DS\ (ON)} - Ta$



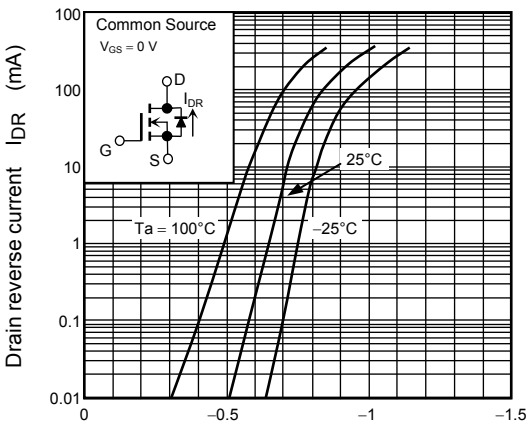
$V_{th}$ – Ta



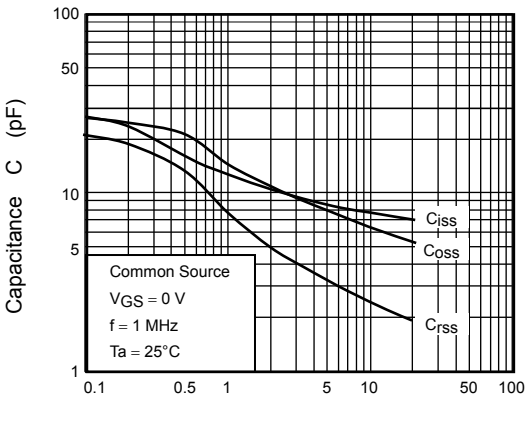

$|Y_{fs}|$ – $I_D$



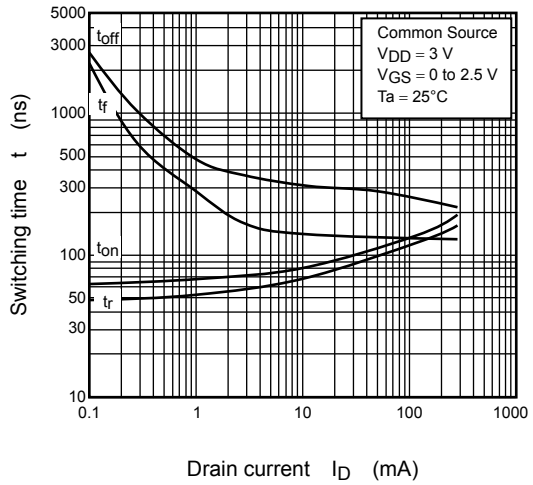

$I_{DR}$ – $V_{DS}$



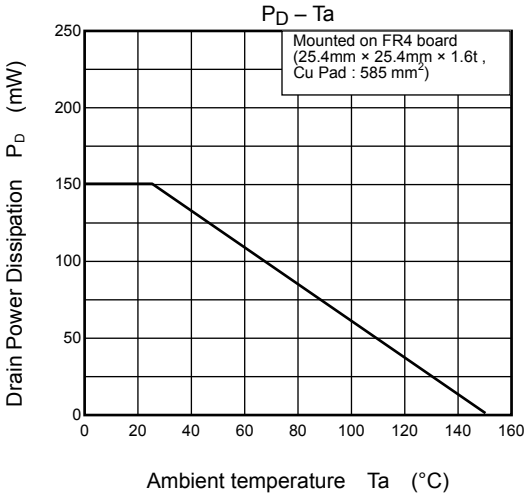

C – $V_{DS}$




t – $I_D$




$P_D$ – Ta



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20070701-EN GENERAL

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