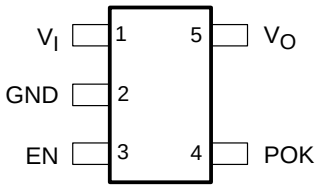
features

- **Low Dropout Voltage Regulator, 1.2-V**
- **150-mA Load Current Capability**
- **Power Okay (POK) Function**
- **Load Independent, Low Ground Current,150-μA**
- **Current Limiting**
- **Thermal Shutdown**
- **Low Sleep State Current (Off Mode)**
- **Fast Transient Response**
- **Low Variation Due to Load and Line Regulation**
- **Output Stable With Low ESR Capacitors**
- **TTL Logic Controlled Enable Input**

DBV PACKAGE
(TOP VIEW)



applications

- **Processor Powerup Sequencing**
- **Palmtop Computers, Laptops, and Notebooks**

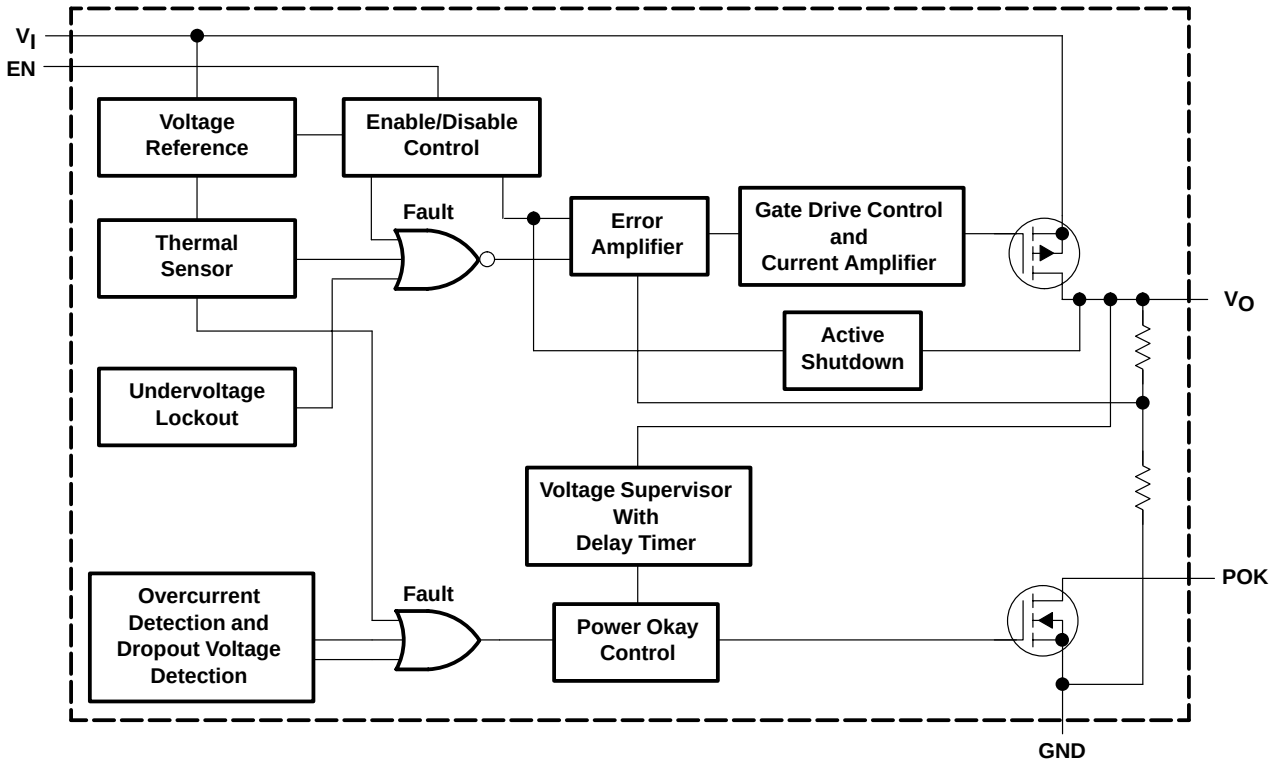
description

The TPPM0125 is a low dropout voltage regulator with an output tolerance of ±2% over the operating range. The device is optimized for low noise applications and has a low quiescent current (enable <0.8 V). The device has a low dropout voltage at full load (150 mA). The power okay function monitors the output voltage and indicates when an error occurs in the system (active low). In the event of an output fault such as overcurrent, thermal shutdown, or dropout, the power okay output is pulled low (open drain).

The TPPM0125 has a fast transient response recovery capability in the event of load transition from heavy load to light load. The device also minimizes overshoot during this condition. During power down, the output capacitor and load are de-energized through the internal active shutdown clamp, which is turned on when the device is disabled.

The TPPM0125 requires a small output capacitor for stability with low ESR. An input capacitor is not required unless the bulk ac capacitor is placed away from the device or the power supply is a battery. In this situation, a 1-μF capacitor is recommended for the application. Low ESR ceramic capacitors may be used with the device to reduce board space in power applications, a key concern in hand-held wireless devices.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
EN	3	I	Enable/shutdown input (active high)
GND	2	I	Ground
POK	4	I	Power okay indicator
V_I	1	I	Input supply voltage
V_O	5	O	Output voltage

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Main input voltage range, V_I (see Notes 1 and 2) . . . . . 0 V to 7 V
Enable input voltage range, $V_{(EN)}$ (see Notes 1 and 2) . . . . . 0 V – V_I
Power okay output voltage range $V_{(POK)}$, (see Notes 1 and 2) . . . . . 0 V – V_I
Regulated output current limit, I_O . . . . . 400 mA
Continuous power dissipation, P_D, T_A = 25°C . . . . . 0.5 W
Electrostatic discharge susceptibility, $V_{(HBMESD)}$, (see Note 3) . . . . . 2 kV
Junction temperature, T_J, ... 150°C
Storage temperature range, T_{stg} . . . . . –55°C to 150°C
Lead temperature (soldering, 10 sec) . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to GND.
2. Absolute negative voltage on these terminals should not go below –0.5 V.
3. The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each terminal. Devices are ESD sensitive. Handling precautions are recommended.

recommended operating conditions

	MIN	TYP	MAX	UNIT
Main input voltage, V_I (see Notes 1 and 2)	3		5.25	V
Enable input voltage, $V_{(EN)}$ (see Notes 1 and 2)	0		V_I	V
Power okay voltage, $V_{(POK)}$ (see Notes 1 and 2)	0		V_I	V
Operating ambient temperature, T_A	0		70	°C

NOTES: 1. All voltage values are with respect to GND.
2. Absolute negative voltage on these terminals should not go below –0.5 V.

electrical characteristics, T_A = 25°C, V_I = 5 V, $V_{(EN)} = V_I$, I_O = 100 µA, C_L = 1 µF (unless otherwise noted)

regulator V_O

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_O	Output voltage	I_O = 25 mA		1.2		V
	Output voltage accuracy	I_O = 0	–1%		1%	
		I_O = 50 mA, T_A = 0°C to 70°C (see Note 4)	–2%		2%	
I_Q	Quiescent supply current	$V_{(EN)} \le 0.8$ V		1		µA
$I_{(GND)}$	Ground terminal current (see Note 5)	I_O = 0		150		µA
		I_O = 150 mA		150		
I_L	Output load current		150			mA
$I_{(Limit)}$	Output current limit	V_O = 0	160	300		mA
$\Delta V_{(LNR)}$	Line regulation	V_I = 3 V to 5.25 V		10		mV
$\Delta V_{(LDR)}$	Load regulation	I_O = 0.1 mA to150 mA, See Note 6		2%	3%	
$V_I - V_O$	Dropout voltage	I_O = 100 µA		1		V
		I_O = 150 mA		1		
C_L	Load capacitance	ESR and capacitance tradeoffs		1		µF
$I_{(REV)}$	Reverse output current on V_I	V_I = GND, V_O = regulated voltage			50	µA

NOTES: 4. Assured by design, not tested in production.
5. Ground terminal current is the regulator quiescent current drawn from the supply to support the load current.
6. Regulation is measured at constant junction temperature using low duty cycle pulse testing. Devices are tested for load regulation in the load range from 0.1 mA to 150 mA.

enable input

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Regulated shutdown	V_I = 3 V to 5.25 V regulated shutdown			0.8	V
V_{IH}	Regulated enabled	V_I = 3 V to 5.25 V regulated enabled	2			V
$I_{(EN)}$	Enable input current	Shutdown, $V_{IL} \le 0.8$ V		0.01		µA
		Enabled, $V_{IH} \ge 2$ V		0.01		
	Resistance discharge	$V_{(EN)} \le 0.8$ V		500		Ω

thermal protection (see Note 4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$T_{(SD)}$	Thermal shutdown			165		°C
$T_{(SDHYS)}$	Hysteresis			15		°C

NOTE 4: Assured by design, not tested in production.

power okay (see Note 7)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
$V_{(POKLO)}$	Low threshold	Output falls % of V_O (power NOT okay)	85%			
$V_{(POKTH)}$	High threshold	Output reaches % of V_O, starts delay timer (power okay)			90%	
V_{OL}	V_O out of regulation	Fault condition, I_{OL} = 100 µA			0.4	V
I_{lkg}	Leakage current	V_I = 5 V			1	µA

NOTE 7: Power okay is a function of the output voltage being 5% lower than the specified range. The function is a detection of one of the following: over current, over temperature, or dropout.

switching characteristics (see Note 4),T_A = 25°C, V_I = 5 V, $V_{(EN)}$ = V_I, I_O = 100 μA, C_L = 1 μF(unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Power up overshoot	Maximum voltage overshoot allowed on output during powerup		1%		
$t_{(STEP)}$	Output transient time limit	Time for output to return within specified regulation range		5		μs
	Output transient voltage limit	Voltage that load step can affect the nominal output voltage		1%		
$I_{(SR)}$	Load step current slew rate	I_L = 0.1 mA to 150 mA		10		mA/μs
t_r	Power up rise time			50		μs
t_f	Power down fall time	Discharge resistance = 500 Ω, V_O < 1.08 V		60		μs
$t_{d(POK)}$	Power okay delay time	V_I > $V_{(POKTH)}$ until POK↑		2.5		ms

NOTE 4: Assured by design, not tested in production.

thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal impedance, junction-to-case			145		°C/W
$R_{\theta JA}$	Thermal impedance, junction-to-ambient			235		°C/W

PARAMETER MEASUREMENT INFORMATION

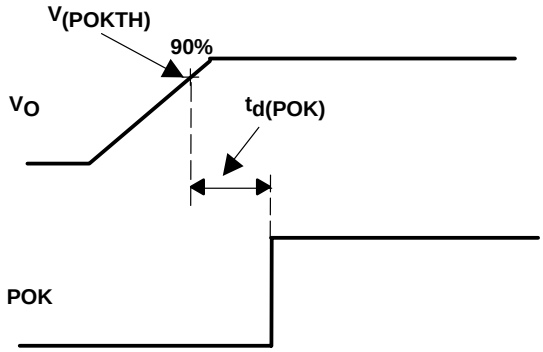


Figure 1. Power Okay Timing During Power Up

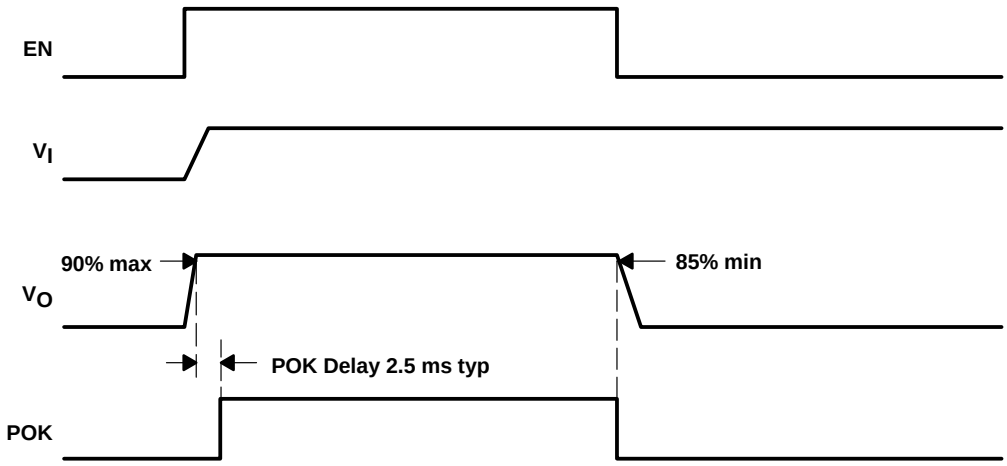


Figure 2. Power Okay Delay Timing and Output Voltage Supervisory

TYPICAL CHARACTERISTICS

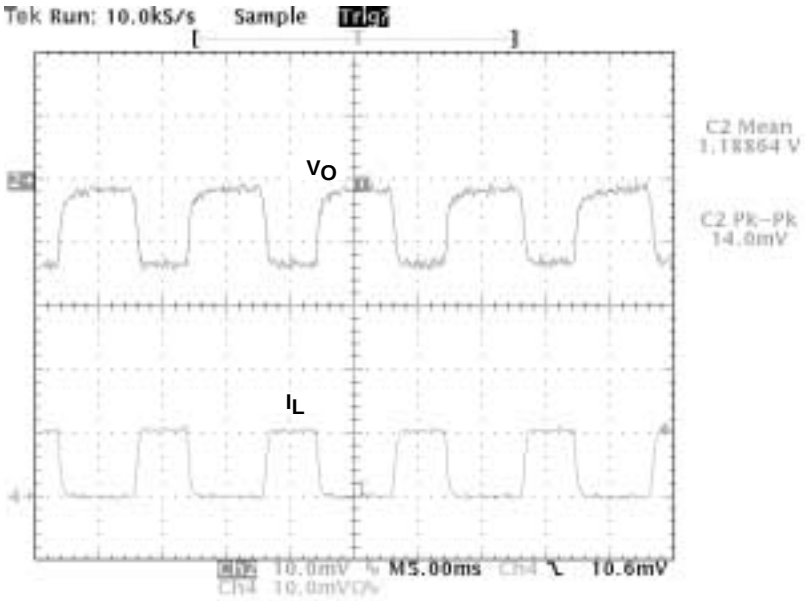


Figure 3. Load Regulation, 50-mA Dynamic Load Step (V_I = 3 V)

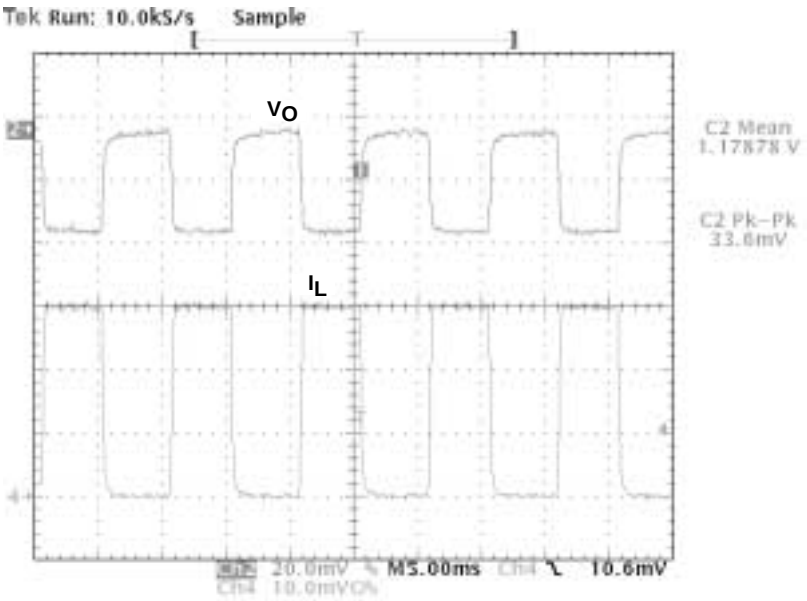


Figure 4. Load Regulation, 150-mA Dynamic Load Step (V_I = 3 V)

TYPICAL CHARACTERISTICS

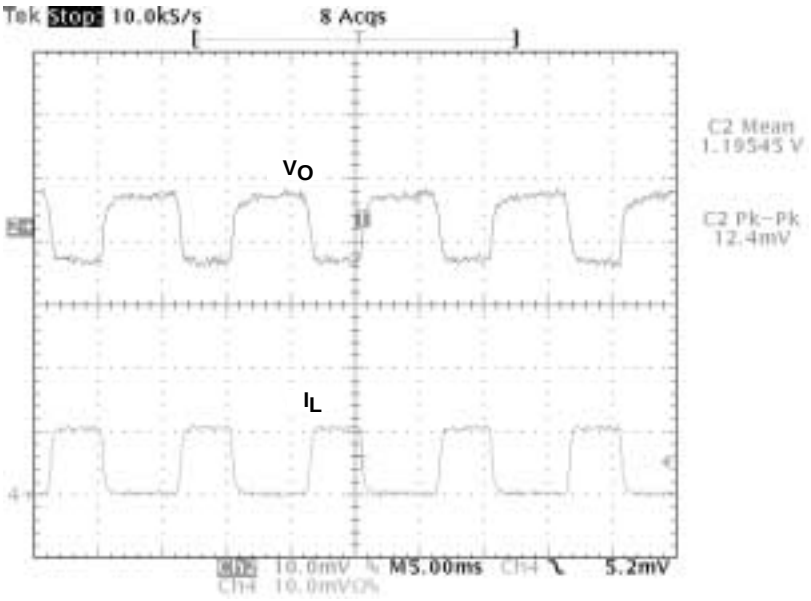


Figure 5. Load Regulation, 50-mA Dynamic Load Step (V_I = 5 V)

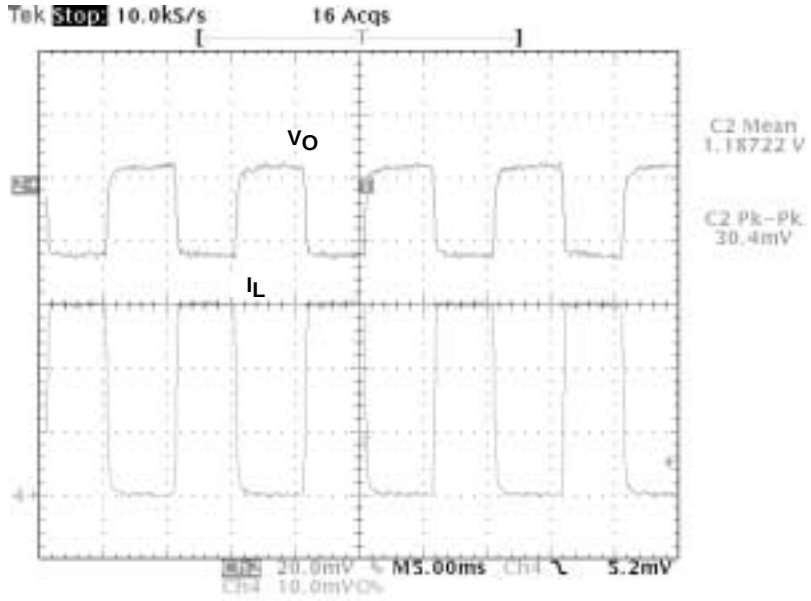


Figure 6. Load Regulation, 150-mA Dynamic Load Step (V_I = 5 V)

TYPICAL CHARACTERISTICS

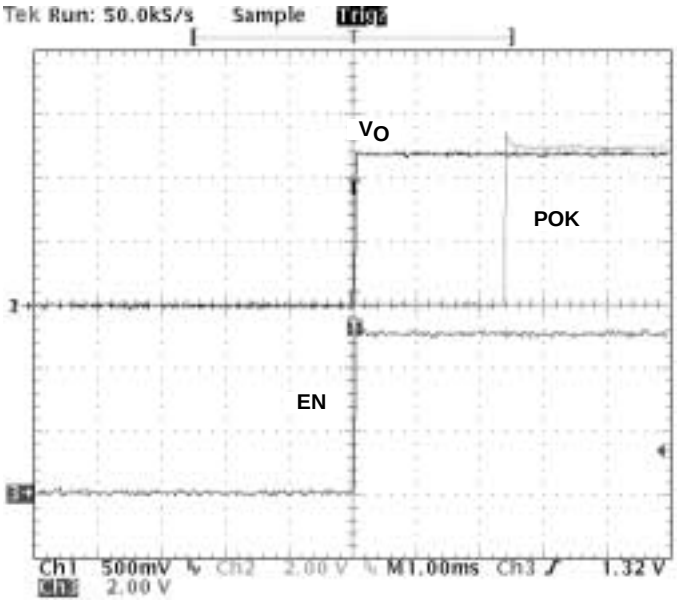


Figure 7. Power Okay Delay During Power Up Condition

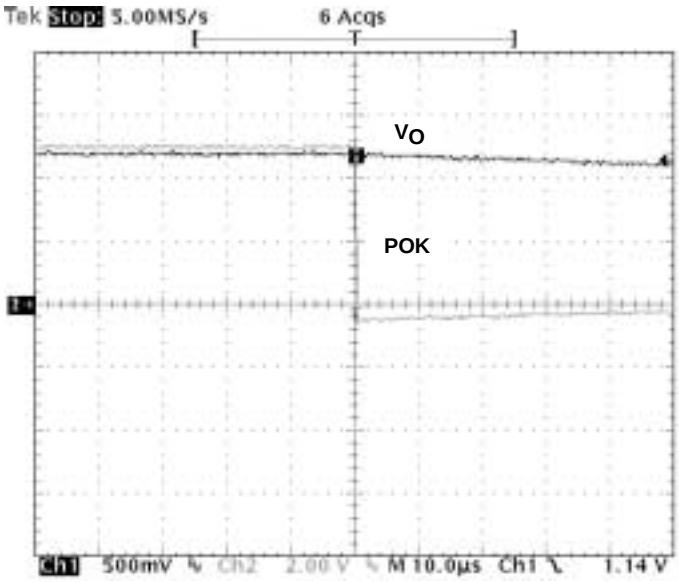


Figure 8. Power Okay Delay During Power Down Condition

THERMAL INFORMATION

The TPPM0125 is designed to provide a continuous load current of 150 mA when the maximum power dissipation of the package is not exceeded in the application. To determine the maximum power dissipation of the package, use the junction-to-ambient thermal resistance of the device. The basic equation is as follows:

Maximum power dissipation (W)

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / R_{\theta JA} \text{ (maximum power dissipation limit)}$$

Where:

$T_{J(MAX)}$ is the maximum junction temperature of the die (less than 150°C, minimum thermal shutdown)
T_A is the operating ambient temperature
$R_{\theta JA}$ is the thermal resistance and is layout dependent

The recommended minimum footprint offers a $R_{\theta JA}$ of 235°C/W.
To determine the actual power dissipation of the regulator, use the following equation:

$$P_D = (V_I - V_O) I_O + V_I I_{(GND)} \text{ (Watts)}$$

Power dissipation resulting from quiescent current is negligible. When the power dissipation is excessive, the thermal protection circuit is triggered.

APPLICATION INFORMATION

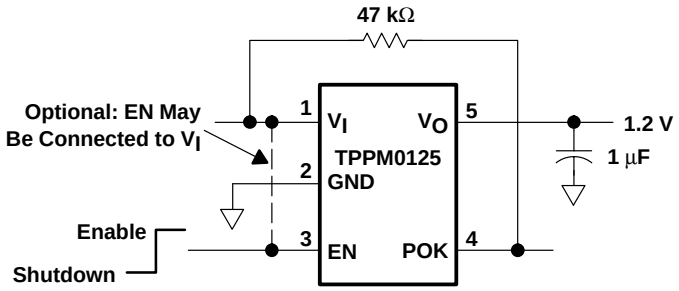


Figure 9. Typical Application Schematic

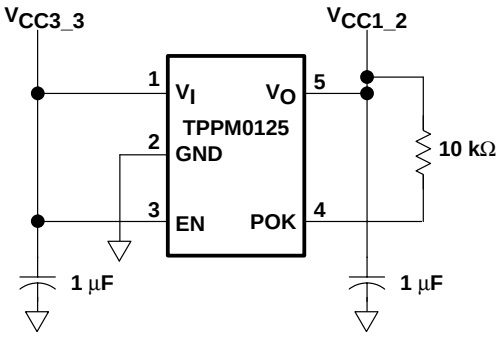
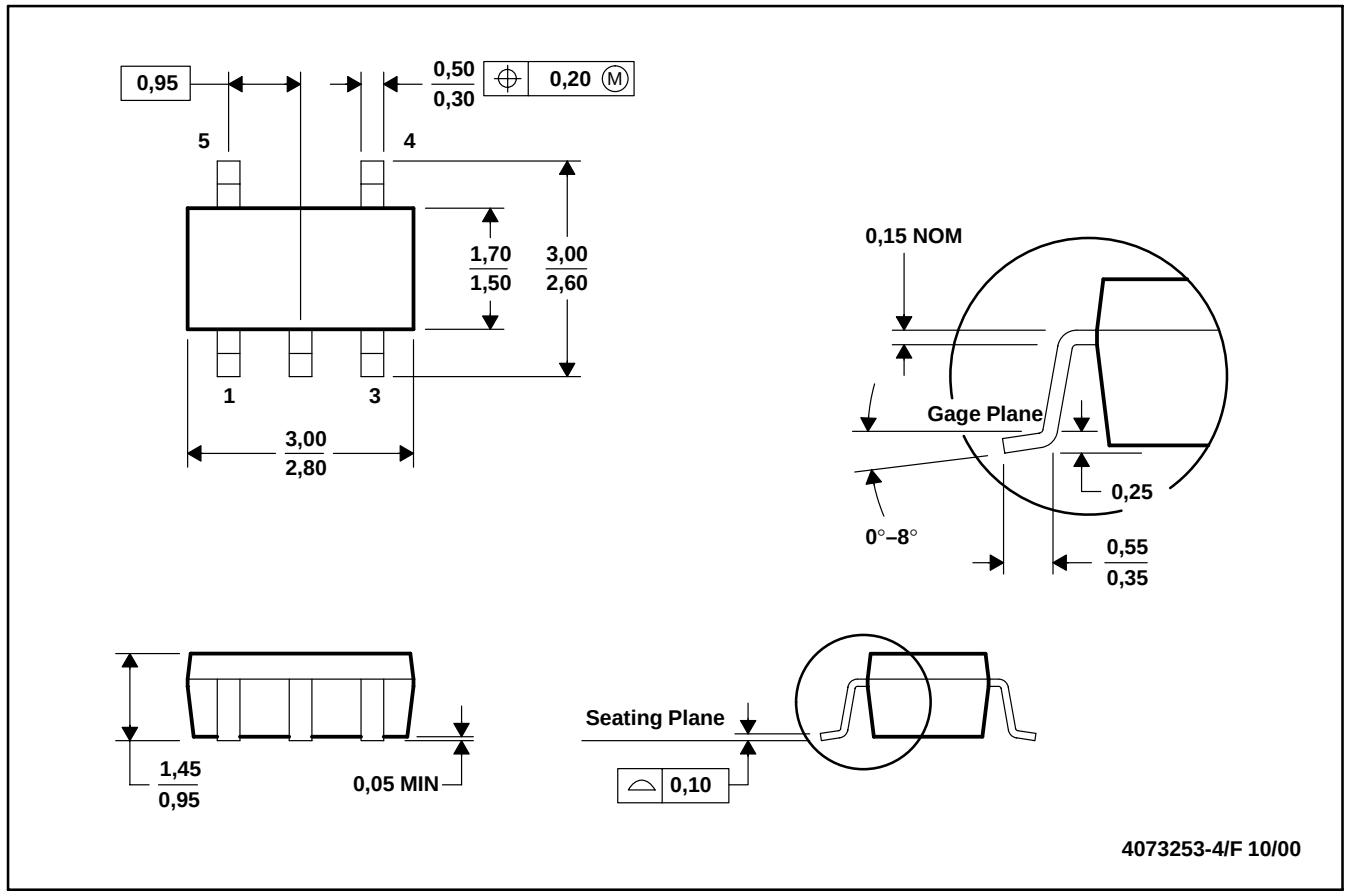


Figure 10. Typical Application For Processor VID Code Power Sequencing Schematic

MECHANICAL DATA

DBV (R-PDSO-G5) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-178

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