GSM 4 W power amplifiers CGY2010G; CGY2011G

FEATURES

- Power Amplifier (PA) overall efficiency 45%
- 35.5 dB gain
- 0 dBm input power
- Gain control range >55 dB
- Integrated power sensor driver
- Low output noise floor of PA < −129 dBm/Hz in GSM RX band
- Wide operating temperature range −20 to +85 °C
- LQFP 48 pin package
- Compatible with power ramping controller PCA5075
- Compatible with GSM RF transceiver SA1620.

APPLICATIONS

- 880 to 915 MHz hand-held transceivers for E-GSM applications
- 900 MHz TDMA systems.

GENERAL DESCRIPTION

The CGY2010G and CGY2011G are GSM class 4 GaAs Monolithic Microwave Integrated Circuits (MMICs) power amplifiers specifically designed to operate at 4.8 V battery supply. These ICs also include a power sensor driver so that no directional coupler is required in the power control loop.

Both ICs have the same performance but are issued from different wafer fabs.

The PAs require only a 30 dB harmonic low-pass filter to comply with the GSM transmit spurious specification. They can be switched off and their power controlled by monitoring the actual drain voltage applied to the amplifier stages.

QUICK REFERENCE DATA

SYMBOL	PARAMETER (1)	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	–	4.2	–	V
I_{DD}	positive peak supply current	–	1.8	–	A
$P_{out(max)}$	maximum output power	–	35.5	–	dBm
T_{amb}	operating ambient temperature	−20	–	+85	°C

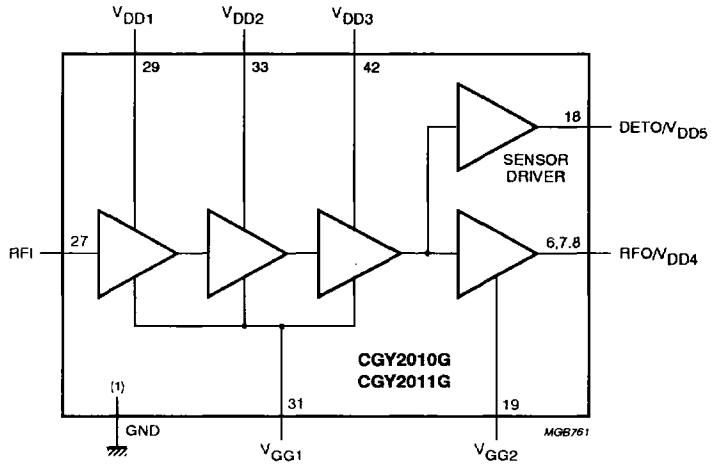
Note

1. For conditions, see Chapters "AC characteristics" and "DC characteristics".

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CGY2010G	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
CGY2011G			

BLOCK DIAGRAM



(1) Ground pins 1 to 5, 9 to 17, 20 to 26, 28, 30, 32, 34 to 41 and 43 to 48.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
GND	1 to 5	ground
RFO/V_{DD4}	6 to 8	power amplifier output and fourth stage supply voltage
GND	9 to 17	ground
DETO/V_{DD5}	18	power sensor output and supply voltage
V_{GG2}	19	fourth stage negative gate supply voltage
GND	20 to 26	ground
RFI	27	power amplifier input
GND	28	ground
V_{DD1}	29	first stage supply voltage
GND	30	ground
V_{GG1}	31	first three stages negative gate supply voltage
GND	32	ground
V_{DD2}	33	second stage supply voltage
GND	34 to 41	ground
V_{DD3}	42	third stage supply voltage
GND	43 to 48	ground

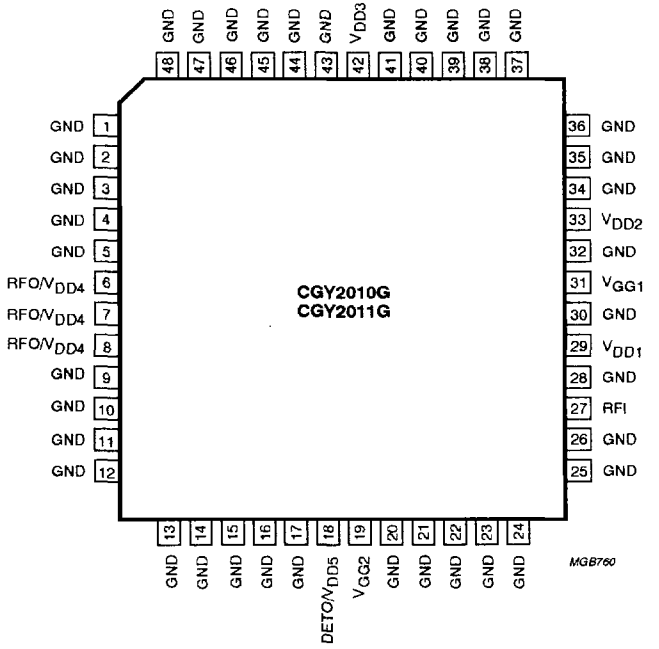


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Operating conditions

The CGY2010G and CGY2011G are designed to meet the European Telecommunications Standards Institute (ETSI) GSM documents, the *"ETS 300 577 specification"*, which are defined as follows:

- t_{on} = 542.8 µs
- T = 4.3 ms
- Duty cycle = 1/8

The devices are specifically designed for pulse operation allowing the use of a LQFP48 plastic package.

Power amplifier

The power amplifier consists of four cascaded gain stages with an open-drain configuration. Each drain has to be loaded externally by an adequate reactive circuit which also has to be a DC path to the supply.

The amplifier bias is set by means of a negative voltage applied at pins V_{GG1} and V_{GG2}. This negative voltage must be present before the supply voltage is applied to the drains to avoid current overstress for the amplifier.

Power sensor driver

The power sensor driver is a buffer amplifier that delivers a signal to the DETO output pin which is proportional to the amplifier power. This signal can be detected by external diodes for power control purpose. As the sensor signal is taken from the input of the last stage of the PA, it is isolated from disturbances at the output by the reverse isolation of the PA output stage.

Impedance mismatch at the PA output therefore, does not significantly influence the signal delivered by the power sensor as this normally occurs when power sense is made using a directional coupler. Consequently the cost and space of using a directional coupler are saved.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); general operating conditions applied.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	positive supply voltage	–	7	V
V_{GG}	negative supply voltage	–	−10	V
$T_{j(max)}$	maximum operating junction temperature	–	150	°C
T_{stg}	IC storage temperature	–	150	°C
P_{tot}	total power dissipation	–	1.5	W

THERMAL CHARACTERISTICS

General operating conditions applied.

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}c}$	thermal resistance from junction to case; note 1	32	K/W

Note

1. This thermal resistance is measured under GSM pulse conditions.

DC CHARACTERISTICS

V_{DD} = 4.5 V; T_{amb} = 25 °C; general operating conditions applied; peak current values during burst; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins RFO/V_{DD4}, V_{DD3}, V_{DD2}, V_{DD1} and DETO/V_{DD5}						
V_{DD}	positive supply voltage		0	4.2	5.5	V
I_{DD}	positive peak supply current		–	1.8	2.2	A
Pins V_{GG1} and V_{GG2}						
V_{GG1}	negative supply voltage	note 1	–	−2	–	V
V_{GG2}	negative supply voltage	note 1	–	−2	–	V
$I_{GG1} + I_{GG2}$	negative peak supply current		–	2.5	5	mA

Note

1. The negative bias V_{GG1} and V_{GG2} must be applied 10 μs before the power amplifier is switched on, and must remain applied until the power amplifier has been switched off.

AC CHARACTERISTICS

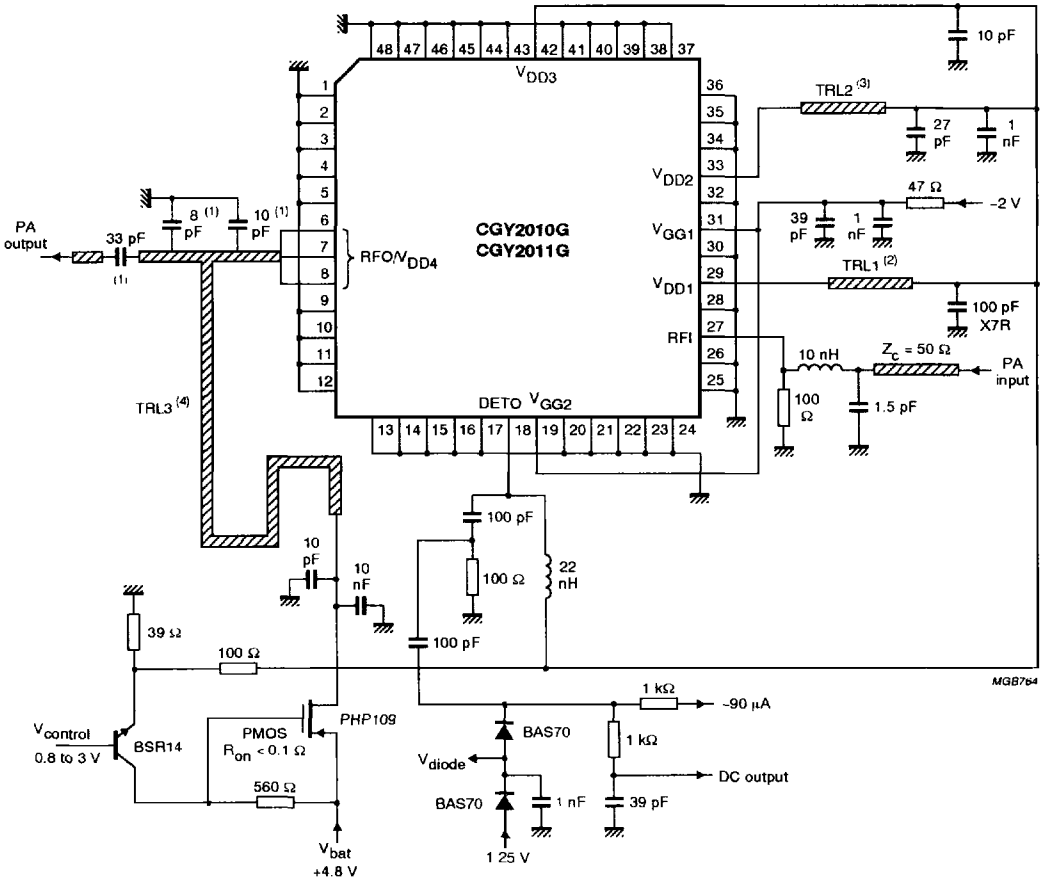
V_{DD} = 4.5 V; T_{amb} = 25 °C; general operating conditions applied; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power amplifier						
P_{in}	input power		−1.5	–	+1.5	dBm
S_{11}	input return loss	note 1; 50 Ω source	–	–	−6	dB
f_{RF}	RF frequency range		880	–	915	MHz
$P_{out(max)}$	maximum output power	T_{amb} = 25 °C; V_{DD} = 4.5 V	34.5	35.5	–	dBm
		T_{amb} = −20 to +85 °C; V_{DD} = 4.2 V	32.5	–	–	dBm
η	efficiency	V_{DD} = 4.2 V	–	45	–	%
$P_{out(min)}$	minimum output power	V_{DD} < 0.1 V	–	–	−20	dBm
N_{RX}	output noise in RX band	f_{RF} = 925 MHz at $P_{out(max)}$	–	–	−117	dBm/Hz
		f_{RF} = 935 MHz at $P_{out(max)}$	–	–	−129	dBm/Hz
		f_{RF} = 960 MHz at $P_{out(max)}$	–	–	−129	dBm/Hz
H2	2nd harmonic level		–	−33	−30	dBc
H3	3rd harmonic level		–	−40	−37	dBc
Stab	stability	note 2	–	–	−70	dBc
Power sensor driver						
$P_{out(DET)}$	sensor driver output power	R_L = 100 Ω; relative to PA output power into 50 Ω load	–	−23	–	dBc
$\Delta P_{out(DET)}$	driver output power variation	load VSWR < 6 : 1 at PA output	–	–	2	dB

Notes

1. Including the 100 Ω resistor connected in parallel at the power amplifier input on the evaluation board.
2. The device is adjusted to provide nominal value of load power into a 50 Ω load. The device is switched off and a 6 : 1 load replaces the 50 Ω load. The device is switched on and the phase of the 6 : 1 load is varied 360 electrical degrees during a 60 second period.

APPLICATION INFORMATION



(1) These capacitors are type: SMD0402; rest of the capacitors: SMD0603.
(2) TRL1: width: 0.3 mm; length: 16 mm.
(3) TRL2: width: 0.3 mm; length: 6.3 mm.
(4) TRL3: width: 0.3 mm; length: 20 mm.

Fig.3 Evaluation board schematic (FR4, 0.8 mm).