

Document Title

4M DDR SYNCHRONOUS SRAM

Revision History

<u>Rev.No.</u>	<u>History</u>	<u>DraftData</u>	<u>Remark</u>
Rev. 0.0	Initial document.	Aug. 1998	Advance
Rev.0.5	Correction on the miss print and the package size.	July. 1999	Preliminary
Rev.1.0	Added 4ns cycle time (500Mbps).	Nov. 1999	Final

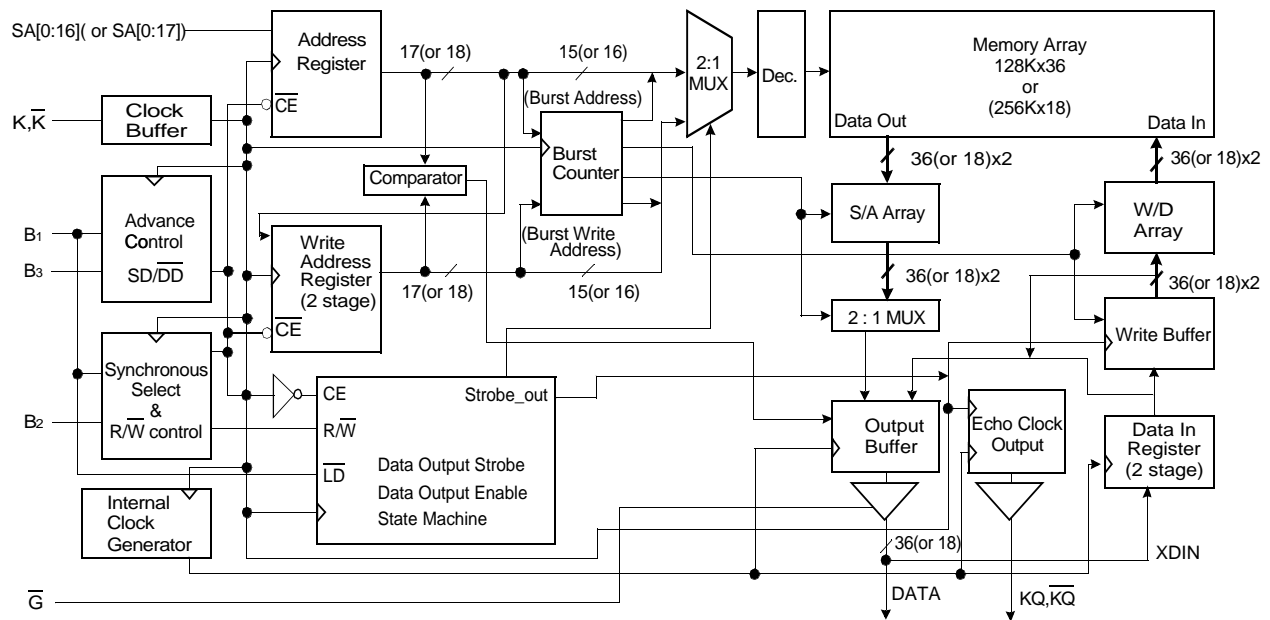
FEATURES

- 128Kx36 or 256Kx18 Organizations.
- 2.5V Core/1.5V Output Power Supply.
- HSTL Input and HSTL Outputs.
- Single Differential HSTL Clock.
- Synchronous Pipeline Mode of Operation with Self-Timed Late Write.
- Free Running Active High and Active Low Echo Clock Output Pin.
- Asynchronous Output Enable.
- Registered Addresses, Burst Control Inputs and Data Inputs.
- Registered Outputs.
- Single and Double Data Rate Burst Read and Write.
- 4 Count Burst Operation
- JTAG 1149.1 Compatible Test Access port.
- 153(9x17) Pin Ball Grid Array Package(14mm x 22mm).

- Programmable Impedance Output Drivers.

Organization	Part Number	Cycle Time	Access Time
128Kx36	K7D403671M-H25	4	2.4
	K7D403671M-H22	44	2.4
	K7D403671M-H20	5	2.7
	K7D403671M-H16	6	3.3
256Kx18	K7D401871M-H25	4	2.4
	K7D401871M-H22	44	2.4
	K7D401871M-H20	5	2.7
	K7D401871M-H16	6	3.3

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Description	Pin Name	Pin Description
K, K-bar	Differential Clocks	G-bar	Asynchronous Output Enable
SA	Synchronous Address Input	TCK	JTAG Test Clock
SA0, SA1	Synchronous Burst Address Input	TMS	JTAG Test Mode Select
DQ	Synchronous Data I/O	TDI	JTAG Test Data Input
VDD	Core Power Supply	TDO	JTAG Test Data Output
VDDQ	Output Power Supply	ZQ	Output Driver Impedance Control Input
VREF	HSTL Input Reference Voltage	LBO-bar	Linear Burst Order
B1	Load External Address	MODE	No Connect (Reserved)
B2	Burst R/W Enable	Vss	GND
B3	Single/Double Data Selection	NC	No Connection
KQ, KQ-bar	Differential Output Echo Clocks		

PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7D403671(128Kx36)

	1	2	3	4	5	6	7	8	9
A	Vss	VDDQ	SA	SA	ZQ	SA	SA	VDDQ	Vss
B	DQ	DQ	SA	Vss	B1	Vss	SA	DQ	DQ
C	Vss	VDDQ	SA	SA	\overline{G}	SA	SA	VDDQ	Vss
D	DQ	DQ	N.C	Vss	VDD	Vss	NC	DQ	DQ
E	Vss	VDDQ	Vss	VDD	VREF	VDD	Vss	VDDQ	Vss
F	DQ	KQ	DQ	VDD	VDD	VDD	DQ	KQ	DQ
G	Vss	VDDQ	Vss	Vss	K	Vss	Vss	VDDQ	Vss
H	DQ	DQ	DQ	VDD	\overline{K}	VDD	DQ	DQ	DQ
J	Vss	VDDQ	Vss	VDD	VDD	VDD	Vss	VDDQ	Vss
K	DQ	DQ	DQ	Vss	B2	Vss	DQ	DQ	DQ
L	Vss	VDDQ	Vss	\overline{LBO}	B3	MODE	Vss	VDDQ	Vss
M	DQ	\overline{KQ}	DQ	VDD	VDD	VDD	DQ	\overline{KQ}	DQ
N	Vss	VDDQ	Vss	VDD	VREF	VDD	Vss	VDDQ	Vss
P	DQ	DQ	NC	Vss	VDD	Vss	SA	DQ	DQ
R	Vss	VDDQ	VDD	SA	SA1	SA	VDD	VDDQ	Vss
T	DQ	DQ	SA	Vss	SA0	Vss	SA	DQ	DQ
U	Vss	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ	Vss

K7D401871(256Kx18)

	1	2	3	4	5	6	7	8	9
A	Vss	VDDQ	SA	SA	ZQ	SA	SA	VDDQ	Vss
B	NC	DQ	SA	Vss	B1	Vss	SA	NC	DQ
C	Vss	VDDQ	SA	SA	\overline{G}	SA	SA	VDDQ	Vss
D	DQ	NC	NC	Vss	VDD	Vss	NC	DQ	NC
E	Vss	VDDQ	Vss	VDD	VREF	VDD	Vss	VDDQ	Vss
F	NC	KQ	NC	VDD	VDD	VDD	DQ	NC	DQ
G	Vss	VDDQ	Vss	Vss	K	Vss	Vss	VDDQ	Vss
H	DQ	NC	DQ	VDD	\overline{K}	VDD	NC	DQ	NC
J	Vss	VDDQ	Vss	VDD	VDD	VDD	Vss	VDDQ	Vss
K	NC	DQ	NC	Vss	B2	Vss	DQ	NC	DQ
L	Vss	VDDQ	Vss	\overline{LBO}	B3	MODE	Vss	VDDQ	Vss
M	DQ	NC	DQ	VDD	VDD	VDD	NC	\overline{KQ}	NC
N	Vss	VDDQ	Vss	VDD	VREF	VDD	Vss	VDDQ	Vss
P	NC	DQ	SA	Vss	VDD	Vss	SA	NC	DQ
R	Vss	VDDQ	VDD	SA	SA1	SA	VDD	VDDQ	Vss
T	DQ	NC	SA	Vss	SA0	Vss	SA	DQ	NC
U	Vss	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ	Vss

FUNCTION DESCRIPTION

The K7D403671M and K7D401871M are 4,718,592 bit Synchronous Pipeline Burst Mode SRAM devices. They are organized as 131,072 words by 36 bits for K7D403671M and 262,144 words by 18 bits for K7D401871M, fabricated using Samsung's advanced CMOS technology.

Single differential HSTL level K clocks are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of K clock, all addresses and burst control inputs are registered internally. And data inputs are registered at rising edges of K clock for a single data controlled mode, or at rising and falling edges of K clock for a dual data controlled mode, in the following cycle after write addresses are asserted.

An internal write data buffer allows write data to be stored before loaded into memory core in the next write cycles. Data outputs are updated from output registers on the rising edges of K clock for a single data controlled mode, or on the rising and falling edges of the K clock for a dual data controlled mode. Read data is referenced to Echo clock outputs. The chip is operated with a single +2.5V power supply and is compatible with HSTL input and HSTL output. The package is 9x17(153) Ball Grid Array balls on a 1.27mm pitch.

Read Operation(Single and Double)

During single read operation, the address is registered during the first clock edge, the internal array is read between this first edge and second edge, it is read again in the following cycle from the address increased by burst counter, and data is captured in the output register driven to the CPU during the second clock high edge and third clock high edge. During double read operation, the address is registered during the first clock edge, the internal array is read twice as much as wider than external bits, transferred to output buffer sequentially by burst order and the following cycle the same operation occur from address increased by burst counter, and data is captured in the output register driven to the CPU at active high clock edge and active low clock edge.

During consecutive read cycles where the address is the same, the data output must be held constant without any glitches. This characteristic is because the SRAM will be read by devices that will operate slower than the SRAM frequency and will require multiple SRAM cycles to perform a single read operation.

Write(Store) Operation

All addresses and R/W are sampled with B1 and B2 on the clock rising edge. B1 and B2 are low on the rising clock. Write address is sampled on the rising clock, one cycle after write address and Din have been sampled by the SRAM during 2 consecutive cycles at each active high and low clock edge and stored to write buffer for next real writing array. Actual write is done by using write data buffer on the SRAM that capture the write addresses on one address write cycles, and write the array on the next address write cycles. The "next address write cycles" can actually be many cycles away, broken by a series of read cycles. The SRAM is able to write 72 bits per cycle with 2-prefetched write buffer. This alleviates timing penalty of read after write cycle.

Echo clock operation

To assure the output tracibility, the SRAM provides the output Echo clock, pair of complement clock, which is synchronized with internal data output.

During read and write cycle, the Echo clock is triggered by internal output clock signal, and transferred to external through same structures as output driver in read cycle.

Bypass Read Operation

Since write data is not fully written into the array on first write cycle, there is a need to sense the address in case a future read is to be done from the location that has not been written yet. For this case, the address comparator check to see if the new read address is the same as the contents of the stored write address latch. If the contents match, the read data must be supplied from the stored write data latch with standard read timing. If there is no match, the read data comes from the SRAM array.

PROGRAMMABLE IMPEDANCE OUTPUT BUFFER OPERATION

The designer can program the SRAM's output buffer impedance by terminating the ZQ pin to Vss through a precision resistor(RQ). The value of RQ is five times the output impedance desired. For example, 250Ω resistor will give an output impedance of 50Ω. The allowable range of RQ is between 175Ω and 350Ω. Impedance updates occur early in cycles that do not activate the outputs, such as deselect cycles. They may also occur in cycles initiated with \bar{G} high. In all cases impedance updates are transparent to the user and do not produce access time "push-outs" or other anomalous behavior in the SRAM. Periodic readjustment is necessary as the impedance is greatly affected by drifts in supply voltage and temperature. Impedance updates occur no more often than every 32 clock cycles. Clock cycles are counted whether the SRAM is selected or not and proceed regardless of the type of cycle being executed. Therefore, the user can be assured that after 33 continuous read cycles have occurred, an impedance update will occur the next time \bar{G} are high at a rising edge of the K clock. There are no power up requirements for the SRAM. However, to guarantee optimum output driver impedance after power up, the SRAM needs 1024 non-read cycles.

TRUTH TABLE

K	\overline{G}	B1	B2	B3	DQ	Operation
L	H	X	X	X	Hi-Z	Clock Stop
↑	H	H	L	X	Hi-Z	No Operation, Pipeline High-Z
↑	L	L	H	H	DOUT	Load Address, Single Read
↑	L	L	H	L	DOUT	Load Address, Double Read
↑	H	L	L	H	DIN	Load Address, Single Write
↑	H	L	L	L	DIN	Load Address, Double Write
↑	L	H	H	X	B	Increment Address, Continue

NOTE : B(Both) is DIN in write cycle and DOUT in read cycle. Byte write function is not supported. X means "Don't Care".

BURST SEQUENCE TABLE

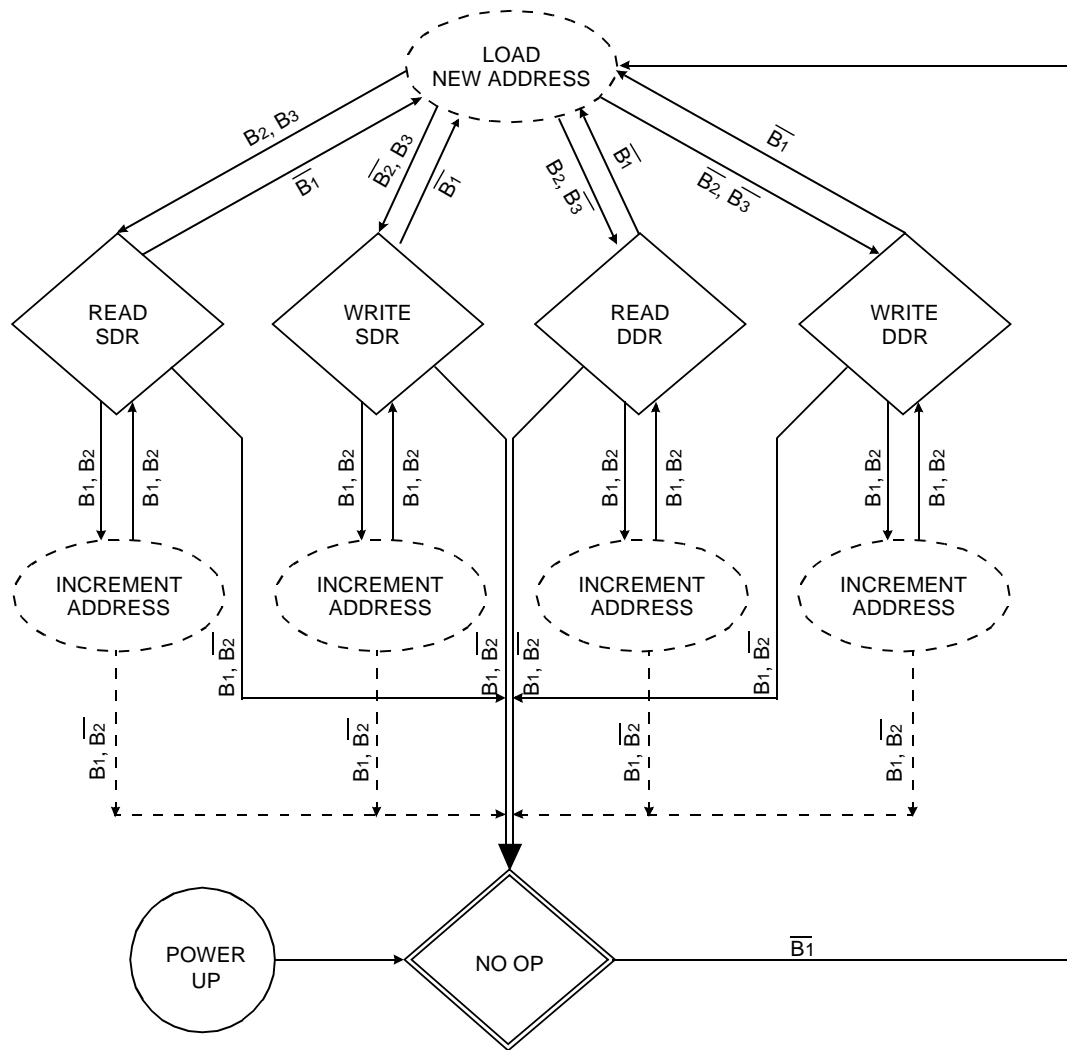
4 Burst Operation for Interleaved Burst ($\overline{LBO} = \text{High}$)

Interleaved Burst	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
↓	0	1	0	0	1	1	1	0
↓	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

4 Burst Operation for Linear Burst ($\overline{LBO} = \text{Low}$)

Interleaved Burst	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
↓	0	1	1	0	1	1	0	0
↓	1	0	1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	1	0

BUS CYCLE STATE DIAGRAM



NOTE :

- State transitions ; $\overline{B1}$ =(Load Address), $B1$ =(Increment Address, Continue)
 $B2$ =(Read), $\overline{B2}$ =(Write)
 $B3$ =(Single Data Rate), $\overline{B3}$ =(Double Data Rate)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Core Supply Voltage Relative to Vss	VDD	-0.5 to 3.5	V
Output Supply Voltage Relative to Vss	VDDQ	-0.5 to VDD+0.5	V
Voltage on any pin Relative to Vss	VIN	-0.5 to VDD+0.5	V
Maximum Power Dissipation	Pd	-	W
Output Short-Circuit Current(per I/O)	IOUT	25	mA
Storage Temperature	TSTR	-55 to 125	°C

NOTE : Power Dissipation Capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data. Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Core Power Supply Voltage	VDD	2.4	2.5	2.6	V	
Output Power Supply Voltage	VDDQ	1.4	1.5	1.6	V	
Input High Level Voltage	VIH	VREF+0.1	-	VDD + 0.3	V	1, 2
Input Low Level Voltage	VIL	-0.3	-	VREF-0.1	V	1, 3
Input Reference Voltage	VREF	0.6	0.75	1.0	V	
Operating Junction Temperature	TJ	20	-	110	°C	4

NOTE : 1. These are DC test criteria. DC design criteria is VREF±50mV. The AC VIH/VIL levels are defined separately for measuring timing parameters.

2. VIH (Max)DC=VDD+0.3, VIH (Max)AC=VDD+1.5V(pulse width ≤ 5ns).

3. VIL (Min)DC=-0.3V, VIL (Min)AC=-1.5V(pulse width ≤ 5ns).

4. Junction temperature is a function of on-chip power dissipation, package thermal impedance, mounting site temperature and mounting site thermal impedance. TJ=TA + Pd x THETA_JA

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Note
Average Power Supply Operating Current(x36) (Cycle time = tKHKH min)	IDD4	-	700	mA	1,2
	IDD44		650		
	IDD5		600		
	IDD6		550		
Average Power Supply Operating Current(x18) (Cycle time = tKHKH min)	IDD4	-	650	mA	1,2
	IDD44		600		
	IDD5		550		
	IDD6		500		
Stop Clock Standby Current (VIN=VDD-0.2V or 0.2V fixed, Clock=Low)	ISB1	-	50	mA	1
Input Leakage Current (VIN=Vss or VDD)	ILI	-1	1	µA	
Output Leakage Current (VOUT=Vss or VDDQ except KQx,KQx)	ILO	-1	1	µA	
Output High Voltage(Programmable Impedance Mode)	VOH1	VDDQ/2	VDDQ	V	3
Output Low Voltage(Programmable Impedance Mode)	VOL1	Vss	VDDQ/2	V	4
Output High Voltage(IoH=-0.1mA)	VOH3	VDDQ-0.2	VDDQ	V	5
Output Low Voltage(IoL=0.1mA)	VOL3	Vss	0.2	V	5

NOTE : 1. Minimum cycle. IOUT=0mA.

2. 50% read cycles.

3. |IoH|=(VDDQ/2)/(RQ/5)±10% @ VOH=VDDQ/2 for 175Ω ≤ RQ ≤ 350Ω.

4. |IoL|=(VDDQ/2)/(RQ/5)±10% @ VOL=VDDQ/2 for 175Ω ≤ RQ ≤ 350Ω.

5. Minimum Impedance Mode when ZQ pin is connected to VDD.

PIN CAPACITANCE

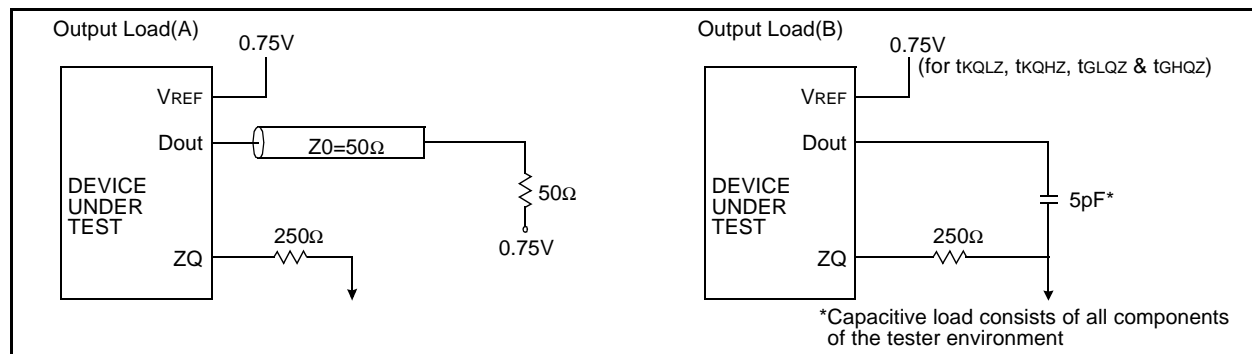
Parameter	Symbol	Typ.	Max	Unit
Input Pin Capacitance	C _{IN}	-	6	pF
I/O Pin Capacitance	C _{I/O}	-	7	pF
Clock Pin Capacitance	C _{CLK}	-	7	pF

*NOTE : Periodically Sampled and not 100% tested. (dV=0V, f=1MHz)

AC TEST CONDITIONS(T_J=20 to 110°C, V_{DD}=2.4 -2.6V, V_{DDQ}=1.4 - 1.6V)

Parameter	Symbol	Value	Unit	Note
Input High/Low Level	V _{IH} /V _{IL}	1.25/0.25	V	-
Input Reference Level	V _{REF}	0.75	V	-
Input Rise/Fall Time	T _R /T _F	1.0/1.0	ns	-
Output Timing Reference Level		0.75	V	-
Clock Input Timing Reference Level		Cross Point	V	-
Output Load		See Below		-

AC TEST OUTPUT LOAD

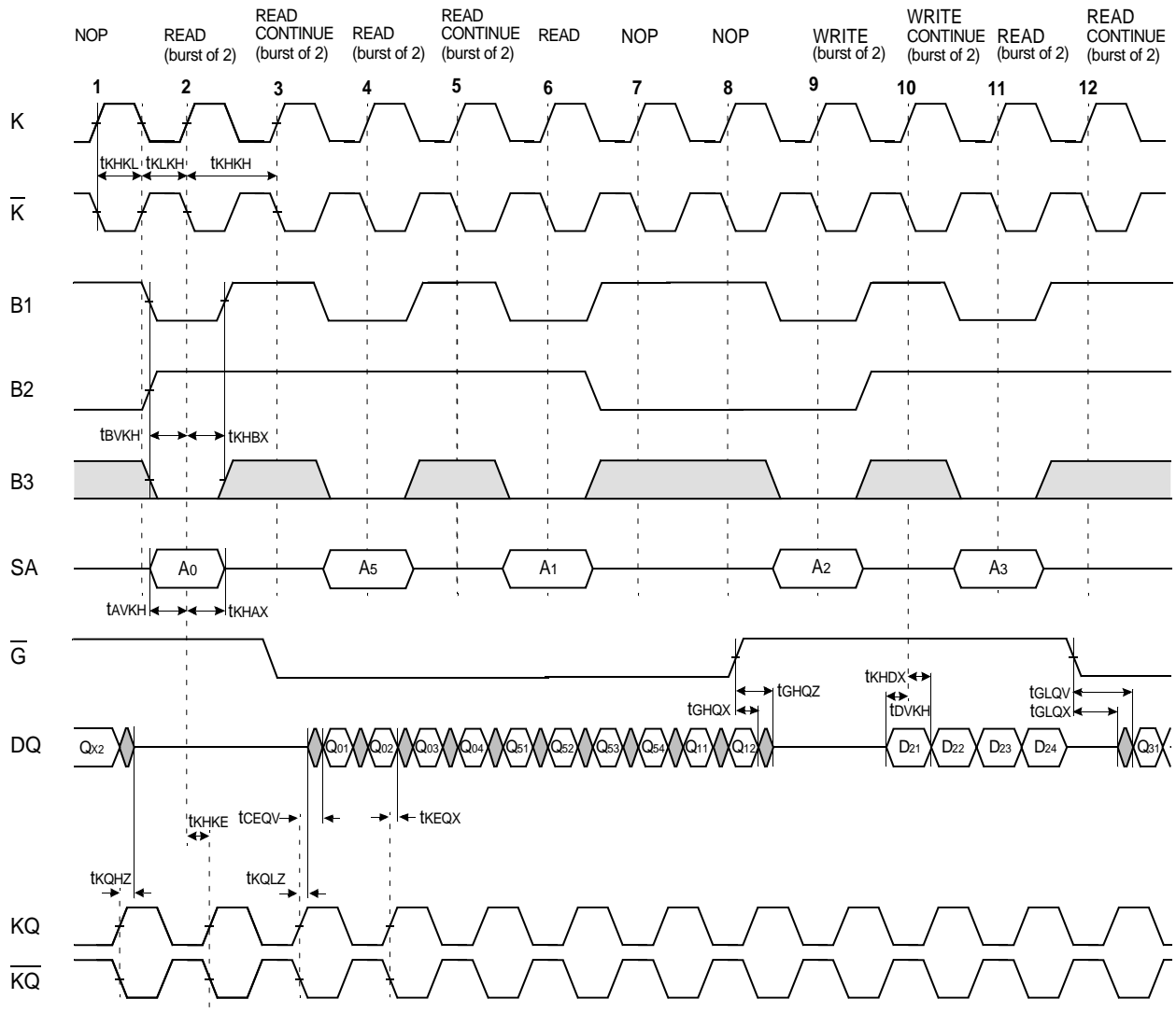


AC CHARACTERISTICS

Parameter	Symbol	-25		-22		-20		-16		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock Cycle Time	t _{KHKH}	4.0	-	4.4	-	5.0	-	6.0	-	ns	
Clock High Pulse Width	t _{KHKL}	1.6	-	1.8	-	2.0	-	2.4	-	ns	
Clock Low Pulse Width	t _{KLKH}	1.6	-	1.8	-	2.0	-	2.4	-	ns	
Clock to Echo Clock(KQ, \overline{KQ})	t _{KHKE}	-	2.2	-	2.2	-	2.5	-	3.0	ns	1
Echo Clock to Output Valid	t _{KEQV}	-	0.2	-	0.2	-	0.2	-	0.3	ns	1,2
Echo Clock to Output Hold	t _{KEQX}	-0.5	-	-0.5	-	-0.5	-	-0.6	-	ns	1
Echo Clock to Output Low-Z	t _{KQLZ}	-0.5	-	-0.5	-	-0.5	-	-0.6	-	ns	1
Echo Clock to Output High-Z	t _{KQHZ}	-	0.2	-	0.2	-	0.2	-	0.2	-	1
\overline{G} Low to Output Low-Z	t _{GLQX}	0.5	-	0.5	-	0.5	-	0.5	-	ns	1
\overline{G} High to Output High-Z	t _{GHQZ}	-	2.2	-	2.2	-	2.7	-	3.3	ns	1
\overline{G} Low to Output Valid	t _{GLQV}	-	2.2	-	2.2	-	2.7	-	3.3	ns	1
\overline{G} High to Output Hold	t _{GHQX}	0.5	-	0.5	-	0.5	-	0.5	-	ns	
Address Setup Time	t _{AVKH}	0.5	-	0.5	-	0.5	-	0.7	-	ns	
Address Hold Time	t _{KHAX}	0.5	-	0.5	-	0.5	-	0.7	-	ns	
Burst Control Setup Time	t _{BVKH}	0.5	-	0.5	-	0.5	-	0.7	-	ns	
Burst Control Hold Time	t _{KHBX}	0.5	-	0.5	-	0.5	-	0.7	-	ns	
Data Setup Time	t _{DVKH}	0.5	-	0.5	-	0.5	-	0.7	-	ns	
Data Hold Time	t _{KHDX}	0.5	-	0.5	-	0.5	-	0.7	-	ns	

NOTE : 1. See AC Test Output Load figure
 2. Design target is 0ns

TIMING WAVEFORMS FOR DOUBLE DATA RATE CYCLES
(Burst Length=4)

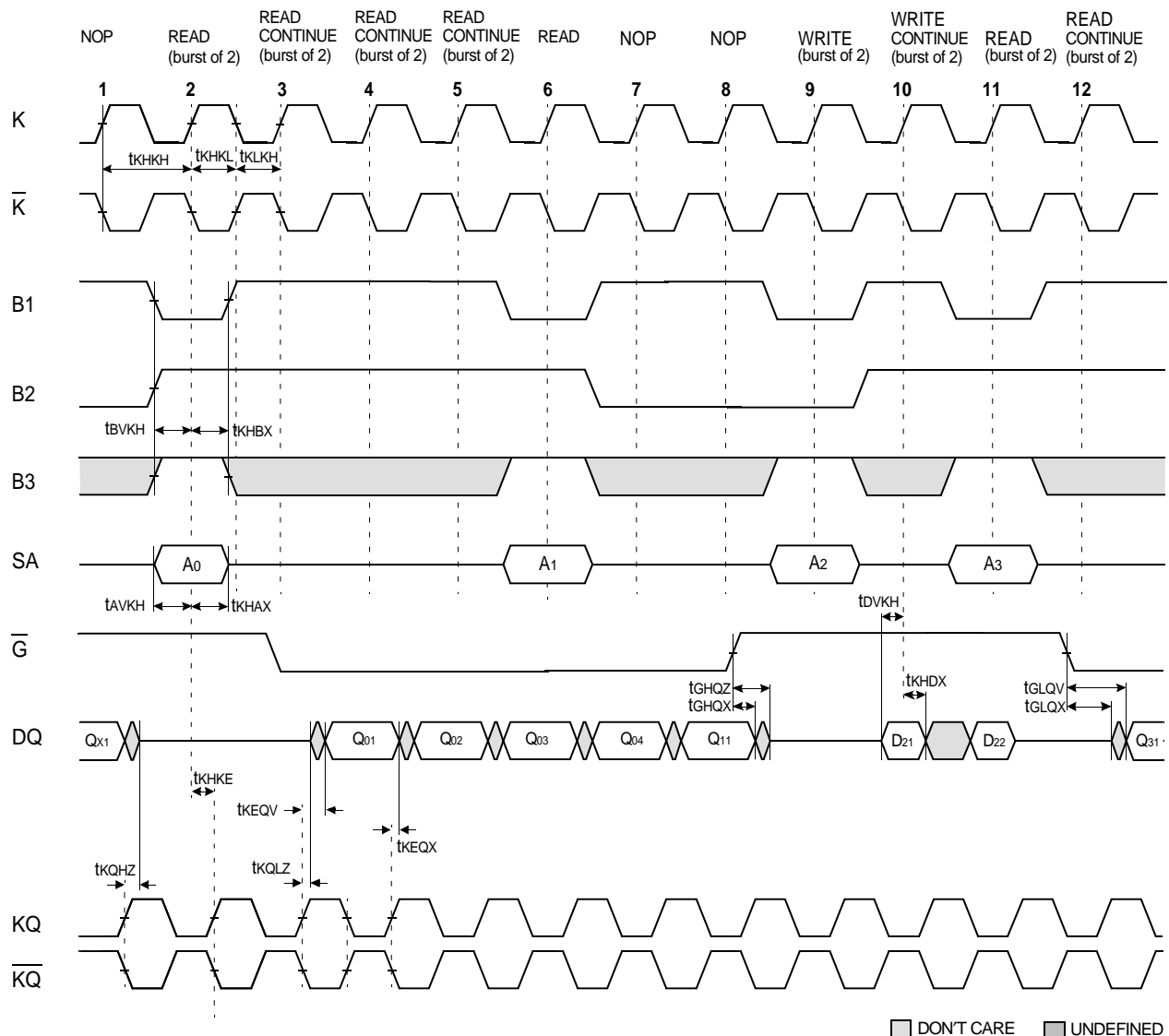


□ DON'T CARE ■ UNDEFINED

NOTE

1. Q₀₁ refers to output from address A₀. Q₀₂ refers to output from the next internal burst address following A₀, etc.
2. Outputs are disabled(High-Z) one clock cycle after NOP detected.
3. Doing more than one Read Continue or Write Continue will cause the address to wrap around.
4. The second NOP cycle is not necessary for correct device operation.
However, at high clock frequencies it may be required to prevent bus contention.

**TIMING WAVEFORMS FOR SINGLE DATA RATE CYCLES
(Burst Length=4)**



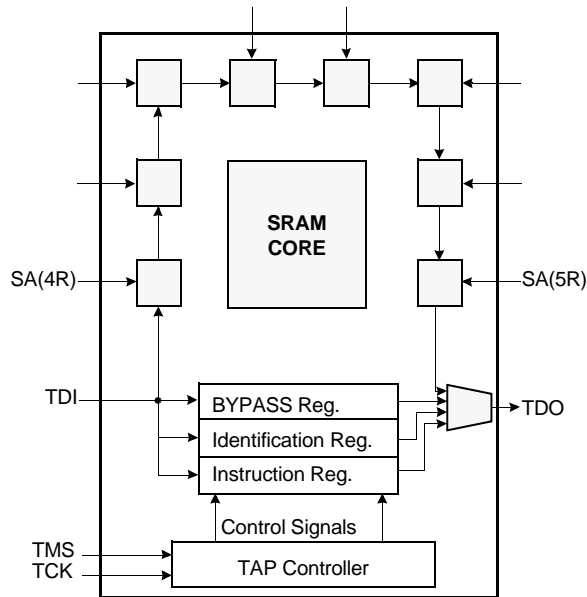
NOTE :

1. Q₀₁ refers to output from address A₀. Q₀₂ refers to output from the next internal burst address following A₀, etc.
2. Outputs are disabled(High-Z) one clock cycle after NOP detected
3. This devices supports cycle lengths of 1, 2, 4. Continue(B1=HIGH, B2=HIGH, B3=X) up to three times following a B1 operation.
4. This device will have an address to wrap around if further Continues are applied.
5. The second NOP cycle is not necessary for correct device operation.
however, at high clock frequencies it may be required to prevent bus contention.

IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port (TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to VDD through a resistor. TDO should be left unconnected.

JTAG Block Diagram



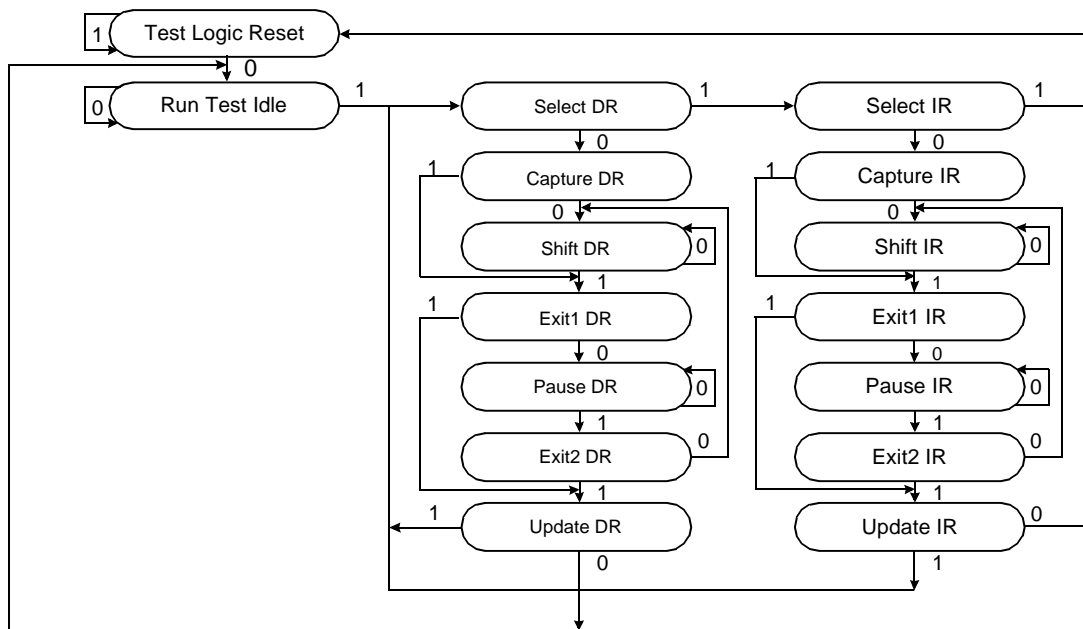
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Note
0	0	0	SAMPLE-Z	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	BYPASS	Bypass Register	3
1	1	0	BYPASS	Bypass Register	3
1	1	1	BYPASS	Bypass Register	3

NOTE :

1. Places DQs, KQx, \overline{KQx} in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction does not place DQs, KQx, \overline{KQx} in Hi-Z.

TAP Controller State Diagram



SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
128Kx36	3 bits	1 bits	32 bits	68 bits
256Kx18	3 bits	1 bits	32 bits	49 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit (0)
128Kx36	0000	00101 00100	XXXXXX	00001001110	1
256Kx18	0000	00110 00011	XXXXXX	00001001110	1

BOUNDARY SCAN EXIT ORDER(x36)

36	4A	SA		SA	6A	35
37	4C	SA		SA	6C	34
38	3A	SA		SA	7A	33
39	3B	SA		SA	7B	32
40	3C	SA		SA	7C	31
41	3D	NC ¹		NC ¹	7D	30
42	2B	DQ		DQ	8B	29
43	1B	DQ		DQ	9B	28
44	2D	DQ		DQ	8D	27
45	3F	DQ		DQ	7F	26
46	1D	DQ		DQ	9D	25
47	2F	KQ		KQ	8F	24
48	1F	DQ		DQ	9F	23
49	3H	DQ		DQ	7H	22
50	2H	DQ		DQ	8H	21
51	1H	DQ		DQ	9H	20
52	5A	ZQ		\overline{G}	5C	19
53	5B	B1		K	5G	18
54	5K	B2		\overline{K}	5H	17
55	5L	B3		MODE ²	6L	16
56	4L	\overline{LBO}		DQ	9K	15
57	1K	DQ		DQ	8K	14
58	2K	DQ		DQ	7K	13
59	3K	DQ		DQ	9M	12
60	1M	DQ		\overline{KQ}	8M	11
61	2M	\overline{KQ}		DQ	9P	10
62	1P	DQ		DQ	7M	9
63	3M	DQ		DQ	8P	8
64	2P	DQ		DQ	9T	7
65	1T	DQ		DQ	8T	6
66	2T	DQ		SA	7P	5
67	3T	SA		SA	7T	4
68	4R	SA		SA	6R	3
				SA ₀	5T	2
				SA ₁	5R	1

BOUNDARY SCAN EXIT ORDER(x18)

26	4A	SA		SA	6A	25
27	4C	SA		SA	6C	24
28	3A	SA		SA	7A	23
29	3B	SA		SA	7B	22
30	3C	SA		SA	7C	21
31	3D	NC ¹		NC ¹	7D	20
32	2B	DQ				
				DQ	9B	19
				DQ	8D	18
				DQ	7F	17
33	1D	DQ				
34	2F	KQ				
				DQ	9F	16
35	3H	DQ				
				DQ	8H	15
36	1H	DQ				
37	5A	ZQ		\overline{G}	5C	14
38	5B	B1		K	5G	13
39	5K	B2		\overline{K}	5H	12
40	5L	B3		MODE ²	6L	11
41	4L	\overline{LBO}		DQ	9K	10
42	2K	DQ		DQ	7K	9
43	1M	DQ		\overline{KQ}	8M	8
				DQ	9P	7
44	3M	DQ				
45	2P	DQ				
46	1T	DQ		DQ	8T	6
47	3P	SA		SA	7P	5
48	3T	SA		SA	7T	4
49	4R	SA		SA	6R	3
				SA ₀	5T	2
				SA ₁	5R	1

NOTE :

1. Pins 7D/3D are no connection pins to internal chip and place holders for 8M/16M parts. The scanned data are fixed to "1" for this 4M part.
2. Mode pin 6L is no connection pin to internal chip. The scanned data is fixed to "1".

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	VDD	2.4	2.5	2.6	V	
Input High Level	V _{IH}	1.7	-	V _{DD} +0.3	V	
Input Low Level	V _{IL}	-0.3	-	0.7	V	
Output High Voltage(I _{OH} =-2mA)	V _{OH}	2.0	-	V _{DD}	V	
Output Low Voltage(I _{OL} =2mA)	V _{OL}	V _{SS}	-	0.4	V	

NOTE : 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC TEST CONDITIONS

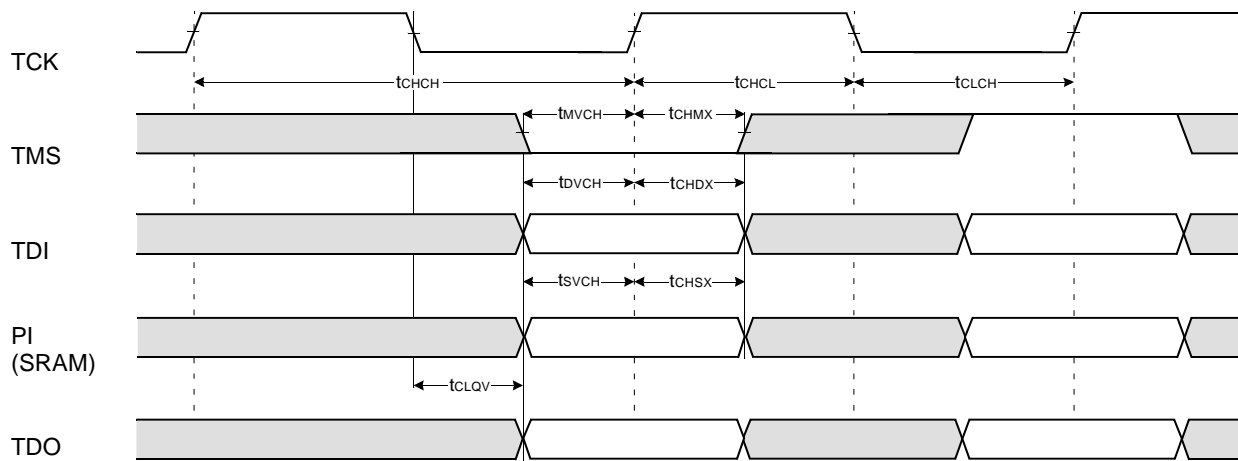
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V _{IH} /V _{IL}	2.5/0.0	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		1.25	V	1

NOTE : 1. See SRAM AC test output load on page 7.

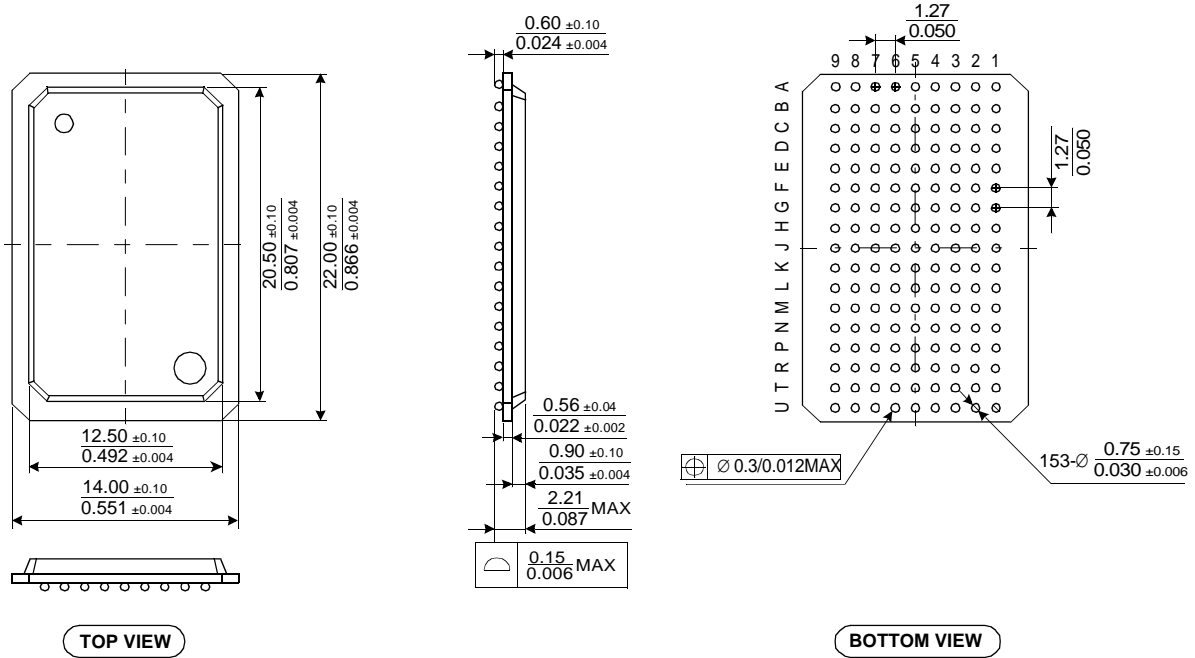
JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t _{CHCH}	50	-	ns	
TCK High Pulse Width	t _{CHCL}	20	-	ns	
TCK Low Pulse Width	t _{CLCH}	20	-	ns	
TMS Input Setup Time	t _{MVCH}	5	-	ns	
TMS Input Hold Time	t _{CHMX}	5	-	ns	
TDI Input Setup Time	t _{DVCH}	5	-	ns	
TDI Input Hold Time	t _{CHDX}	5	-	ns	
SRAM Input Setup Time	t _{SVCH}	5	-	ns	
SRAM Input Hold Time	t _{CHSX}	5	-	ns	
Clock Low to Output Valid	t _{CLQV}	0	10	ns	

JTAG TIMING DIAGRAM



153 BGA PACKAGE DIMENSIONS



NOTE :

1. All Dimensions are in Millimeters.
2. Solder Ball to PCS Offset : 0.10 MAX.
3. PCB to Cavity Offset : 0.10 MAX.