M2006-01

Frequency Synthesizer

FEATURES

- Output Clock Frequency up to 700MHz
- Intrinsic Jitter <1ps rms (12kHz - 50MHz)
- Automatic Phase Slope Limiting
- Dual Differential Inputs
- Input Compatible with LVPECL, LVDS, HSTL, SSTL, etc.
- Triple Input MUX
- Configurable Input and Feedback Dividers
- Tunable Loop Filter Response
- Two Differential LVPECL outputs
- Single 3.3V Supply
- Small 9mm x 9mm SMT Package

APPLICATIONS

- SONET / SDH / 10GbE System Synchronization
- Add / Drop Muxes, Access and Edge Switches
- Line Card System Clock Cleaner / Translator
- Optical Module Clock Cleaner / Translator

DESCRIPTION

The M2006-01 integrates a high performance Phase Locked Loop (PLL) with a Voltage Controlled SAW Oscillator (VCSO) to provide a low jitter Frequency Synthesizer in a 9mm x 9mm surface mount package.

The internal high “Q” SAW filter provides low jitter signal performance and determines the output frequency of the VCSO.

Selecting between two differential LVPECL clocks or one single-ended LVCMOS / LVTTL clock provides the input reference signal to the Frequency Translator. The maximum input frequency is 700MHz.

The M2006-01 will default to a multiplying factor of 32 on power-up. The multiplying factor can be changed by serially programming the input and feedback dividers via the configuration logic.

A differential LVPECL signal provides the output clock for the device. A second differential output which can be programmed to divide the output frequency by a factor of 4 is also available. The output frequency can be momentarily increased or decreased to add or subtract one net output clock cycle by asserting the ADD_CLK or DROP_CLK inputs, respectively.

An external loop filter sets the PLL bandwidth which can be optimized to provide jitter attenuation of the input reference clock. A phase slope limiting feature, which reduces phase build-out in order to meet GR-253 MTIE upon an input transient, can be manually selected by asserting the PSL input. The phase slope limiting feature is automatically activated whenever a new input reference clock is selected.

The frequency agility, bandwidth control, and phase slope limiting features make the M2006-01 ideal for use as a clock jitter attenuator, frequency translator, and clock frequency generator in OC-3 through OC-192 applications.

ABSOLUTE MAX RATINGS

Inputs, V_I: ..... -0.5 to V_{CC}+0.5V
Output, V_O: ..... -0.5 to V_{CC}+0.5V
Supply Voltage, V_{CC}: ..... 4.6 V
Storage Temperature, T_{STO}: ..... -45°C to +100°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the DC Characteristics *or* AC Characteristics *is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.*

ISO 9001 Registered

FUNCTIONAL BLOCK DIAGRAM

The internal PLL will adjust the VCSO output frequency to be M (feedback divider) divided by R (input divider) times the selected input reference clock frequency. Note that the ratio of M/R times input frequency must be such that it falls within the “lock” range of the VCSO. The M divider (10-bits) can be programmed for a maximum value of 1023 and a minimum value of 4. The R divider (9-bits) can be set to a maximum value of 511 and a minimum value of 1.

There are two differential LVPECL outputs (Fout 0, Fout 1) which operate at the VCSO frequency. When P1 is HIGH the Fout 1 output will operate at 1/4 the VCSO frequency and when P1 is LOW Fout 1 output operates at the VCSO frequency.

The relationship between the VCSO frequency, the M and R dividers, and the input REF_CLK is defined as follows:

$$F_{VCSO} = F_{REF\_CLK} \times M / R$$

On power-up the R and M dividers are set to 1 and 32, respectively.

The input reference clock is selected from DIF_CLK 0, DIF_CLK 1, or REF_CLK by selecting the appropriate REF_SEL 0 and REF_SEL 1 inputs. When a new reference is selected the M2006-01 will automatically switch to the “phase slope limiting” mode to control the phase build-out of the output clocks.

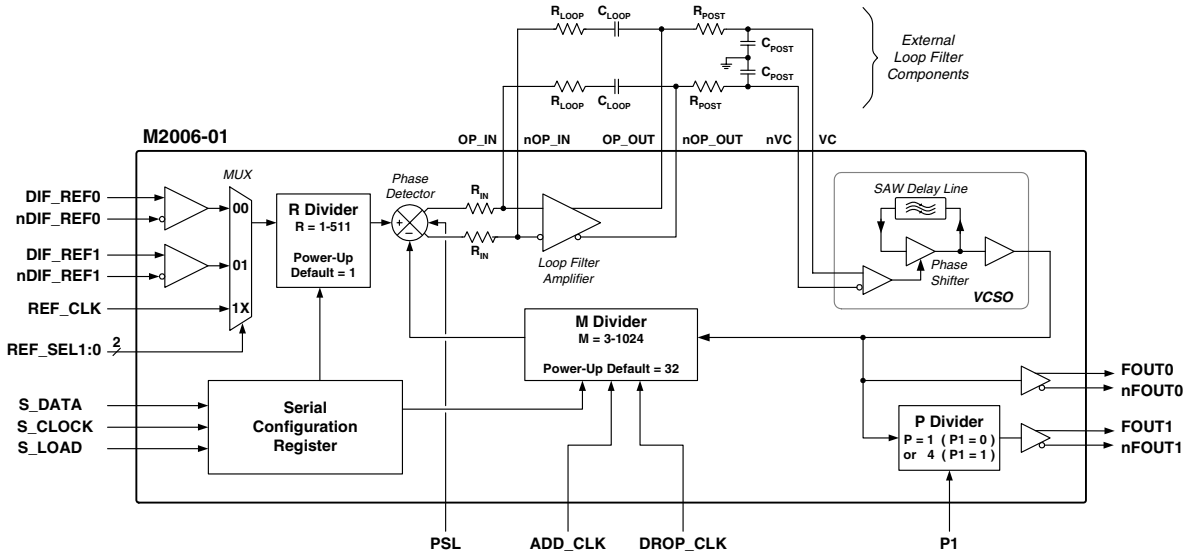
The ADD_CLK and DROP_CLK inputs increments or decrements the M (feedback) divider for one phase detector cycle. This results in a momentary increase or decrease in output frequency and an extra or missing output clock cycle relative to the input reference clock. The "phase slope limiter" is used to ensure MTIE compliance. The PSL input provides manual control.

When PSL is HIGH, the output phase slope is limited by changing the phase detector gain to a non-linear function.

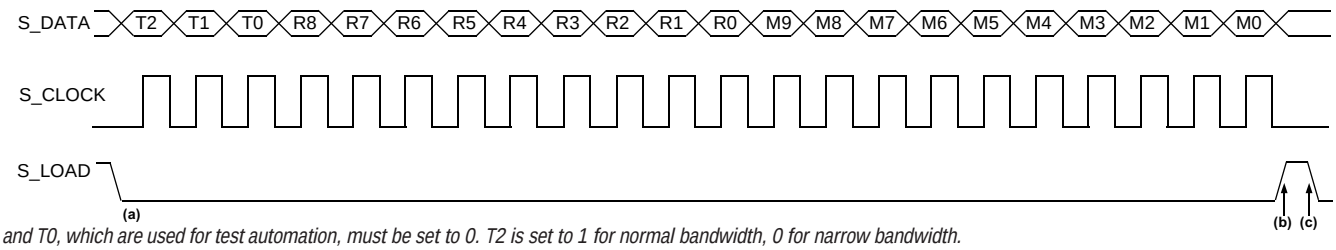
The M2006-01 is serially programmed via a 3 wire interface.

Refer to the timing diagram below (labeled "SERIAL PROGRAMMING") for the following explanation.

Serial operation begins at point "(a)", when S_LOAD is LOW; the shift register is loaded one bit at-a-time by sampling the S_DATA bits with the rising edge of S_CLOCK.
Divider load occurs at point "(b)" , when S_LOAD transitions from LOW to HIGH; all of the data in the shift register is loaded into the R and M dividers.
Latch occurs at point "(c)", on the HIGH-to-LOW transition of S_LOAD; divider values will not be affected by serial input.
(If S_LOAD is held HIGH, any S_DATA input is passed directly to the R and M dividers on each rising edge of S_CLOCK.)



SERIAL PROGRAMMING



Note: T1 and T0, which are used for test automation, must be set to 0. T2 is set to 1 for normal bandwidth, 0 for narrow bandwidth.

FUNCTIONAL DESCRIPTION

LOOP FILTER

The M2006-01 requires the use of an external loop filter via the provided filter pins. Due to the differential design, the implementation requires two identical RC filters as shown in Figure 2.

FIGURE 2

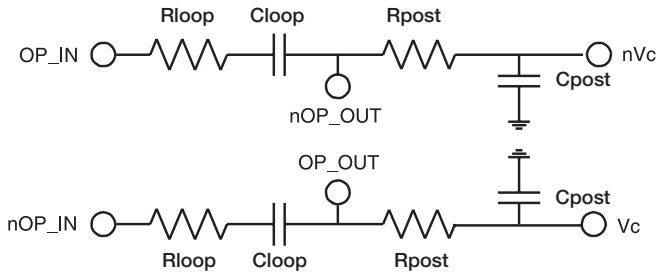


TABLE 1. EXAMPLE OF LOOP FILTER VALUES

PLL Bandwidth	Damping Factor	R loop	C loop	R post	C post
330Hz	2.0	3.9KΩ	2.2µF	20kΩ	250pF
1015Hz	2.0	12KΩ	.22µF	20kΩ	250pF
1975Hz	2.7	24KΩ	.1µF	20kΩ	250pF

Input Reference Frequency = 19.44MHz; VCSO Frequency = 622.0800MHz

PIN DESCRIPTIONS

TABLE 2

Pin Number	Name	I/O	Configuration	Description
1, 2, 3	GND	GND		Power Supply Ground
4, 9	OP_IN, nOP_IN	Analog I/O		Used for external loop filter. See Figure 2.
5, 8	nOP_OUT, OP_OUT	Analog I/O		Used for external loop filter. See Figure 2.
6, 7	nVC, VC	Input		VCSO Differential Control Voltage Input Pair
10, 14, 26	GND	GND		Power Supply Ground
11, 19, 33	Vcc	Power		Positive Supply Pins
12, 13	FOUT1, nFOUT1	Output	Unterminated	Differential output, 3.3V LVPECL levels.
15, 16	FOUT0, nFOUT0	Output	Unterminated	Differential output, 3.3V LVPECL levels.
17	P1	Input	Pull - down	Determines the output divider value. LVCMOS / LVTTL interface levels.
18	S_CLOCK	Input	Pull - down	Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. LVCMOS / LVTTL interface levels.
20	S_DATA	Input	Pull - down	Shift register serial input. Data is sampled on the rising edge of S_CLOCK. LVCMOS / LVTTL interface levels.
21	S_LOAD	Input	Pull - down	Controls transition of data from shift register into the dividers. LVCMOS / LVTTL interface levels.
22, 29	REF_SEL1, REF_SEL0	Input	Pull - down	Selects between the different reference clock inputs as the PLL reference source. LVCMOS / LVTTL interface levels.
23	NDIF_CLK0	Input	Pull - up	Inverting differential clock input. LVCMOS / LVTTL interface levels.
24	DIF_CLK0	Input	Pull - down	Non-inverting differential clock input. LVCMOS / LVTTL interface levels.
25	REF_CLK	Input	Pull - down	Reference clock input. LVCMOS / LVTTL interface levels.
27	NDIF_CLK1	Input	Pull - up	Inverting differential clock input. LVPECL levels.
28	DIF_CLK1	Input	Pull - down	Non-inverting differential clock input.
30	ADD_CLK	Input	Pull - down	Increases the output frequency by one output clock cycle for a given input clock cycle. The added clock occurs during the next input clock period following the rising edge of ADD_CLK. Only one output clock can be added for each input reference clock cycle. LVCMOS / LVTTL interface levels.
31	DROP_CLK	Input	Pull - down	Decreases the output frequency by one output clock cycle for a given input clock cycle. The deletion occurs during the next input clock period following the rising edge of DROP_CLK. Only one output clock can be deleted for each input reference clock cycle. LVCMOS / LVTTL interface levels.
32	PSL	Input	Pull - down	Asserting PSL (phase slope limiter) causes a decrease in the loop bandwidth by reducing the phase detector gain. LVCMOS / LVTTL interface levels.
34, 35, 36	DNC			No connection. Internal test pins must be left floating.

PIN CHARACTERISTICS

TABLE 4

Symbol	Parameter	Test Conditions	Min	Typical	Max	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

SERIAL MODE FUNCTION

TABLE 5

Inputs S_LOAD	Inputs S_CLOCK	Inputs S_DATA	Conditions
L	↑	Data	Serial input mode. Shift register loads state of S_DATA on each rising clock of S_CLOCK. (However, serial input does not affect the values in the R and M dividers.)
↑	L	Data	Entire contents of the shift register are passed (all at once) to the R and M dividers.
↓	L	Data	R and M divider values are latched.
L	X	X	Serial input does not affect the values in the R and M dividers.
H	↑	Data	Serial input affects dividers: S_DATA passed directly to R and M dividers as it is clocked.

Note: L = Low; H = High; X = Don't care; ↑ = Rising Edge Transition; ↓ = Falling Edge Transition

REFERENCE SELECT FUNCTION TABLE

TABLE 5C

Inputs REF_SEL1	Inputs REF_SEL0	Reference
0	0	DIF_CLK0, nDIF_CLK0
0	1	DIF_CLK1, nDIF_CLK1
1	X	REF_CLK

POWER SUPPLY DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
I_{CC}	Power Supply Current			162		mA

V_{CC} = 3.3V±5%, T_A = 0°C to 70°C

DIFFERENTIAL INPUT DC CHARACTERISTICS

Symbol	Parameter		Test Conditions	Min	Typ	Max	Units
Iib	Input High Current	nDIF_CLK0, nDIF_CLK1				5	µA
		DIF_CLK0, DIF_CLK1				150	µA
Iil	Input High Current	nDIF_CLK0, nDIF_CLK1		-150			µA
		DIF_CLK0, DIF_CLK1		-5			µA
V_{p-p}	Peak to Peak Input Voltage			0.15			V
V_{cmr}	Common Mode Input Voltage			0.5		V_{CC} - .85	V

V_{CC} = 3.3V±5%, T_A = 0°C to 70°C

LVCMOS/LVTTL DC CHARACTERISTICS

Symbol	Parameter		Test Conditions	Min	Max	Units
V_{IH}	Input High Voltage	REF_SEL0, REF_SEL1, S_LOAD, S_DATA, S_CLK, ADD_CLK, DROP_CLK, P1, PSL, REF_CLK		2	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	REF_SEL0, REF_SEL1, S_LOAD, S_DATA, S_CLK, ADD_CLK, DROP_CLK, P1, PSL, REF_CLK		-0.3	0.8	V
I_{IH}	Input High Current	REF_SEL0, REF_SEL1, S_LOAD, S_DATA, S_CLK, ADD_CLK, DROP_CLK, P1, PSL, REF_CLK			150	µA
I_{IL}	Input Low Current	REF_SEL0, REF_SEL1, S_LOAD, S_DATA, S_CLK, ADD_CLK, DROP_CLK, P1, PSL, REF_CLK		-5		µA

V_{CC} = 3.3V±5%, T_A = 0°C to 70°C

LVPECL DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	Output High Voltage		V_{CC} – 1.4	V_{CC} – 1.0	V
V_{OL}	Output Low Voltage		V_{CC} – 2.0	V_{CC} – 1.7	V
V_{p-p}	Peak-to-Peak Output Voltage		0.6	0.85	V

Note 1: Output terminated with 50Ω to V_{CC} –2.V

INPUT FREQUENCY CHARACTERISTICS

Symbol	Parameter		Test Conditions	Min	Max	Units
F_{IN}	Input Frequency	DIF_CLK0, nDIF_CLK0 DIF_CLK1, nDIF_CLK1		0.3	700	MHz
		S_CLOCK			50	MHz
		REF_CLK		0.3	200	MHz

Note 1: Output terminated with 50Ω to V_{CC}–2.V

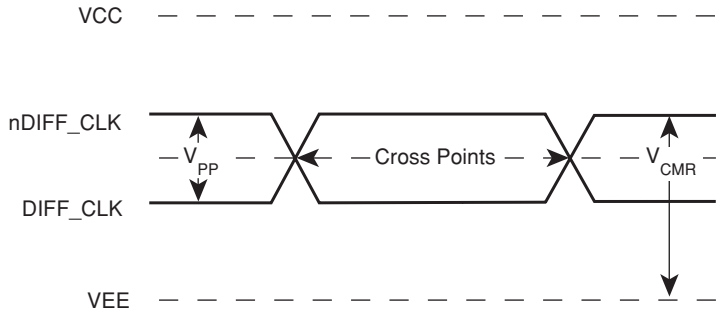
AC CHARACTERISTICS

Symbol	Parameter		Test Conditions	Min	Typ	Max	Units
F_{OUT}	Output Frequency			75		700	MHz
ØN	Single Side Band	1kHz offset	1kHz offset		-72		dBc/Hz
	Phase Noise	10kHz offset	10kHz offset		-94		dBc/Hz
	@ 622MHz	100kHz offset	100kHz offset		-123		dBc/Hz
J (t)	Jitter (RMS)	Non-deterministic	50kHz to 80MHz		0.50	1	ps
odc	Output Duty Cycle				50		%
t_R (Note 1)	Output Rise Time for output pairs FOUT0, nFOUT0 & FOUT1, nFOUT1	FOUT = 155MHz	20% to 80%, each output of pair measured is terminated into 50Ω load biased at Vcc-2V	350	450	550	ps
		FOUT = 311MHz		325	425	500	ps
		FOUT = 622MHz		200	275	350	ps
t_F (Note 1)	Output Fall Time for output pairs FOUT0, nFOUT0 & FOUT1, nFOUT1	FOUT = 155MHz	20% to 80%, each output of pair measured is terminated into 50Ω load biased at Vcc-2V	350	450	550	ps
		FOUT = 311MHz		325	425	500	ps
		FOUT = 622MHz		200	275	350	ps
t_S	Setup Time	S_DATA to S_CLK		5			ns
		S_CLK to S_LOAD		5			ns
t_H	Hold Time	S_DATA to S_CLK		5			ns
		S_CLK to S_LOAD		5			ns
t_{LOCK}	PLL Lock Time					100	ms
t_{PW}	Input Pulse Width	S_LOAD		10			ns
		ADD_CLK		10			ns
		DROP_CLK		10			ns
MTIE	Mean Time Interval Error		Compliant with GR-253-CORE				

Note: The output frequencies of 155MHz, 311MHz and 622MHz were chosen for device characterization as these are common optical network clock frequencies.

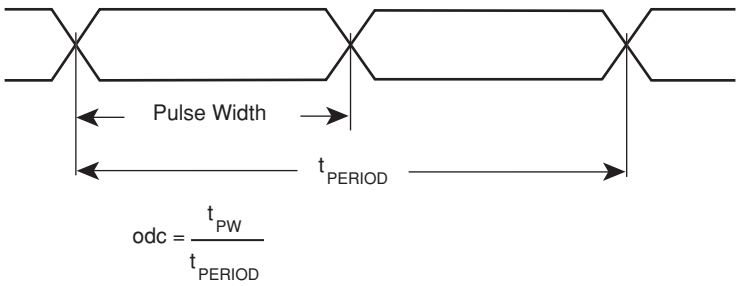
PARAMETER MEASUREMENT INFORMATION

DIFFERENTIAL INPUT LEVEL

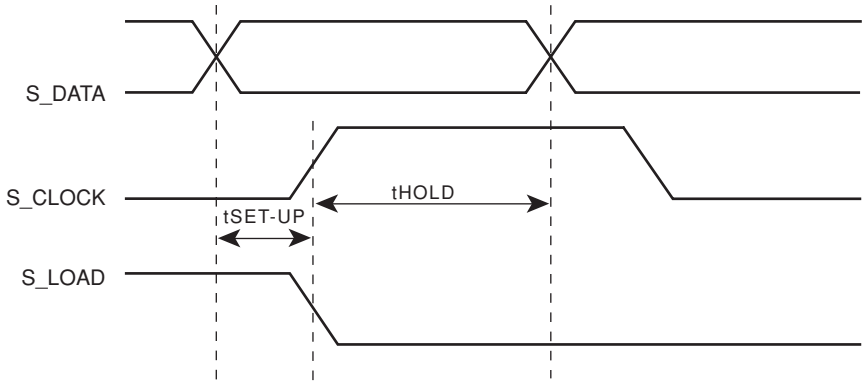


INPUT AND OUTPUT RISE AND FALL TIME

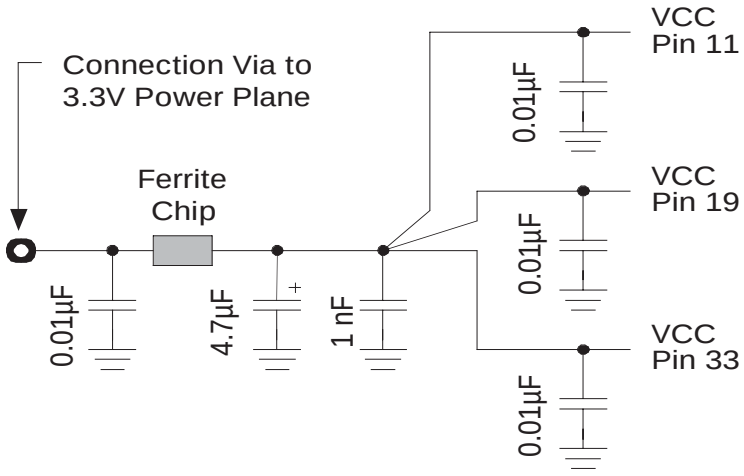
ODC & t_{PERIOD}



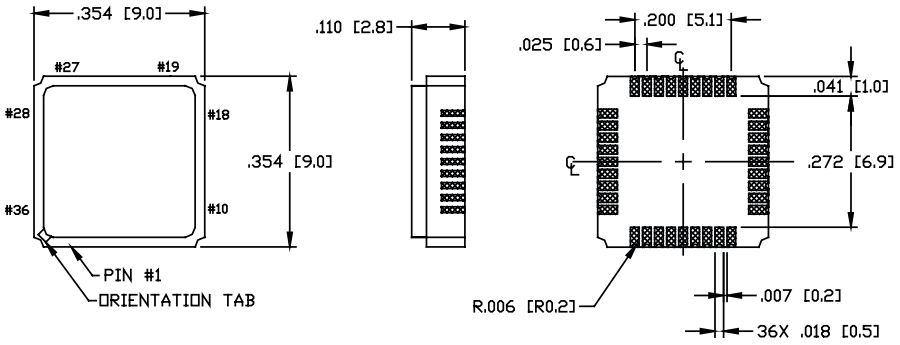
SETUP AND HOLD TIME

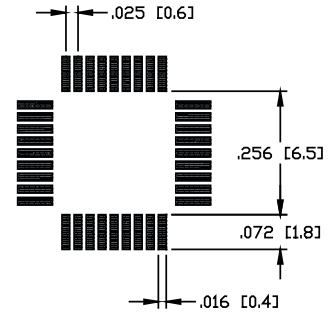


RECOMMENDED POWER SUPPLY DECOUPLING



MECHANICAL DIMENSIONS & PIN CONFIGURATION





RECOMMENDED FOOTPRINT

PIN#	DESIGNATION
1	GND
2	GND
3	GND
4	OP_IN
5	nOP_OUT
6	nVC
7	VC
8	OP_OUT
9	nOP_IN
10	GND
11	VCC
12	FOUT1
13	nFOUT1
14	GND
15	FOUT0
16	nFOUT0
17	P1

PIN#	DESIGNATION
18	S_CLOCK
19	VCC
20	S_DATA
21	S_LOAD
22	REF_SEL1
23	nDIF_CLK0
24	DIF_CLK0
25	REF_CLK
26	GND
27	nDIF_CLK1
28	DIF_CLK1
29	REF_SEL0
30	ADD_CLK
31	DROP_CLK
32	PSL
33	VCC
34, 35, 36	DNC

1. DIMENSIONS ARE IN INCHES, (DIMENSIONS) ARE IN MM.

ORDERING INFORMATION

PART NUMBER M2006-01-622.0800

Series

Model

VCSO Center Frequency
(i.e. 622.0800MHz)

Available VCSO Frequencies	
622.0800	669.1281
625.0000	669.3266
627.3296	672.1600
644.5313	690.5692
666.5143	693.4830

Micro Networks
An Integrated Circuit Systems Company
324 Clark Street ■ Worcester, MA 01606 ■ tel: 508-852-5400 ■ fax: 508-852-8456
European Sales Headquarters ■ Hertogsingel 20 ■ 6214 AD Maastricht ■ The Netherlands ■ tel: +31-43-32-70912 ■ fax: +31-43-32-70715
www.micronetworks.com