UM61M256 Series

32K X 8, 3.3V I/O High Speed CMOS SRAM

Features

- Single +5V power supply
- Access times: 12/15 ns (max.)
- Current: Operating: 150mA (max.)
  Standby: 12mA (max.)
- Full static operation, no clock or refreshing required
- 3.3V I/O compatible
- All inputs and outputs directly TTL compatible
- Common I/O using three-state output
- Data retention voltage: 3V (min.)
- Available in 28-pin SOJ and SKINNY DIP packages

General Description

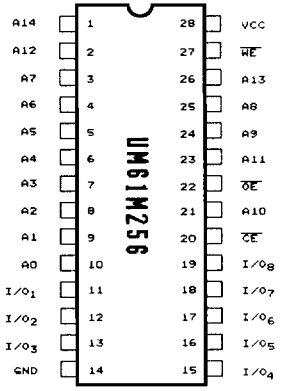
The UM61M256 is a high-speed, low-power 262,144-bit static random access memory organized as 32,768 words by 8 bits and operates on a single 5V power supply. It is built using UMC's high performance CMOS process.

Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

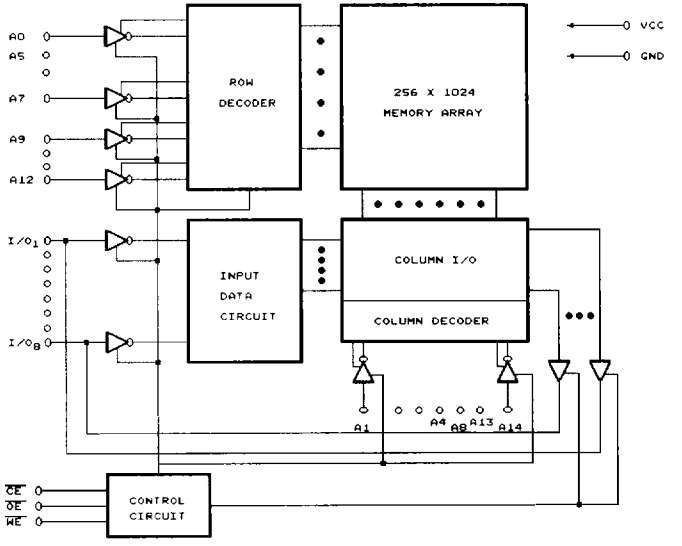
Special designed output circuitry allows for easy interfacing with a 5V or 3.3V system bus and is ideal for mixed voltage systems.

Minimum standby power is drawn by this device when $\overline{CE}$ is at a high level, independent of the other input levels. Data retention is guaranteed at a power supply voltage of as low as 3V.

Pin Configuration



Block Diagram



Pin Description

Pin No.	Symbol	Description
1-10, 21, 23-26	A0 - A14	Address Input
27	$\overline{WE}$	Write Enable
22	$\overline{OE}$	Output Enable
20	$\overline{CE}$	Chip Enable
11-13, 15-19	I/O1 - I/O8	Data Input/Output
28	VCC	Power Supply (+5V)
14	GND	Ground

Recommended DC Operating Conditions

(T_A = 0°C to + 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.75	5.0	5.25	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	VCC + 0.5	V
V_{IL}	Input Low (1) Voltage	-0.5	0	+0.8	V
C_L	Output Load	-	-	30	pF

Absolute Maximum Ratings*

VCC to GND . . . . . -0.5V to +7.0V
IN, IN/OUT Volt to GND . . . . . -0.5V to VCC +0.5V
Operating Temperature, Topr . . . . . 0°C to +70°C
Storage Temperature, Tstg . . . . . -55°C to +125°C
Temperature under Bias, Tbias . . . . . -10°C to +85°C
Power Dissipation, Pt 1.0W

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (T_A = 0°C to + 70°C, VCC = 5V ± 5%, GND = 0V)

Symbol	Parameter	UM61M256-12/15		Unit	Conditions	Note
		Min.	Max.			
$\|I_{LI}\|$	Input Leakage Current	–	2	μA	V_{IN} = GND to VCC	
$\|I_{LO}\|$	Output Leakage Current	–	2	μA	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = GND to VCC	
I_{CC1}	Dynamic Operating Current	–	150	mA	$\overline{CE}$ = V_{IL}, $I_{I/O}$ = 0mA	1, 2
I_{SB}	Standby Power Supply Current	–	30	mA	$\overline{CE}$ = V_{IH}	
I_{SB1}		–	12	mA	$\overline{CE}$ ≥ VCC - 0.2V V_{IN} ≥ VCC -0.2V or V_{IN} ≤ 0.2V	

DC Electrical Characteristics (continued)

Symbol	Parameter	UM61M256-12/15		Unit	Conditions	Note
		Min.	Max.			
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 8 mA	
V_{OH}	Output High Voltage	2.4	3.3	V	I_{OH} = -4 mA	

Note: 1. V_{IL} = -3.0V for pulses of less than 20 ns.
2. I_{CC1} is dependent on output loading, cycle rates, and Read/Write patterns.

Truth Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O Operation	Supply Current
Standby	H	X	X	High Z	I_{SB}, I_{SB1}
Output Disable	L	H	H	High Z	I_{CC}, I_{CC1}
Read	L	L	H	D_{OUT}	I_{CC}, I_{CC1}
Write	L	X	L	D_{IN}	I_{CC}, I_{CC1}

Note: X: H or L

Capacitance (T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}*	Input Capacitance		10	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance		10	pF	$V_{I/O}$ = 0V

* These parameters are sampled and not 100% tested.

AC Characteristics (T_A = 0°C to +70°C, VCC = 5V ± 5%)

Symbol	Parameter	UM61M256-12		UM61M256-15		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	12	–	15	–	ns
t_{AA}	Address Access Time	–	12	–	15	ns
t_{ACE}	Chip Enable Access Time	–	12	–	15	ns
t_{OE}	Output Enable to Output Valid	–	7	–	9	ns
t_{CLZ}	Chip Enable to Output in Low Z	2	–	3	–	ns
t_{OLZ}	Output Enable to Output in Low Z	2	–	2	–	ns
t_{CHZ}	Chip Disable to Output in High Z	0	7	0	8	ns
t_{OHZ}	Output Disable to Output in High Z	2	6	2	7	ns
t_{OH}	Output Hold from Address Change	2	–	3	–	ns
Write Cycle						
t_{WC}	Write Cycle Time	12	–	15	–	ns
t_{CW}	Chip Enable to End of Write	10	–	12	–	ns
t_{AS}	Address Setup Time of Write	0	–	0	–	ns
t_{AW}	Address Valid to End of Write	10	–	12	–	ns
t_{WP}	Write Pulse Width	8	–	10	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	ns

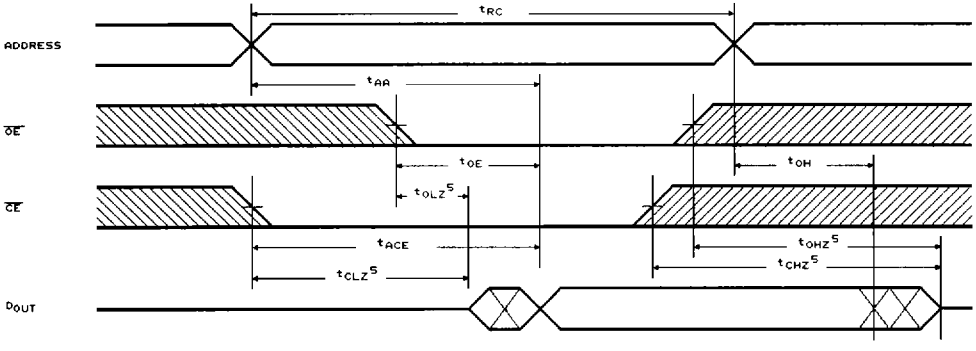
AC Characteristics (continued)

Symbol	Parameter	UM61M256-12		UM61M256-15		Unit
		Min.	Max.	Min.	Max.	
t_{WHZ}	Write to Output in High Z	0	7	0	8	ns
t_{DW}	Data to Write Time Overlap	8	–	10	–	ns
t_{DH}	Data Hold from Write Time	0	–	0	–	ns
t_{OW}	Output Active from End of Write	5	–	5	–	ns

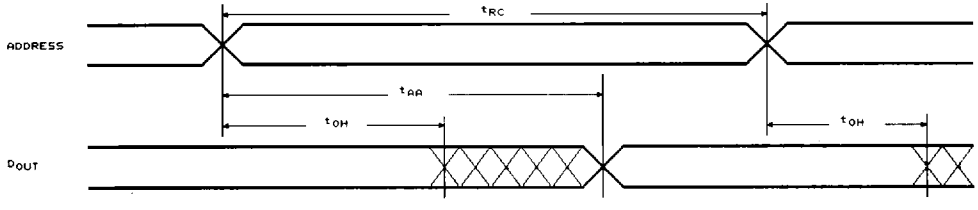
Notes: t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Timing Waveforms

Read Cycle 1 (1)

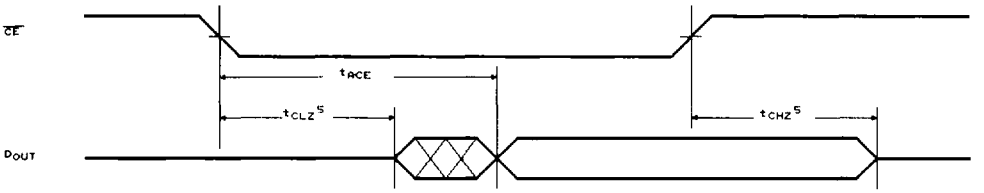


Read Cycle 2 (1, 2, 4)



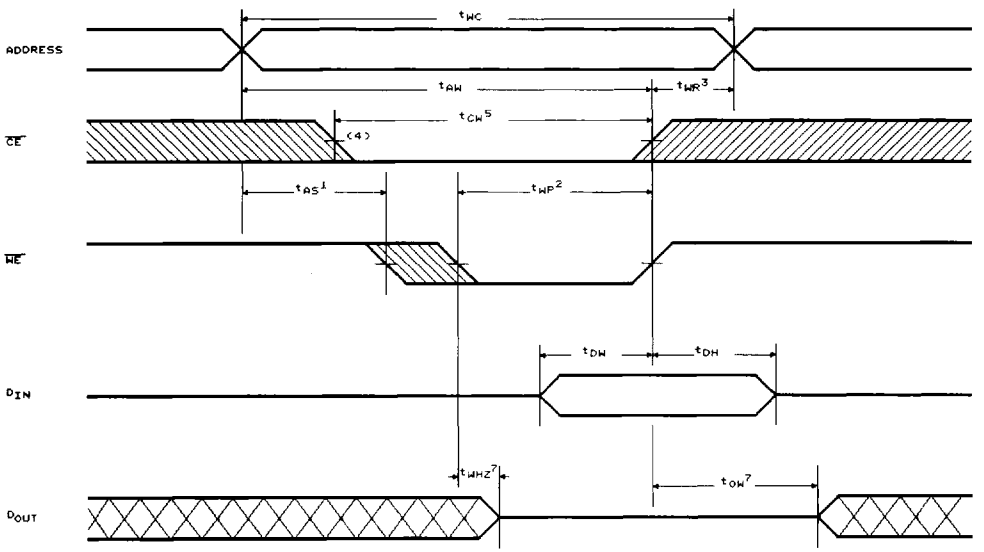
Timing Waveforms (continued)

Read Cycle 3 (1, 3, 4)



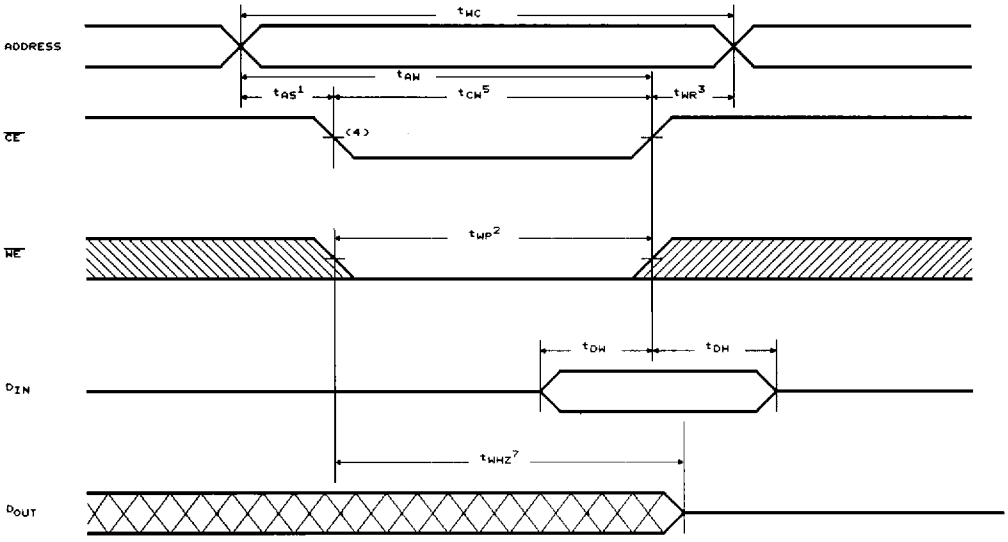
Notes: 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously enabled, $\overline{CE}$ = VIL.
3. Address valid prior to or coincident with $\overline{CE}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

Write Cycle 1 (6)
(Write Enable Controlled)



Timing Waveforms (continued)

Write Cycle 2 [6]
(Chip Enable Controlled)



Notes: 1. t_{AS} is measured from the address valid to the beginning of Write.
2. A Write occurs during the overlap (t_{WP}) of a low $\overline{CE}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earliest of $\overline{CE}$ or $\overline{WE}$ going high to the end of the Write cycle.
4. If the $\overline{CE}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. t_{CW} is measured from the later of $\overline{CE}$ going low to the end of Write.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).
7. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Fig. 1, 2

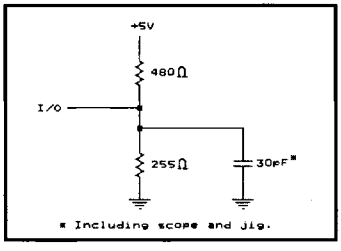


Figure 1. Output Load

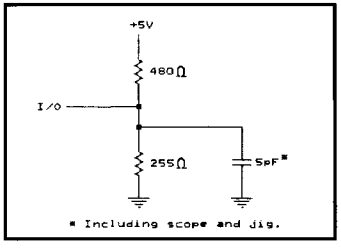


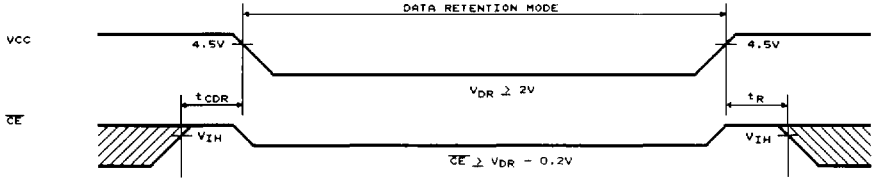
Figure 2. Output Load for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ}, and t_{OW}

Data Retention Characteristics (T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Max.	Unit	Conditions
V_{DR}	VCC for Data Retention	3.0	5.5	V	$\overline{CE} \geq VCC - 0.2V$
I_{CCDR}	Data Retention Current	–	12	mA	VCC = 3.0V, $\overline{CE} \geq VCC - 0.2V$ $V_{IN} \geq VCC - 0.2V$ or $V_{IN} \leq 0.2V$
t_{CDR}	Chip Disable to Data Retention Time	0	–	ns	See Retention Waveform
t_R	Operation Recovery Time	t_{RC}*	–	ns	

* t_{RC} = Read Cycle Time

Low VCC Data Retention Waveform



Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (mA)	Package
UM61M256K-12	12	150	12	28L SKINNY
UM61M256S-12	12	150	12	28L SOJ
UM61M256K-15	15	150	12	28L SKINNY
UM61M256S-15	15	150	12	28L SOJ