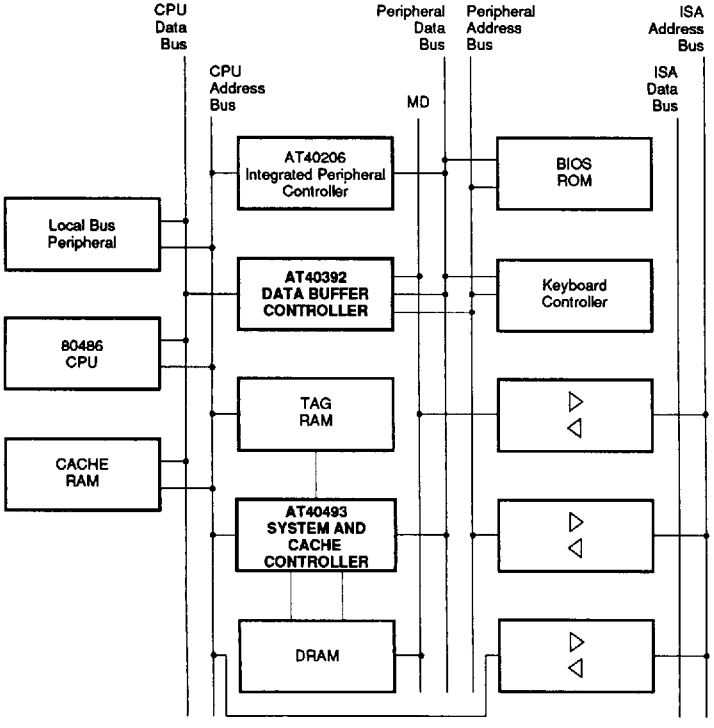
Features

- Two-Chip PC/AT Compatible Chip Set for 80486 Based Systems Operating up to 50 MHz
  - AT40493 System and Cache Controller
  - AT40392 Data Buffer Controller
- Two 160-Pin Quad Flatpacks
- On-Chip Support for Direct-Mapped Write-Back Cache
- 0 Wait State Cache Read Hit and Programmable 0/1 Wait State Cache Write Hit
- Two Programmable Non-Cacheable Regions
- On-Chip Tag Comparator
- Burst Line Fill During Cache Read Misses
- Page Mode Main Memory Operation with Programmable Wait States Supporting Platform Memory Sizes up to 64 Mbytes
- Support for 256K, 1-Mbit and 4-Mbit DRAMs
- Low Power CAS# Before RAS#, Transparent DRAM Refresh
- Low Power, Slow Refresh for Laptop PC Operation
- Parity Generation and Detection
- Support for Shadow RAM
- Cacheable Video BIOS Option
- 8042 Emulation for Fast CPU Reset and Gated A20 Generation
- ISA Bus Control with Programmable Clock
- 0 or 1 Wait State for 16-Bit ISA Bus Cycles
- Support for Local Bus Peripherals
- Supports 2-1-1-1 and 3-2-2-2 Cache and DRAM Burst Cycles

Block Diagram



80486 PC/AT Chip Set

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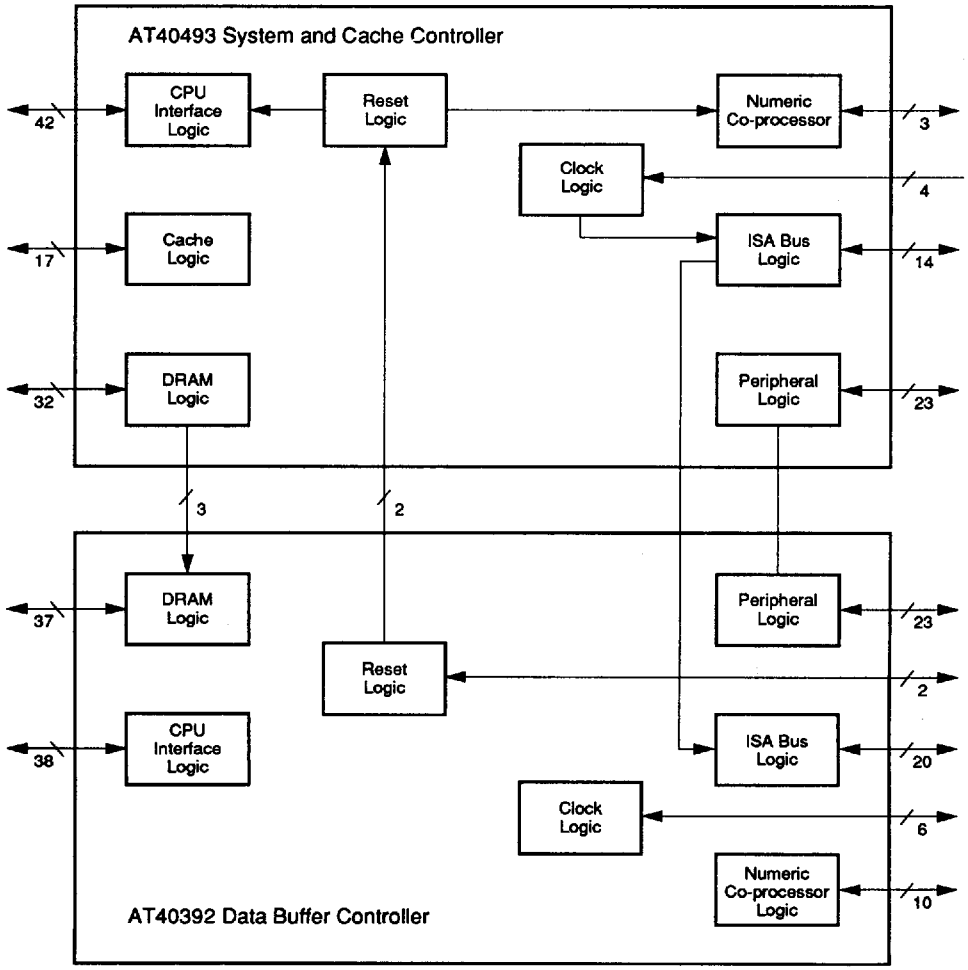
Description

The Atmel AT40493/AT40392 chip set is an IBM PC/AT compatible chip set for 80486 based systems operating up to 50 MHz. The high integration and an on-chip write-back, direct-mapped cache controller design allows maximum system performance. Together with a peripheral controller, such as the AT40206 integrated peripheral controller, a very high performance, yet low cost, 80486 motherboard can be built with a minimum number of components.

The AT40493 system controller performs the system control, memory and cache control functions. The system control logic consists of the following logic blocks: CPU control, AT bus cycle control, numeric co-processor control, synchronous clock circuitry and peripheral bus control. The memory and cache controller functions consist of a write-back, direct-mapped cache controller and a paged mode DRAM controller. The AT40493 supports cache sizes up to 512 Kbytes (16-byte line size), platform memory sizes up to 64 Mbytes and burst mode for all system configurations.

The AT40392 data buffer controller performs the data buffer and co-processor interface functions. The data buffer logic performs bus conversion logic for various 8-, 16- and 32-bit data movements as required among the system buses. The other functions of the AT40392 are co-processor interface, keyboard controller decoding, reset and generation of various peripheral clocks.

Low cost systems are made possible through the support of single ROM/EPROM BIOS configurations. The BIOS ROM/EPROM can be either 8-bit or 16-bit. DRAM is located on the system platform bus, thus reducing DRAM speed requirements by at least 15 ns.



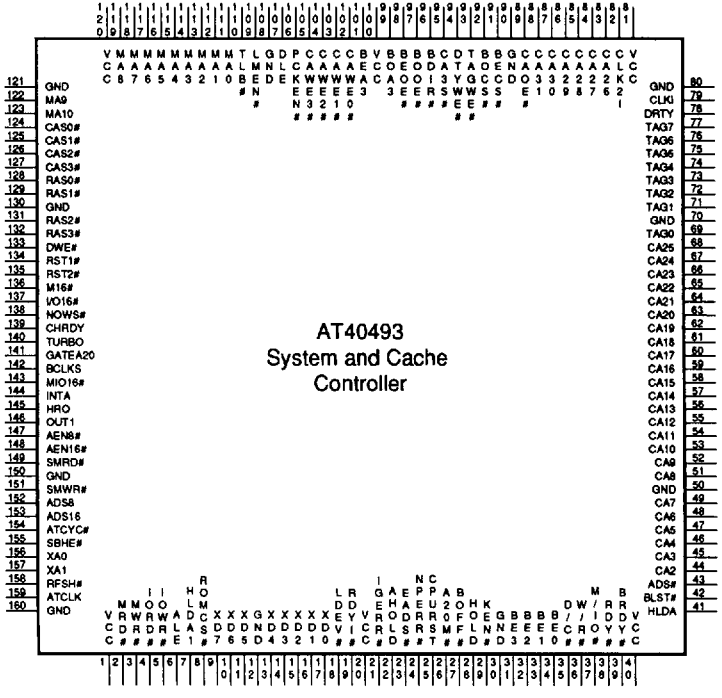
Atmel AT40493 System and Cache Controller

- **Programmable ISA bus clock generator**
- **CPU and numeric co-processor reset control**
- **Direct-mapped write-back cache controller**
- **0 wait state cache read hit and programmable 0/1 wait state cache write hit**
- **Two programmable non-cacheable regions**
- **Cacheable video BIOS option**
- **On-chip tag RAM comparator**
- **Burst line fill during cache read misses**
- **Programmable page mode DRAM controller for 256K, 1-Mbit, and 4-Mbit DRAMs for platform memory sizes up to 64 Mbytes**
- **Decoupled system platform and ISA bus DRAM refresh**
- **Low power CAS# before RAS#, transparent DRAM refresh**
- **Slow refresh option**
- **Shadow RAM support**
- **Programmable 0/1 wait state for ISA bus cycles**
- **Supports 2-1-1-1 and 3-2-2-2 cache and DRAM burst cycles**

The Atmel AT40493 is a highly integrated system and cache controller for 16 MHz, 20 MHz, 25 MHz, 33 MHz and 50 MHz 80486 PC/AT systems. When combined with the AT40392 data buffer controller and the AT40206 integrated peripheral controller, a powerful but low cost PC/AT can be built with minimal components.

The AT40493 performs all the system control, memory control, cache control, and bus arbitration functions for an 80486 PC/AT system including the reset and power shutdown functions and synchronous CPU and ISA bus clocks generation. The flexible memory controller supports system memory sizes up to 64 Mbytes with a wide range of DRAMs. The direct-mapped write-back cache controller implements a high performance cache system while requiring minimal external components. The functions of the AT40493 are programmed through twelve configuration registers.

Pin Configuration



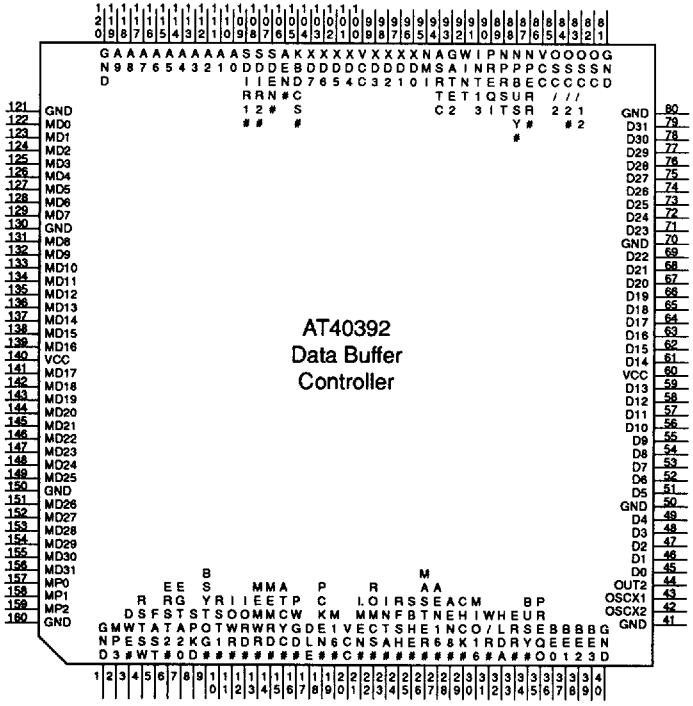
AT40392 Data Buffer Controller

- **Data bus conversions**
- **DRAM parity generation and detection**
- **ISA bus direction control**
- **Reset logic**
- **Peripheral clock generation**
- **Keyboard and real-time clock chip select**
- **Speaker control**
- **PortB, 70H and NMI logic**
- **Numeric co-processor interface**
- **Keyboard reset and Gate A20 emulation logic**

The Atmel AT40392 is a highly integrated data buffer controller for 16 MHz, 20 MHz, 25 MHz, 33 MHz and 50 MHz 80486 based PC/AT systems. Together with the AT40493 system and cache controller and the AT40206 integrated peripheral controller, a low cost yet powerful PC/AT can be built with minimal components.

The AT40392 data buffer controller performs all of the data buffering control required in a 486 PC/AT system. Under the control of the CPU and the AT40493 system and memory controller, the AT40392 routes data to and from the CPU bus, MD bus, XD bus and the ISA bus, while also providing any necessary data size conversions. The AT40392 also performs high byte to low byte and low byte to high byte swapping on the ISA bus. For platform DRAM accesses, the AT40392 performs parity error checking and generation.

Pin Configuration



Ordering Information

CPU Clock (MHz)	Power Supply	Ordering Code	Package	Operation Range
25	5 V ± 5%	AT40493-25 AT40392-25	160Q 160Q	Commercial (0°C to 70°C)
33	5 V ± 5%	AT40493-33 AT40392-33	160Q 160Q	Commercial (0°C to 70°C)
50	5 V ± 5%	AT40493-50 AT40392-50	160Q 160Q	Commercial (0°C to 70°C)

Package Type	
160Q	160 Lead, Plastic Gull Wing Quad Flat Package (PQFP)