



Overview

The H8/534, H8/536 and H8/537 are CMOS microcomputer units (MCUs) comprising a CPU core plus a full range of supporting functions \$BQa (Jn entire system integrated onto a single chip.

The CPU features a highly orthogonal instruction set that permits addressing modes and data sizes to be specified independently in each instruction. An internal 16-bit architecture and 16-bit access to on-chip memory enhance the CPU's data-processing capability and provide the speed needed for realtime control applications.

The on-chip supporting functions include RAM, ROM, timers, a serial communication interface (SCI), A/D conversion, and I/O ports. An on-chip data transfer controller (DTC) can transfer data in either direction between memory and I/O independently of the CPU.

For the on-chip ROM, a choice is offered between masked ROM and programmable ROM (PROM). The PROM version can be programmed by the user with a general-purpose PROM writer.



Function Overview

Features	Description			
CPU	General-register architecture · Eight 16-bit general registers · Five 8-bit and two 16-bit control registers			
	High speed · Maximum clock rates			
	H8/534, H8/536	S- and A-mask products	5-V version	16 MHz (oscillator frequency: 32 MHz)
			3-V version	10 MHz (oscillator frequency: 20 MHz)
			2.7-V version	8 MHz (oscillator frequency: 16 MHz)
		U-mask products	5-V version	16 MHz (oscillator frequency: 16 MHz)
	H8/537		5-V version	16 MHz (oscillator frequency: 16 MHz)
			3-V version	10 MHz (oscillator frequency: 10 MHz)
			2.7-V version	8 MHz (oscillator frequency: 8 MHz)
	Two CPU operating modes · Minimum mode: Supports an address space of up to 64 kbytes			

	<ul style="list-style-type: none"> ·Maximum mode: Supports an address space of up to 1 Mbyte Highly orthogonal instruction set ·The addressing mode and data size can be specified independently for each instruction. 1.5 address instructions ·Register-register type ·Register-memory type Instruction set optimized for the C language ·Special short formats for frequently-used instructions and addressing modes 												
Memory	<ul style="list-style-type: none"> · PROM or mask ROM · high-speed on-chip RAM <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Product Name</th> <th>RAM</th> <th>ROM</th> </tr> </thead> <tbody> <tr> <td>H8/534</td> <td>2 kbytes</td> <td>32 kbytes</td> </tr> <tr> <td>H8/536</td> <td>2 kbytes</td> <td>62 kbytes</td> </tr> <tr> <td>H8/537</td> <td>4 kbytes</td> <td>124 kbytes</td> </tr> </tbody> </table>	Product Name	RAM	ROM	H8/534	2 kbytes	32 kbytes	H8/536	2 kbytes	62 kbytes	H8/537	4 kbytes	124 kbytes
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16-bit free-running timer (FRT) (3 channels)	<p>Each channel provides:</p> <ul style="list-style-type: none"> ·One free-running counter (which can count external events) ·Two output-compare registers ·One input-capture register 												
8-bit timer (1 channel)	<ul style="list-style-type: none"> ·One 8-bit up-counter (which can count external events) ·Two time constant registers 												
PWM timer (3 channels)	<ul style="list-style-type: none"> ·Duty: Generates pulses with any duty ratio from 0 to 100% ·Resolution: 1/250 												
Watchdog timer (WDT) (1 channel)	<ul style="list-style-type: none"> ·Generates a reset or external output on overflow ·Can also be used as an interval timer 												
Serial communication interface (SCI) (2 channels)	<ul style="list-style-type: none"> ·Synchronous or asynchronous mode (selectable) ·Full duplex: can send and receive simultaneously ·Built-in dedicated baud rate generator 												
A/D converter	<ul style="list-style-type: none"> ·Resolution: 10 bits ·Eight channels: single mode or scan mode (selectable) ·Sample-and-hold function ·A/D conversion start can be triggered by an external signal 												
I/O ports	<ul style="list-style-type: none"> ·57 I/O pins: six 8-bit ports, one 5-bit port, one 4-bit port ·8 input-only pins: one 8-bit port 												

<p>Interrupt controller (INTC)</p>	<p>·7 external interrupt pins: NMI, IRQ0, IRQ1 to IRQ5 ·23 internal interrupts ·8 priority levels (settable)</p>																																				
<p>Data transfer controller (DTC)</p>	<p>Supports bidirectional data transfers between memory and I/O space independent of the CPU</p>																																				
<p>Wait-state controller (WSC)</p>	<p>Can insert wait states in accesses to external memory or the external I/O space</p>																																				
<p>Operating modes</p>	<p>5 operating modes</p> <table border="1" data-bbox="467 600 1365 1421"> <thead> <tr> <th>Model Name</th> <th>Mode No.</th> <th>Mode</th> <th>Address Space</th> </tr> </thead> <tbody> <tr> <td rowspan="5">H8/534, H8/536</td> <td>Mode 1</td> <td>Expanded minimum mode (ROM disabled)</td> <td>64 kbytes</td> </tr> <tr> <td>Mode 2</td> <td>Expanded minimum mode (ROM enabled)</td> <td>64 kbytes</td> </tr> <tr> <td>Mode 3</td> <td>Expanded maximum mode (ROM disabled)</td> <td>1 Mbytes</td> </tr> <tr> <td>Mode 4</td> <td>Expanded maximum mode (ROM enabled)</td> <td>1 Mbytes</td> </tr> <tr> <td>Mode 7</td> <td>Single-chip mode</td> <td>-</td> </tr> <tr> <td rowspan="5">H8/537</td> <td>Mode 1</td> <td>Expanded minimum mode (ROM disabled)</td> <td>64 kbytes</td> </tr> <tr> <td>Mode 2</td> <td>Expanded maximum mode (ROM enabled)</td> <td>128 kbytes</td> </tr> <tr> <td>Mode 3</td> <td>Expanded maximum mode (ROM disabled)</td> <td>1 Mbytes</td> </tr> <tr> <td>Mode 4</td> <td>Expanded maximum mode (ROM enabled)</td> <td>1 Mbytes</td> </tr> <tr> <td>Mode 7</td> <td>Single-chip mode</td> <td>-</td> </tr> </tbody> </table> <p>Low power modes ·Sleep mode ·Software standby mode ·Hardware standby mode</p>	Model Name	Mode No.	Mode	Address Space	H8/534, H8/536	Mode 1	Expanded minimum mode (ROM disabled)	64 kbytes	Mode 2	Expanded minimum mode (ROM enabled)	64 kbytes	Mode 3	Expanded maximum mode (ROM disabled)	1 Mbytes	Mode 4	Expanded maximum mode (ROM enabled)	1 Mbytes	Mode 7	Single-chip mode	-	H8/537	Mode 1	Expanded minimum mode (ROM disabled)	64 kbytes	Mode 2	Expanded maximum mode (ROM enabled)	128 kbytes	Mode 3	Expanded maximum mode (ROM disabled)	1 Mbytes	Mode 4	Expanded maximum mode (ROM enabled)	1 Mbytes	Mode 7	Single-chip mode	-
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<p>Other features</p>	<p>·E clock output available</p>																																				



Product Lineup

Model Name		Package	ROM
H8/534	S-mask products	HD6475348SCG	84-pin windowed LCC (CG-84)
		HD6475348SCP	84-pin PLCC (CP-84)
		HD6475348SF	80-pin QFP (FP-80A)
		HD6475348STF	80-pin TQFP (TFP-80C)
		HD6435348SCP	84-pin PLCC (CP-84)
		HD6435348SF	80-pin QFP (FP-80A)
	HD6435348STF	80-pin TQFP (TFP-80C)	
	A-mask products	HD6435348ACP	84-pin PLCC (CP-84)
		HD6435348AF	80-pin QFP (FP-80A)
		HD6435348SAF	80-pin TQFP (TFP-80C)
	U-mask products	HD6475348UCG	84-pin windowed LCC (CG-84)
		HD6475348UCP	84-pin PLCC (CP-84)
HD6475348UF		80-pin QFP (FP-80A)	
HD6475348UTF		80-pin TQFP (TFP-80C)	
HD6475348UCP		84-pin PLCC (CP-84)	
HD6475348UF		80-pin QFP (FP-80A)	
HD6475348UTF	80-pin TQFP (TFP-80C)		
H8/536	S-mask products	HD6475368SCG	84-pin windowed LCC (CG-84)
		HD6475368SCP	84-pin PLCC (CP-84)
		HD6475368SF	80-pin QFP (FP-80A)
		HD6475368STF	80-pin TQFP (TFP-80C)
		HD6435368SCP	84-pin PLCC (CP-84)
		HD6435368SF	80-pin QFP (FP-80A)
	HD6435368STF	80-pin TQFP (TFP-80C)	
	A-mask products	HD6435368ACP	84-pin PLCC (CP-84)
		HD6435368AF	80-pin QFP (FP-80A)
		HD6435368ATF	80-pin TQFP (TFP-80C)
	U-mask products	HD6475368UCG	84-pin windowed LCC (CG-84)
		HD6475368UCP	84-pin PLCC (CP-84)
HD6475368UF		80-pin QFP (FP-80A)	
HD6475368UTF		80-pin TQFP (TFP-80C)	
HD6435368UCP		84-pin PLCC (CP-84)	
HD6435368UF		80-pin QFP (FP-80A)	
HD6435368UTF	80-pin TQFP (TFP-80C)		

H8/537	HD6475378CP	84-pin PLCC (CP-84)	PROM
	HD6475378CG	84-pin windowed LCC (CG-84)	
	HD6475378F	80-pin QFP (FP-80A)	
	HD647538TF	80-pin TQFP (TFP-80C)	
	HD6435378CP	84-pin PLCC (CP-84)	Mask ROM
	HD6435378F	80-pin QFP (FP-80A)	
	HD6435378TF	80-pin TQFP (TFP-80C)	

·H8/534 and H8/536

Specifications		Product Class			
		S- and A-Mask Products			U-Mask Products
		High-Speed Version	Low-Voltage Version		
		16-MHz Version	3-V Version	2.7-V Version	
Clock oscillator divisor		Divided by 2	Divided by 2	Divided by 2	No divisor
Operating frequency range		2 to 16 MHz	2 to 10 MHz	2 to 8 MHz	2 to 16 MHz
Supply voltage range		5 V \pm 10%	3 V to 5.5 V	2.7 V to 5.5 V	5 V \pm 10%
Model name	PROM versions	HD6475368S	HD6475368SV	HD6475368SV	HD6475368U
		HD6475348S	HD6475348SV	HD6475348SV	HD6475348U
	Mask ROM versions	HD6435368S	HD6435368SV	HD6435368SV	HD6435368U
		HD6435368A	HD6435368AV	HD6435368AV	
		HD6435348S	HD6435348SV	HD6435348SV	HD6435348U
		HD6435348A	HD6435348AV	HD6435348AV	

·H8/537

Specifications		Model Name		
		High-Speed Version	Low-Voltage Version*	
		16-MHz Version	3-V Version	2.7-V Version
Type	PROM	HD6475378	HD6475378V	HD6475378V
	Mask ROM	HD6435378	HD6435378V	HD6435378V
Operating frequency		2 to 16 MHz	2 to 10 MHz	2 to 8 MHz
Operating power-supply voltage		5 V \pm 10%	3 V to 5.5 V	2.7 V to 5.5 V

Note: The product codes of the 3-V and 2.7-V low-voltage versions include a suffix that identifies the frequency version. The examples shown below are for the H8/536 PROM version in an 80-pin QFP package

Examples: 3-V version: HD6475368SVF10

2.7-V version: HD6475368DVF8



Internal Block Diagram



Pin Arrangement

·CP-84,Top V0000053195 00000 n 0000053371 00000 n 0000053428 00000 n 0000053538 00000 n
0000053650 00000 n 0000053707 00000 n 0000053764 00000 n 0000053821 00000 n 0000053930
00000 n 0000054064 00000 n 0000054121 00000 n 0