Integrated Device Technology, Inc

1 MEGABIT (128K x 8) REGISTERED/BUFFERED/ LATCHED CMOS STATIC RAM SUBSYSTEMS

IDT7M824 FAMILY

FEATURES:

- High-density 1024K-bit (128K x 8-bit) CMOS static RAM modules with registered/buffered/latched addresses and I/Os
- High-speed registered access time:
  - Military temperature range: 60ns (max.)
  - Commercial temperature range: 50ns (max.)
- 20MHz read cycle time
- Low power consumption (typ.)
  - Active: 1.5W
  - Standby: 75mW
- Low input capacitance (typ.): input 20pF; output 25pF
- High output drive (min.): I_{OL} = 48mW; I_{OH} = -15mA
- Available in 64-pin, 900 mil centre sidebraze DIP (with LCCs on both sides), achieving very high memory density
- Module select output
- Separate inputs and outputs
- Clear data and clock enables on all registers
- Address, input and outputs on separate clocks or latch enables
- Registered write enable
- Internal bypass capacitors for minimizing power supply noise
- TTL-compatible; single 5V (±10%) power supply
- Five GND pins for maximum noise immunity, five V_{CC} pins
- Military grade module available with semiconductor components compliant to the latest revision of MIL-STD-883, Class B

DESCRIPTION:

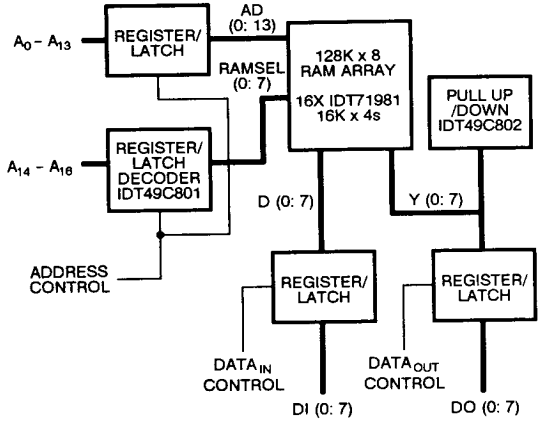
The IDT7M824 family is a set of 1024K-bit (128K x 8-bit) high-speed CMOS static RAM modules with registered/buffered/latched addresses and I/Os. They are constructed on co-fired, multi-layered ceramic substrates with sidebrazed leads using 16 IDT71981 (16K x 4) static RAMs, IDT logic devices and decoupling capacitors. Devices in leadless chip carriers are mounted top and bottom for maximum density.

Extremely high speeds are achievable by the use of IDT71981s and logic devices fabricated in IDT's high-performance, high-reliability CEMOS™ technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides the fastest circuits possible. The IDT7M824 has registered access times of 50ns (max.) over the commercial temperature range and can be operated with cycle times as fast as 20MHz.

Designing with this device can be very flexible because of such features as module select output and clock enables on all registers, registered write enable and 8-bit separate inputs and outputs. Because of the proprietary IDT49C801, the modules are cascadable in terms of depth with no additional external decoding. The write enable can be turned off when the module is deselected. Immunity to noise has been extended with such features as 8-bit separate inputs and outputs; addresses, inputs, and outputs on separate clocks; internal decoupling capacitors; five ground pins and five V_{CC} pins.

The semiconductor components used on all IDT military modules are manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT SELECTOR GUIDE

PART NO.	I/O AND ADDRESS FEATURES		
	ADDRESS BUS	INPUT DATA BUS	OUTPUT DATA BUS
IDT7M820	L/B	L/B	L/B
IDT7M821	L/B	R	R
IDT7M822	L/B	R	L/B
IDT7M823	L/B	L/B	R
IDT7M825	R	R	R
IDT7M826	R	R	L/B
IDT7M827	R	L/B	R
IDT7M828	R	L/B	L/B

NOTES:

1. L/B = LATCHED/BUFFERED
   R = REGISTERED
2. For module dimensions, please refer to module drawing M8 in the packaging section.

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PIN NAMES

NAME	DESCRIPTION
$A_0 - A_{16}$	Addresses
$DI_0 - DI_7$	Data input
$DO_0 - DO_7$	Data output
$\overline{CLRDIN}$	Data input clear
CPDIN/LEDIN	Data input register clock/latch enable
$\overline{ENDIN}/\overline{PREDIN}$	Data input register clock enable/latch preset
$\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$	Output enable
CPDOUT/LEDOUT	Data output register clock/latch enable
$\overline{ENDOUT}/\overline{PREDOUT}$	Data output register clock enable/latch preset
$\overline{CS}_1$, $\overline{CS}_2$, & CS_3	Chip select
$\overline{WE}$	Write enable
$\overline{SEL}$	Select output
LE/CP	Latch enable/clock pulse control input
$\overline{CE}$/GND	Clock enable/ground
REG/$\overline{LAT}$	Register/latch (low active) input control
V_{CC}	Power
GND	Ground

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	20	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	25	pF

NOTE:
1. This parameter is sampled and not 100% tested.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	120	120	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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DC ELECTRICAL CHARACTERISTICS

Following Conditions Apply Unless Otherwise Specified:
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% Min. = 4.50V Max. = 5.50V (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.[3]		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 32mA MIL.	–	–	0.4	
			I_{OL} = 48mA COM'L.	–	–	0.5	
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, V_{CC} = Max., Output Open, f = 0		–	300	600	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS}$ = V_{IL}, V_{CC} = Max., Output Open, f = f_{MAX}		–	320	650	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Output Open, f = f_{MAX}		–	15	330	mA

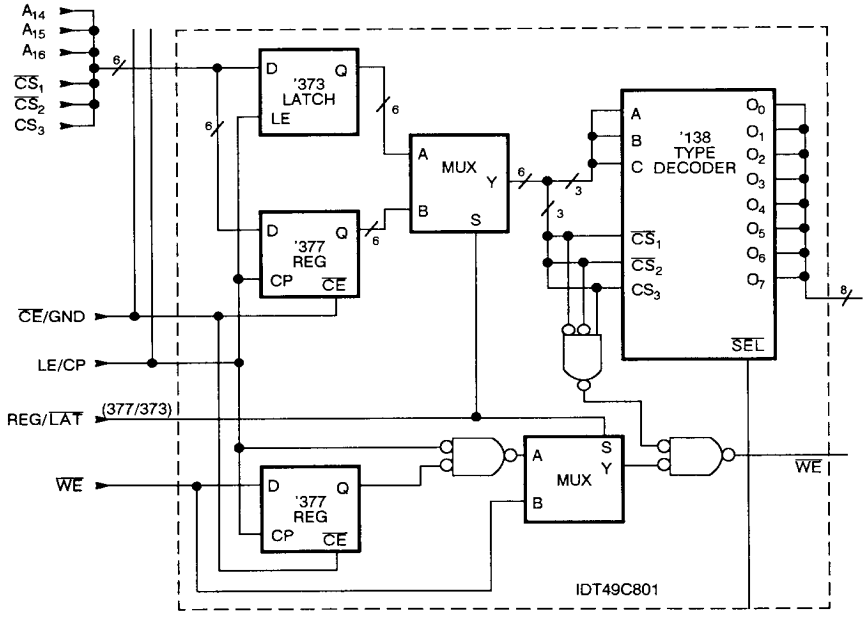
NOTES:
1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

IDT49C801

REGISTERED/LATCHED DECODER

The IDT49C801 is a proprietary IDT gate array that includes a 138-type 1-of-8 decoder, as well as latches and registers for all inputs and controls for WRITE ENABLE ($\overline{WE}$). The latch or register mode is controlled by a single input, REG/$\overline{LAT}$.

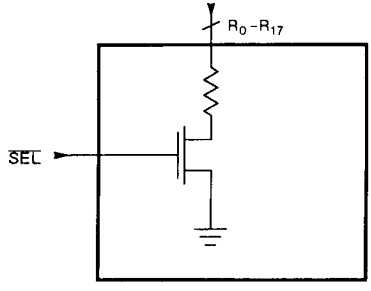
With the IDT49C801 in the Latch mode, the three address and the three chip select inputs are latched by a 373-type latch. When LE is high, the latch is transparent and, when LE goes low, all data that meets the required set-up time is latched. The $\overline{WE}$ input is not latched but it is gated by the result of the three chip select inputs. With the IDT49C801 in the Register mode, the three address and chip select inputs are registered by a 377-type register. All data that meets the set-up time requirements before the rising edge of CP will be transferred to the output of the register provided Clock Enable ($\overline{CE}$) is asserted. In this mode, $\overline{WE}$ is also registered but the output of its register is gated with CP so that when CP goes low, the output of $\overline{WE}$ is applied to the RAMs.



IDT49C802

UNIVERSAL PULL-UP/DOWN RESISTORS

The IDT49C802 is a proprietary gate array that has 18 selectable pull-up or pull-down resistors, only eight of which are used on these parts. The purpose of the pull-down resistor, as used in these parts, is to prevent the RAM DO pins from floating when the RAM array is deselected. When the RAM array is selected, the pull-down resistor is inhibited. The value of the resistors is approximately 15KΩ.



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