3033-1.3 November 1991

MCT83100 Series

MIL-STD-1553B STANAG 3838 REMOTE TERMINAL UNIT

(Supersedes H10401FUG all versions)

The MCT83100 series is a range of complete dual redundant MIL-STD-1553B (STANAG 3838) Remote Terminal Units with an easy to use processor interface. Each device comprises two low power transceivers, a monolithic Remote Terminal (RT) protocol device, a memory control device, and a 4K x 16 bit double buffered dual port RAM, all in a single co-fired ceramic package. Additionally four MSI devices buffer the Initialise Word and make available the 1553B Command Word.

The MCT83910 thru MCT83912 are identical to the MCT83100 series except that the four MSI devices are omitted. This makes available the internal highway (HD0-15) allowing STANAG 3910 Action and Status Words to be transferred. A number of control lines are also available to provide a means of interfacing to the internal highway.

FEATURES

- Single package device providing comprehensive remote terminal 1553B interface compatibility with most processing systems/devices
- Integral Transceivers
- Integral 4K x 16 Bit Fully Double Buffered Dual Port Static RAM Devices
- All MIL-STD-1553B Data Words are Memory Mapped, so providing a minimum of Software and Hardware overheads
- Separate Data Buffering for Broadcast Commands (in accordance with MIL-STD-1553B Notice 2)
- Contains full memory contention resolution and control
- Provides powerful built in test features initiated either by Host Subsystems or via the 1553B Data Highway
- Integral Illegal Command Monitoring
- Low Power Dissipation
- 90 Pin Quad In Line or Flat Pack Package 2.4 x 1.6 Inches (61 x 41mm)
- Can be configured to operate in either 16 Bit or 8 Bit Mode
- Operates over the full Military Temperature Range (-55°C to +125°C)

Device	Transceiver Voltages	RAM Options (k)
MCT83102	-15, +5	4
MCT83102-3	±15, +5	
MCT83103	-12, +5	4
MCT83103-3	±12, +5	
MCT83105	+5	4
MCT83910	-15, +5	4+3910 I/F
MCT83910-3	±15, +5	
MCT83911	-12, +5	4+3910 I/F
MCT83911-3	±12, +5	
MCT83912	+5	4+3910 I/F

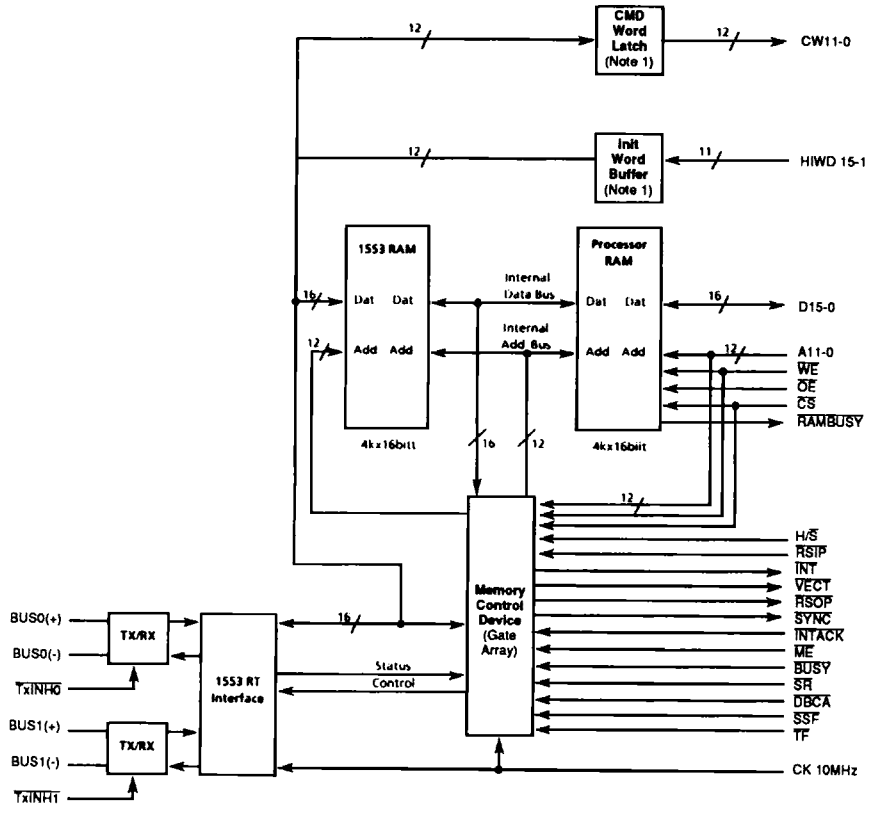
Notes:
1. Package size: 2.4"x1.6" (61mmx41mm)
2. RAM Access Time: 100ns
3. Refer to Customer Services for availability of MCT83102, 83103, 83910, 83911

Table 1: MCT83100 Series

GENERAL DESCRIPTION

Each of the MCT83100 series of devices provides an intelligent, fully double buffered interface between either a single or a dual redundant 1553B data bus and any 16-bit or 8-bit based CPU. The interface appears to a host CPU as a 4kx16-bit area of static RAM into which all 1553B transfers are memory mapped. A host CPU has access to the memory at all time. Only complete, valid messages will be presented to, or transmitted from the CPU.

All of the 1553B RT options are implemented by the MCT83100 series of devices. These along with a number of software and hardware programmable interface options provide a high degree of operational flexibility. A Message Error input is provided in order that any number of broadcast-T/R-subaddress-word count combinations may be declared illegal. The devices also allow a host CPU to make use of the 1553B reserved status bits and mode commands if required in specialist applications.



Notes:
1. See appendix A for details of MCT83910/1/2 operation.
2. Refer to factory for 2k RAM Versions.

Figure 1: MCT83102 Block Diagram

1. FUNCTION

Figure 1 is a block diagram of the MCT83102 (4k x 16-bit RAM version), the device can be seen to contain the following functions:-

1. Two 1553B transceivers.
2. A 1553B RT protocol device.
3. A 4k x 16-bit area of dual port RAM accessed by the host CPU referred to as the "Processor RAM".
4. A 4k x 16-bit area of dual port RAM accessed by the 1553B protocol device referred to as the "1553 RAM".
5. A gate array responsible for memory contention resolution and control.
6. Two output latches which contain the latest Command Word.
7. Two input buffers which buffer the devices Initialise Word.

Mil-Std-1553B Command and Data words are received by the transceivers and validated by the 1553 RT protocol device. The 1553 protocol device accesses the left hand side (LHS) of the "1553 RAM". The host CPU has access to the right hand side (RHS) of the "Processor RAM". The gate array performs data transfers between the RAMs.

After reception of a 1553 receive Command Word followed contiguously by receive data, the 1553 protcol device stores the data in the "1553 RAM". The data is memory mapped using the 1553 Command Word subaddress bits. Upon message validation the 1553 protocol device transmits a Status Word then instructs the gate array to transfer the data from the "1553 RAM" to the "Processor RAM". This transfer may be prevented by the host CPU writing the subaddress value of the data into location 405 (hex) - the Receive Access Control word (RACWd).

The 1553 protocol device will always store receive data in the "1553 RAM" irrespective of the RACWd contents. The gate array compares the RACWd value with the subaddress in the command word after message validation. If the RACWd value matches the subaddress then the "1553 RAM" to "Processor RAM" data transfers will be delayed until the RACWd contents are altered. If the RACWd value does not match the subaddress then the "1553 RAM" to "Processor RAM" data transfer takes place immediately.

In order to read a receive message, the host CPU merely writes the appropriate subaddress value of the data into the RACWd, then reads the data in ascending order, before clearing the RACWd to zero.

Transmit data is stored in the "Processor RAM" by the host CPU. Once the message is complete the host CPU instructs the gate array to transfer the message to the "1553 RAM". The transfer is initiated by the host CPU writing the expected transmit Command Word into either location 406 (hex) or location 407 (hex) - Transfer Control Words 0 and 1 (TCWd). When the 1553 protocol device decodes a transmit Command Word it transmits a Status Word followed by the required number of Data Words - which it reads from the "1553 RAM".

Upon completion of a "Processor RAM" to the "1553 RAM" data transfer the gate array clears the relevant TCWd. The host CPU must not write to a TCWd that has not been cleared. The "Processor RAM" to the "1553 RAM" data transfer may be delayed by up to 640µs if the 1553 protocol device is performing a transmit command using the same subaddress value as contained in the TCWd. Hence a second TCWd is provided.

In order to update a transmit message, the host CPU writes the transmit data into the "Processor RAM". When the message is complete the host CPU interrogates the TCWds in order to ascertain which is clear, before writing the expected transmit command word value into that TCWd.

It is intended that the host CPU views the 83100 interface merely as a block of RAM, hence all Command, Control, Status and Data Words are memory mapped within the 4k boundary. 4k RAM is provided in order that Data Words associated with broadcast commands may be stored independently of non-broadcast data. Figure 5 details the MCT83102 memory architecture.

A 12-bit latched Command Word output and a message error Status Word input are provided in order to allow Command Words to be illegalised with the minimum of external hardware. All 1553B defined illegal commands are automatically illegalised without the addition of external hardware. Four interrupt outputs and six 1553 Status Word inputs are provided should they be required. A further group of eleven inputs is also provided in order to allow the host CPU designer to hard-wire the Hybrid Initialise word.

2. SIGNAL DESCRIPTIONS

Pin	Name	Dir	Logic	Description
1	BUS1(+)	I/O	1553B	Positive threshold exceeded bus 1
2	BUS1(-)	I/O	1553B	Negative threshold exceeded bus 1
3	V_{EE}(1)	I/P	-	-15V/-12V supply to bus 1 transceiver (see note 3) (HIGH CURRENT)
4	V_{DD}(1)	I/P	-	+15V/+12V/+5V supply to bus 1 transceiver (see note 4) (HIGH CURRENT)
5	0V	I/P	-	0V return for all supplies
6	V_{CC}	I/P	-	+5V supply (see note 5)
7	TP1	O/P	-	Factory use only
8	TP2	O/P	-	Factory use only
9	$\overline{TXINHI}$	I/P	T2	Active low bus 1 transmitter inhibit (open circuit enables transmitter) (note 3)
10	H/$\overline{S}$	I/P	C2	Connecting this input to logic 0 will cause the HIWd to be defined by location 401 (hex) of the 1553B RAM. Leaving this input open circuit will cause the HIWd to be defined by the HI15-1 inputs.
11	10MHz	I/P	C3	10MHz clock input. Note: clock must have a mark/space ratio of 1:1±10%
12	$\overline{RSIP}$	I/P	C2	This input must be held to a logic 0 for 1.0µs after power up ie V_{CC} = 4.5V
13	$\overline{RSOP}$	O/P	C1	This output will pulse low for nominally 300ns after reception of a valid Reset RT mode command.
14	$\overline{VECT}$	O/P	C1	This output will pulse low for nominally 300ns after reception of a valid Transmit Vector Word mode command.
15	$\overline{SYNC}$	O/P	C1	This output will pulse low for nominally 300ns after reception of a valid Synchronise Without Data mode command and after reception of a valid Synchronise With Data mode command if bit 14 of the HCWd is set.
16	$\overline{INT}$	O/P	C1	Upon reception of a valid command (if the relevant HCWd bit is set) this output will go low until $\overline{INTACK}$ is taken to logic 0. If $\overline{INTACK}$ is connected directly to $\overline{INT}$ then $\overline{INT}$ will pulse low for nominally 300ns.
17	$\overline{INTACK}$	I/P	C2	Setting this input to a logic 0 will cause the $\overline{INT}$ output to return to a logic 1. Note: Minimum $\overline{INT}$ pulse width is nominally 300ns.
18	HI15	I/P	T2	RTAD4
19	HI14	I/P	T2	RTAD3
20	HI13	I/P	T2	RTAD2
21	HI12	I/P	T2	RTAD1
22	HI11	I/P	T2	RTAD0
23	HI10	I/P	T2	RTADPAR
24	HI9/8	I/P	2xT2	BCST
25	HI7	I/P	T2	$\overline{FLAGOP}$
26	HI3	I/P	T2	TM1
27	HI2	I/P	T2	TM0
28	HI1	I/P	T2	$\overline{ABR}$
				These inputs define the device's HIWd if the H/$\overline{S}$ input is open circuit or at logic 1. The HIWd is only loaded into the 1553 RT Interface device either on the low-to- high transition of the RTON bit in the HCWd or upon reception of a valid Reset RT mode command. The bit allocation of the HIWd is detailed in table 3
29	$\overline{RAMWEH}$	I/P	RA	Pulsing this input with $\overline{RAMCS}$ low will cause the most significant eight bits of the "Processor RAM" (D 15-8) to be written to. Note: The address will be defined by the A11-0 inputs.
30	$\overline{RAMWEL}$	I/P	RW	Pulsing this input low with $\overline{RAMCS}$ low will cause the least significant eight bits of the "Processor RAM" (D7-0) to be written to. Note: in 8 bit mode a pulse on this pin must precede a pulse on $\overline{RAMWEH}$.

Notes:
1. Logic types (RB, RD etc) are described in the Electrical Characteristics section.
2. A bar indicates an active low level signal.
3. Connection to this pin is not required on MCT83105 and MCT83912.
4. Refer to Table 1 for the connection of the appropriate voltage to this pin. For MCT83102, 83103, 83910,83911 this pin is open circuit.
5. Logic supply and with the exception of MCT83105 and MCT83912 it is also the +5V supply to the transceiver.

Table 2: Signal Descriptions

Pin	Name	Dir	Logic	Description
31	$\overline{\text{RAMOE}}$	I/P	RW	Setting this input low whilst $\overline{\text{RAMCS}}$ is low will allow the device's "Processor RAM" to be read.
32	$\overline{\text{RAMCS}}$	I/P	C2	Setting this input low will allow access to the "Processor RAM".
33	A11	I/P	RA	These inputs form the address bus of the "Processor RAM"
34	A10	I/P	RA	
35	A9	I/P	RA	
36	A8	I/P	RA	
37	A7	I/P	RA	
38	A6	I/P	RA	
39	A5	I/P	RA	
40	A4	I/P	RA	
41	A3	I/P	RA	
42	A2	I/P	RA	
43	A1	I/P	RA	
44	A0	I/P	RA	
45	0V	I/P	-	0V return for all supplies
46	CASE	I/P	-	Case connection
47	$\overline{\text{RAMBUSY}}$	O/P	RB	This output will go active low if both the host CPU and the gate array attempt to access the same location in the "Processor RAM". Note: The host CPU must not access the MCT83100 RAM whilst this output is active.
48	D15	I/O	RD	These 16 bi-directional lines form the data bus connections to the "Processor RAM".
49	D14	I/O	RD	
50	D13	I/O	RD	
51	D12	I/O	RD	
52	D11	I/O	RD	
53	D10	I/O	RD	
54	D9	I/O	RD	
55	D8	I/O	RD	
56	D7	I/O	RD	
57	D6	I/O	RD	
58	D5	I/O	RD	
59	D4	I/O	RD	
60	D3	I/O	RD	
61	D2	I/O	RD	
62	D1	I/O	RD	
63	D0	I/O	RD	

Notes:
1. Logic types (RB, RD etc) are described in the Electrical Characteristics section.
2. A bar indicates an active low level signal.
3. Connection to this pin is not required on MCT83105 and MCT83912.
4. Refer to Table 1 for the connection of the appropriate voltage to this pin. For MCT83102, 83103, 83910,83911 this pin is open circuit.
5. Logic supply and with the exception of MCT83105 and MCT83912 it is also the +5V supply to the transceiver.

Table 2: Signal Descriptions (continued)

Pin	Name	Dir	Logic	Description
64	CW11	O/P	T1	These 12 outputs hold the last valid Command Word received by the device. These lines are updated 2.5µs before the on-board 1553B Status Word latch is up dated prior to transmission. CW11 will be a logic 1 after reception of a broadcast command and a logic 0 after a non-broadcast command. Note: these outputs allow the host CPU to decode the Command Word and then set the 1553B Message Error bit by driving the $\overline{ME}$ input to logic 0, so illegalising the command .
65	CW10	O/P	T1	
66	CW9	O/P	T1	
67	CW8	O/P	T1	
68	CW7	O/P	T1	
69	CW6	O/P	T1	
70	CW5	O/P	T1	
71	CW4	O/P	T1	
72	CW3	O/P	T1	
73	CW2	O/P	T1	
74	CW1	O/P	T1	
75	CW0	O/P	T1	
76	$\overline{ME}$	I/P	C2	Setting this input to a logic 0 will cause the Message Error bit to be set in subsequent 1553B Status Word transmissions. Note: Data transfers will be prevented.
77	$\overline{SR}$	I/P	C2	Setting this input to a logic 0 will cause the Service Request bit to be set in subsequent 1553B Status Word transmissions
78	$\overline{BUSY}$	I/P	C2	Setting this input to a logic 0 will cause the Busy bit to be set in subsequent 1553B Status Word transmissions. Note: Data Transfers will be prevented.
79	$\overline{SSF}$	I/P	C2	Setting this input to a logic 0 will cause the Subsystem Flag bit to be set in subsequent 1553B Status Word transmissions.
80	$\overline{DBCA}$	I/P	C2	Setting this input to a logic 0 will cause the Dynamic Bus Control Accept bit to be set in response to Dynamic Bus Control mode commands.
81	$\overline{TF}$	I/P	C2	Setting this input to a logic 0 will cause the Terminal Flag bit to be set in subsequent 1553B Status Word transmissions.
82	$\overline{TXINH0}$	I/P	T2	Active low bus 0 transmitter inhibit. Open circuit enables transmitter) (Note 3).
83	TP4	O/P	-	Factory use only
84	TP3	O/P	-	Factory use only
85	V_{CC}	I/P	-	+5V supply (see note 5)
86	0V	I/P	-	0V return for all supplies
87	$V_{DD}(0)$	I/P	-	+15V/+12V/+5V supply to bus 0 transceiver. (See note 4) (HIGH CURRENT)
88	$V_{EE}(0)$	I/P	-	-15V/-12V supply to bus 0 transceiver. (See note 3) (HIGH CURRENT)
89	BUS0(-)	I/O	1553B	Negative threshold exceeded bus 0.
90	BUS0(+)	I/O	1553B	Positive threshold exceeded bus 0.

Notes:
1. Logic types (RB, RD etc) are described in the Electrical Characteristics section.
2. A bar indicates an active low level signal.
3. Connection to this pin is not required on MCT83105 and MCT83912.
4. Refer to Table 1 for the connection of the appropriate voltage to this pin. For MCT83102, 83103, 83910,83911 this pin is open circuit.
5. Logic supply and with the exception of MCT83105 and MCT83912 it is also the +5V supply to the transceiver.

Table 2: Signal Descriptions (continued)

3. RECOMMENDED OPERATING CONDITIONS

3.1 MCT83102, MCT83910 -15V Device

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	VEE	-14.25	-15.0	-15.75	V
	VCC	4.5	5.0	5.5	V
Supply Current - Standby mode, ie. less than 1% duty cycle (Note 1 applies)	IEE	-	1	3	mA
	ICC	-	237	540	mA
Supply Current transmitting at 1MHz into 35Ω load at point A of Fig.2 - 25% duty cycle (Note 2 applies)	IEE25	-	41	45	mA
Supply current transmitting at 1MHz into 35Ω load at point A of Fig.2 - 100% duty cycle (Note 2 applies)	IEE100	-	166	185	mA
Power dissipation of most critical device during continuous transmission (Note 3 applies)	PC	-	155	160	mW
Thermal Resistance of most critical device	θJC	-	-	60	°C/W
Operating Temperature Range (case)	TOP	-55	-	125	°C
Storage Temperature Range	TST	-65	-	150	°C
Power Dissipation at less than 1% duty cycle	P	-	1.19	2.97	W
Power Dissipation at 25% duty cycle	P25	-	1.38	3.17	W
Power Dissipation at 100% duty cycle	P100	-	1.96	4.20	W

Notes:
1. I_{CC} limits do not change with duty cycle
2. Decreases linearly to applicable 'standby' value at zero duty cycle
3. Decreases linearly to zero at zero duty cycle.

Table 3: Recommended Operating Conditions - MCT83102, MCT83910

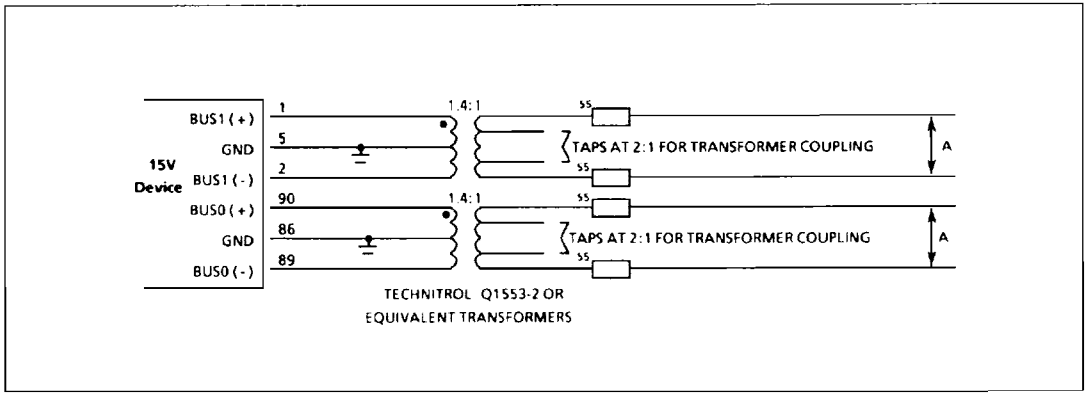


Figure 2: Bus Connections for 15V Devices

3.2 MCT83102-3, MCT83910-3 ±15V Devices

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	VDD	+14.25	+15.0	+15.75	V
	VEE	-14.25	-15.0	-15.75	V
	VCC	4.5	5.0	5.5	V
Supply Current - Standby mode, ie. less than 1% duty cycle (Note 1 applies)	IDD	-	30	44	mA
	IEE	-	50	70	mA
	ICC	-	237	540	mA
Supply Current transmitting at 1MHz into 35Ω load at point A of Fig.2 - 25% duty cycle (Note 2 applies)	IDD25	-	70	100	mA
Supply current transmitting at 1MHz into 35Ω load at point A of Fig.2- 100% duty cycle (Note 2 applies)	IDD100	-	200	260	mA
Power dissipation of most critical device during continuous transmission (Note 3 applies)	PC	-	350	500	mW
Thermal Resistance of most critical device	θJC	-	-	60	°C/W
Operating Temperature Range (case)	TOP	-55	-	125	°C
Storage Temperature Range	TST	-65	-	150	°C
Power Dissipation at less than 1% duty cycle	P	-	2.40	4.75	W
Power Dissipation at 25% duty cycle	P25	-	2.60	5.25	W
Power Dissipation at 100% duty cycle	P100	-	4.35	6.90	W

Notes:
1. I_{CC} and I_{EE} limits do not change with duty cycle
2. Decreases linearly to applicable 'standby' value at zero duty cycle
3. Decreases linearly to zero at zero duty cycle

Table 4: Recommended Operating Conditions - MCT83102-3, MCT83910-3

3.3 MCT83103, MCT83911 -12V Device

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	VEE	-11.4	-12.0	-12.6	V
	VCC	4.5	5.0	5.5	V
Supply Current - Standby mode, ie.less than 1% duty cycle (Note 1 applies)	IEE	-	1	3	mA
	ICC	-	237	540	mA
Supply Current transmitting at 1 MHz into 35Ω load at point A of Fig.3 - 25% duty cycle (Note 2 applies)	IEE25	-	64	68	mA
Supply Current transmitting at 1 MHz into 35Ω load at point A of Fig.3 - 100% duty cycle (Note 2 applies)	IEE100	-	231	254	mA
Power dissipation of most critical device during continuous transmission (Note 3 applies)	PC	-	230	250	mW
Thermal Resistance of most critical device	θJC	-	-	60	°C/W
Operating Temperature Range(case)	TOP	-55	-	125	°C
Storage Temperature Range	TST	-65	-	150	°C
Power Dissipation at less than 1% duty cycle	P	-	1.19	2.97	W
Power Dissipation at 25% duty cycle	P25	-	1.56	3 23	W
Power Dissipation at 100% duty cycle	P100	-	2.24	4.6	W

Notes:
1. I_{CC} limits do not change with duty cycle
2. Decreases linearly to applicable 'standby' value at zero duty cycle
3. Decreases linearly to zero at zero duty cycle

Table 5: Recommended Operating Conditions - MCT83103, MCT83911

3.4 MCT83103-3, MCT83911-3 ±12V Devices

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Power Supply Voltages	VDD	+11.4	+12.0	+12.6	V
	VEE	-11.4	-12.0	-12.6	V
	VCC	4.5	5.0	5.5	V
Supply Current - Standby mode, ie. less than 1% duty cycle (Note 1 applies)	IDD	-	30	44	mA
	IEE	-	50	70	mA
	ICC	-	237	540	mA
Supply Current transmitting at 1 MHz into 35Ω load at point A of Fig.3 - 25% duty cycle (Note 2 applies)	IDD25	-	85	120	mA
Supply Current transmitting at 1 MHz into 35Ω load at point A of Fig.3 - 100% duty cycle (Note 2 applies)	IDD100	-	240	315	mA
Power dissipation of most critical device during continuous transmission (Note 3 applies)	PC	-	350	500	mW
Thermal Resistance of most critical device	θJC	-	-	60	°C/W
Operating Temperature Range(case)	TOP	-55	-	125	°C
Storage Temperature Range	TST	-65	-	150	°C
Power Dissipation at less than 1% duty cycle	P	-	2.15	4.40	W
Power Dissipation at 25% duty cycle	P25	-	2.40	4.90	W
Power Dissipation at100% duty cycle	P100	-	3.06	7.20	W

Notes:
1. I_{CC} and I_{EE} limits do not change with duty cycle or mode of operation
2. Decreases linearly to applicable 'standby' value at zero duty cycle
3. Decreases linearly to zero at zero duty cycle

Table 6: Recommended Operating Conditions - MCT83103-3, MCT83911-3

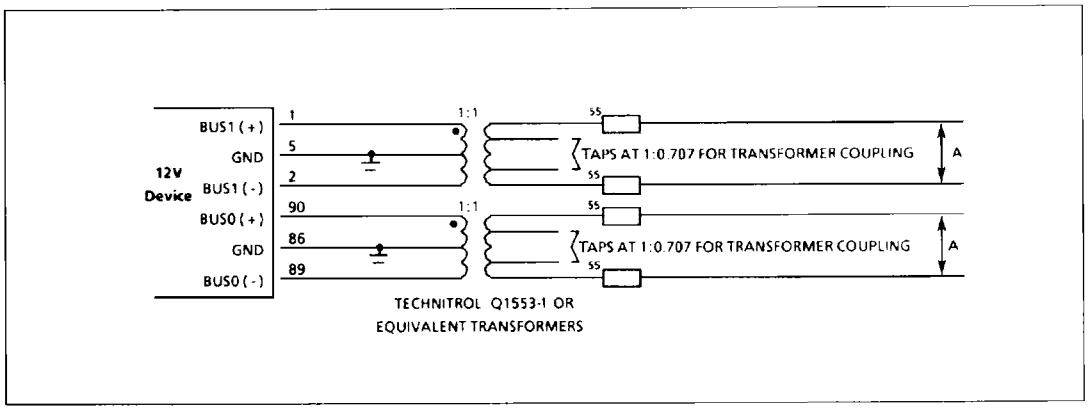


Figure 3: Bus Connections for 12V Devices

3.5 MCT83105, MCT83912 +5V Devices

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Power supply voltages	VDD	4.5	5 0	5 5	V
	VCC	4.5	5.0	5.5	V
Supply Current - Standby mode(ie. less than 1% duty cycle (Note 1 applies)	IDD	-	100	150	mA
	ICC	-	137	390	mA
Supply Current transmitting at 1 MHz into 35Ω load at point A of Fig.4 - 25% duty cycle (Note 2 applies)	IDD25	-	230	293	mA
Supply Current transmitting at 1MHz into 35Ω load at point A of Fig.4 - 100% duty cycle (Note2 applies)	IDD100	-	620	720	mA
Power dissipation of most critical device during continuous transmission (Note 3 applies)	PC	-	260	320	mW
Thermal Resistance of most critical device	θJC	-	-	60	°C/W
Operating Temperature Range(case)	TOP	-55	-	125	°C
Storage Temperature Range	TST	-65	-	150	°C
Power Dissipation at less than 1%duty cycle	P	-	1.19	2.97	W
Power Dissipation at 25% duty cycle	P25	-	1.45	3.28	W
Power Dissipation at 100% duty cycle	P100	-	2.24	4.50	W

Notes
1. I_{CC} limits do not change with duty cycle
2. Decreases linearly to applicable 'standby' value at zero duty cycle
3. Decreases linearly to zero at zero duty cycle

Table 7: Recommended Operating Conditions - MCT83105, MCT83912

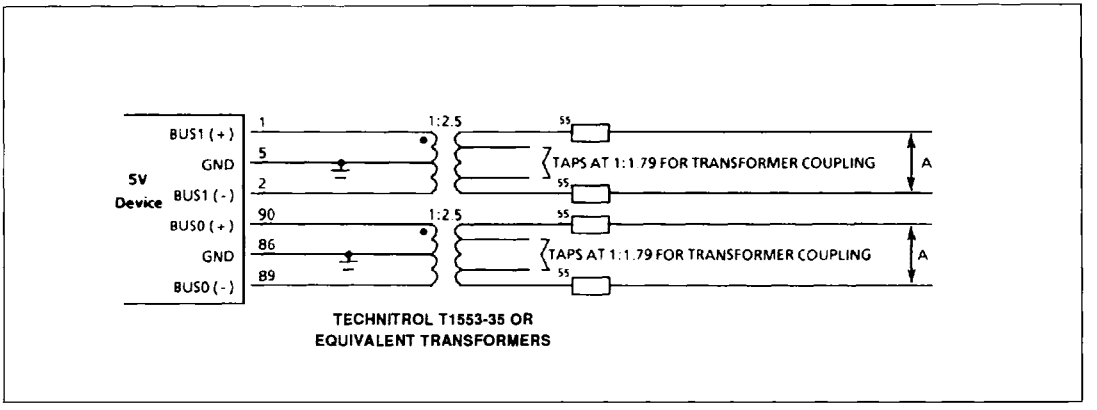


Figure 4: Bus Connections for +5V Device

GUIDELINES FOR USE

A) Decoupling

Decouple V_{DD} to ground close to the hybrid.
A parallel capacitor combination of a 100nF ceramic and a 10μF (or greater) tantalum is recommended.
Note: The peak transmission current drawn from V_{DD} is of the order of 650mA.

B) Board Layout

- Full PCB ground-planing is recommended.
- The connections between the Bus lines and the transformer should be balanced in terms of length, shape and area, and designed to:
  (i) Withstand peak transmission current at worst case operational duty cycle.
  (ii) Minimise added series inductance.
  (iii) Ensure that the input impedance of the hybrid with its associated transformer does not fall below the minimum requirements of MIL-STD-1553B.

4. ABSOLUTE MAXIMUM RATINGS

Parameter	Device	Limits
Power Supply Voltage (V_{EE})	All except MCT83105 MCT83912	+0.3V to -18V
Power Supply Voltage (V_{CC})	All	-0.3V to +7V
Power Supply Voltage (V_{DD})	MCT83102-3 MCT83103-3 MCT83910-3 MCT83911-3	-0.3V to +18V
	MCT83105 MCT83912	-0.3V to +7V
Receiver Differential Input Pin 1 or Pin 2, and Pin 90 or Pin 89	All	±20V (40V p-p)
Receiver Input Voltage Pin 1 or Pin 2, and Pin 90 or Pin 89	All	±15V
Logic Input Voltages	All	-0.3V to +5.5V
Transmitter Output Peak Current Pin 1 to Pin 2, and Pin 90 to Pin 89	MCT83102 MCT83102-3 MCT83910 MCT83910-3	200mA
	MCT83103 MCT83103-3 MCT83911 MCT83911-3	300mA
	MCT83105 MCT83912	800mA
Transmission Duty Cycle at T_{CASE} = 125°C	All	100%
Operating Case Temperature Range (T_{OP})	All	-55°C to +125°C
Storage Temperature Range (T_{ST})	All	-65°C to +150°C

Table 8: Absolute Maximum Ratings

5. ELECTRICAL CHARACTERISTICS

Note: All max/min values are for worst case operating conditions, where appropriate. at -55°C to +125°C

Label	Description	Min	Typ	Max	Unit
VOH	Output High Level Voltage(IOH=-1μA)	4.0	-	-	V
VOL	Output Low Level Voltage (IOL = 4mA)	-	-	0.4	V

Table 9a: Output Type - C1

Label	Description	Min	Typ	Max	Unit
VOH	Output High Level Voltage(IOH= -20μA)	4.0	-	-	V
VOL	Output Low Level Voltage(IOL = 4mA)	-	-	0.4	V

Table 9b: Output Type - T1

Label	Description	Min	Typ	Max	Unit
VOH	Output High Level Voltage (IOH = -4mA)	2.4	-	-	V
VOL	Output Low Level Voltage (IOL = 4mA)	-	-	0.5	V

Table 9c:0utput Type - RB

Label	Description	Min	Typ	Max	Unit
VOH	Output High Level Voltage (IOH = -4mA)	2.4	-	-	V
VOL	Output Low Level Voltage (IOL = 4mA)	-	-	0.5	V
VIH	Input High Level Voltage	2.2	-	-	V
VIL	Input Low Level Voltage	-	-	0.7	V
ILI	Input Leakage Current	-	-	30.0	μA
ILO	Output Leakage Current	-	-	30.0	μA

Table 9d: Input/Output - *RD*

Label	Description	Min	Typ	Max	Unit
VIH	Input High Level Voltage	2.0	-	VCC	V
VIL	Input Low Level Voltage	-	-	0.7	V
IIH	Input High Level Current	-	-	-20	μA
IIL	Input Low Level Current	-	-	200	μA

Table 9e: Input Type - C2 (CMOS I/P with 50kΩ pull up)

Label	Description	Min	Typ	Max	Unit
VIH	Input High Level Voltage	2.0	-	VCC	V
VIL	Input Low Level Voltage	-	-	0.7	V
IIH	Input High Level Current	-	-	100	μA
IIL	Input Low Level Current	-	-	1.5	mA

Table 9f: Input Type - T2 (CTTL I/P with 10KΩ)

Label	Description	min	Typ	max	unit
VIH	Input High Level Voltage	2.0	-	VCC	V
VIL	Input Low Level Voltage	-	-	0.7	V
ILI	Input Leakage Current	-	-	20	µA

Table 9g: Input Type - C3

Label	Description	Min	Typ	Max	Unit
VIH	Input High Level Voltage	2.0	-	VCC	V
VIL	Input Low Level Voltage	-	-	0.7	V
ILI	Input Leakage Current	-	-	60	µA

Table 9h: Input Type - RA

Label	Description	min	Typ	max	unit
VIH	Input High Level Voltage	2.0	-	VCC	V
VIL	Input Low Level voltage	-	-	0.7	V
ILI	Input Leakage Current	-	-	40	µA

Table 9i: Input Type - RW

Parameter/Condition		Symbol	Min	Typ	Max	Unit
Differential input impedance DC to 1 MHz (Transmitter Inhibited)		Zin	2K	-	-	Ω
Input differential voltage range		Vidr	±20	-	-	Vpeak
Input common mode voltage range up to 2MHz (line to ground)		Vicr	±10	-	-	Vpeak
Common mode rejection ratio		CMRR	40	-	-	dB
Threshold characteristics - sinewave at 1MHz		Vth1	0.75	1.0	1.2	Vp-p
Filter characteristics	2MHz	Vth2	1.5	-	8.0	Vp-p
	3MHz	Vth3	5	-	-	Vp-p
Differential output noise		Vnoi	-	-	10	mVp-p
Differential output level (e.g. at point A of Fig.2)		Vo	6	-	9	Vp-p
Rise and fall times (10-90%)		Tr	100	160	300	ns
Output Offset at 2.5µs after mid-bit crossing of the parity bit of the last word of a 660µs message (e.g. at point A of Fig.2)		Vos	-	±20	±75	mVpk

Table 9j: Transceiver Characteristics - For Direct Coupled Operation

6. MEMORY ARCHITECTURE

The memory can be divided into eight distinct areas:-

1. Command Word Stack.
2. Receive Data Buffer.
3. Receive Mode Data Buffer.
4. Control and Status Area.
5. Transmit Data Buffers.
6. Transmit Mode Data Buffers.
7. Broadcast Receive Data Buffer.
8. Broadcast Mode Receive Data Buffer.

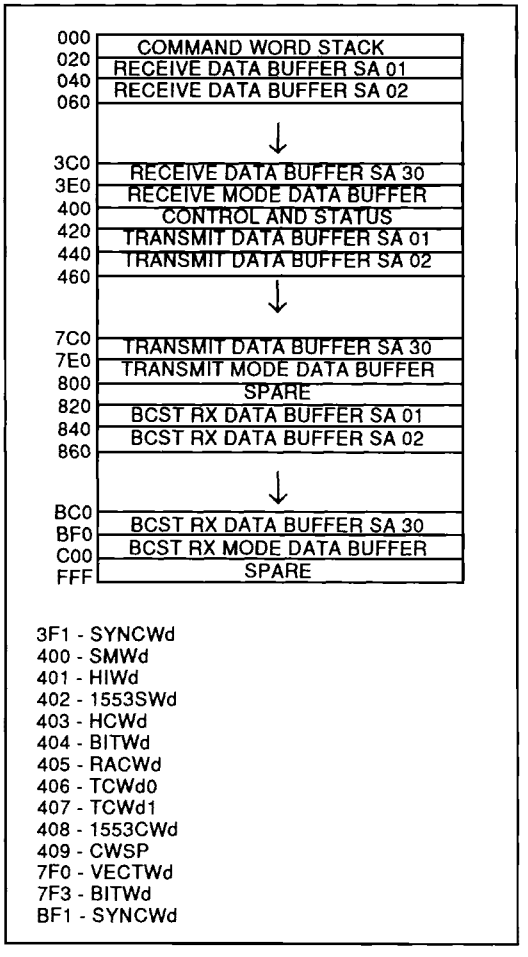


Figure 5: Memory Architecture

6.1 Command Word Stack

Locations 000 - 01F(hex) form the 32 word Command Word Stack. The device will store every valid, legal, logical command (except Transmit Status Word and Transmit Last Command Word mode commands) received in this circular stack. The bit allocation of the words on the Command Word Stack is listed on Table 10.

Bit	Name	Description
0	WC0	Word Count bit 0
1	WC1	Word Count bit 1
2	WC2	Word Count bit 2
3	WC3	Word Count bit 3
4	WC4	Word Count bit 4
5	SA0	Subaddress 0
6	SA1	Subaddress 1
7	SA2	Subaddress 2
8	SA3	Subaddress 3
9	SA4	Subaddress 4
10	T/$\overline{R}$	Transmit/Receive bit
11	BCST	Broadcast Command Detected - Logic 1 indicates reception of a Broadcast command
12	ZERO	Logic 0
13	ZERO	Logic 0
14	ZERO	Logic 0
15	NEWCMD	New Stack Command Word - This bit may be cleared by the host CPU after servicing the command

Table 10: Stack Command Word

6.2 Receive Data Buffers

Locations 020 - 3DF (hex) form the 30 Receive Data Buffers. Each buffer consists of 32 sixteen bit words and is allocated to each of the receive subaddress values excluding 00 and 1F (hex). Upon validation of a non-mode receive command and message the device will store the Data Words in the Receive Data Buffer indicated by the subaddress bits in the Command Word. The host CPU is able to delay this storing process by writing the appropriate subaddress value into the Receive Access Control Word (RACWd) in the Control and Status Area.

6.3 Receive Mode Data Buffer

Locations 3E0 - 3FF (hex) form the Receive Mode Data Buffer. This buffer is used to store the Data Words associated with receive mode commands irrespective of the subaddress bits being set to 00 or 1F (hex) e.g. Location 3F1 (hex) will contain the Data Word associated with a Synchronise with Data Word mode command.

6.4 Transmit Data Buffers

Locations 420-7DF (hex) form the Transmit Data Buffers. Each of these 30 buffers contains 32 sixteen bit words. As in the Receive Data Buffers each buffer is allocated a subaddress value. After the host CPU writes to either of the Transfer Control Words (TCWds) the gate array will transfer the indicated number of data words from the appropriate Transmit Data Buffer in the "Processor RAM" to the "1553 RAM". Upon reception of a non-mode transmit command the device will transmit the Data Words stored in the buffer indicated by the Command Word subaddress value.

6.5 Transmit Mode Data Buffers

Locations 7E0-7FF (hex) form the Transmit Mode Data Buffers. This buffer is used to store the Data Words associated with Transmit Mode Commands eg: Location 7F0 (hex) contains the 1553B Vector Word Location 7F3 (hex) contains the BITWd set up by the host CPU if bit 1 of the HIWd is set.

Note: Use of a TCWd is required to transfer these words from the "Processor RAM" to the "1553 RAM".

6.6 Broadcast Receive Data Buffer

Locations 820-BFF (hex) form the Broadcast Receive Data Buffers. These data buffers are used to store the Data Words associated with broadcast receive commands. As in the Receive Data Buffers each buffer is allocated a subaddress value.

6.7 Broadcast Receive Mode Data Buffer

Locations BE0-BFF (hex) form the Broadcast Receive Mode Data Buffers. This buffer is used to store the Data Words associated with broadcast mode receive commands irrespective of the subaddress bits being set to 00 or 1F (hex) eg: Location BF1 (hex) will contain the Data Word associated with a broadcast Synchronise with Data Word mode command.

6.8 Control and Status Area

Locations 400 - 41F form the Control and Status area. This area consists of ten words associated with the host CPU's monitoring and control of the device's operation.

6.8.1 Status Modifier Word

The Status Modifier Word (SMWd) is located at address 400 (hex), it allows the host CPU a high degree of control over the 1553B Status Word bits. In order to alter the state of the 1553B Status Word this word must be set to the appropriate, value then 0400 (hex) must be written into either of the Transfer Control Words. The bit allocation of the Status Modifier Word is listed in Table 11.

The 1553B Status Word Bits are set as a result of a logical 'OR' of the Status Modifier Word bits and the hardware status inputs (pins 76, 77, 78, 79, 80, 81).

In order to set a 1553B Status Word bit (eg Service Request) either set pin 77 to logic zero or write BFFF (hex) into address 400 (hex) then write 0400 (hex) into either of the Transfer Control Words.

Bit	Name	Description
0	Not Used	Set to one
1	Not Used	Set to one
2	Not Used	Set to one
3	$\overline{\text{ALLOW}}$	Allows reserved mode commands to be declared legal.
4	$\overline{\text{SETINST}}$	Sets the Instrumentation bit of the 1553B Status Word
5	$\overline{\text{SETRES5}}$	Sets bit 5 ot the 1553B Status Word
6	$\overline{\text{SETRES6}}$	Sets bit 6 ot the 1553B Status Word
7	$\overline{\text{SETRES7}}$	Sets bit 7 ot the 1553B Status Word
8	$\overline{\text{SETDBCA}}$	Sets the Dynamic Bus Control Accept bit in the 1553B Status Word transmitted in response to Dynamic Bus Control mode command
9	$\overline{\text{INHTF}}$	Inhibits the Terminal Flag bit in the 1553B Status Word from being set.
10	$\overline{\text{INHSSF}}$	Inhibits the Subsystem Flag bit in the 1553B Status Word from being set.
11	$\overline{\text{SETTF}}$	Sets the Terminal Flag bit in the 1553B Status Word
12	$\overline{\text{SETSSF}}$	Sets the Subsystem Flag bit in the 1553B Staus Word
13	$\overline{\text{SETBUSY}}$	Sets the Busy bit in the 1553B Status Word
14	$\overline{\text{SETSERV}}$	Sets the Service Request bit in the 1553B Status Word
15	$\overline{\text{SETME}}$	Sets the Message Error bit in the 1553B Staus Word

Note: All of the SMWd bits are active low.

Table 11: Status Modifier Word

6.8.2 Hybrid Initialise Word

The Hybrid Initialise Word (HIWd) is located at address 401 (hex), it allows the host CPU to configure the device for a particular application. An option to make this word 'hard-wired' is selectable by leaving the H/$\overline{S}$ input open circuit. In order to alter the state of the device Initialise Word the following sequence must be performed: -

1. Set RTON bit in Hybrid Control Word to zero
2. Write 0403 into address 406/407
3. Set Hybrid Initialise Word to appropriate value
4. Write 0401 into address 406/407
5. Set RTON bit in Hybrid Control Word to one
6. Write 0403 into address 406/407

Notes:

1. All addresses and data in hex.
2. If H/$\overline{S}$ input is open circuit then 4. can be omitted.
3. It is recommended that H/$\overline{S}$ be left open circuit and only the 'hard-wired' HIWd be used.
4. The bit allocation of the Hybrid Initialise Word is listed in Table 12.

Bit	Name	Description
0	Logic One	Set to one
1	$\overline{ABR}$	When low selects contents of 7F3 (hex) as Data Word Associated with Transmit Bit Word mode commands
2	$\overline{TM0}$	Timeout multiplier bit 0 (see note 1)
3	$\overline{TM1}$	Timeout multiplier bit 1 (see note 1)
4	Logic One	Set to one
5	Logic One	Set to one
6	Logic One	Set to one
7	$\overline{FLAGOP}$	Subsystem and Terminal Flag setting option (see note 2)
8	BCSTEN0	When high enables the broadcast address on bus 0
9	BCSTEN1	When high enables the broadcast address on bus 1
10	RTADPAR	Remote Terminal address parity bit (see note 3)
11	RTAD0	Remote Terminal address bit 0
12	RTAD1	Remote Terminal address bit 1
13	RTAD2	Remote Terminal address bit 2
14	RTAD3	Remote Terminal address bit 3
15	RTAD4	Remote Terminal address bit 4

Notes:

1.

$\overline{TM1}$	$\overline{TM0}$	No Response Timeout (μs)
1	1	14
1	0	31
0	1	47
0	0	64

2. $\overline{FLAGOP}$ =1 if the TF or SSF bit is set, it will remain set until some positive action is taken to clear the setting condition, ie, mode command to reset or local resetting.

   $\overline{FLAGOP}$=0 if the TF or SSF bit is set, it will remain set until one status word has been transmitted with the bit set. The TF or SSF will then reset unless the fault condition is still present (ie, $\overline{SETTF}$ or $\overline{SETSSF}$ in the SMWd are still active or pins 79 or 81 still at logic 0).

3. RTADPAR. This pin must be set to a state such that bits 10-15 inclusive have an odd number of bits set to logic 1, ie, an odd parity.

Table 12: Hybrid Initialise Word

6.8.3 1553B Status Word

Location 402 (hex) contains a copy of the 1553B Status Word associated with the last Command Word received by the device.

Bit	Name		Description
0	TERMINALFLAG	Set by one of the following	Driving pin 81 to logic 0
			SMWd bit 9 high and SMWd bit 11 low
			1553 Protocol device(see note 1)
		Reset by one of the following	Status word transmission if HIWd bit 7 low and Driving pin 81 to logic 1
			Status word transmission if HIWd bit 7 low and SMWd bit 11 high
			Reset RT mode command and Driving pin 81 to logic 1
			Reset RT mode command and SMWd bit 11 high
			HCWd bit 0 low
1	Dynamic Bus Control Accept	Set by one of the following	Driving pin 80 to logic 0 and Reception of a valid DBCA mode command
			SMWd bit 8 low and Reception of a valid DBC A mode command
		Reset by one of the following	Driving pin 80 to logic 1 and Reception of any valid command except mode commands 02 or 12 (hex).
			SMWd bit 8 high and Reception of any valid command except mode commands 02 or 12 (hex).
			Reception of any valid command except mode commands 00 or 02 or 12 (hex)
			HCWd bit 0 low
2	Subsystem Flag	Set by one of the following	Driving pin 79 to logic 0
			SMWd bit 9 high and SMWd bit 11 low
		Reset by one of the following	Status word transmission if HIWd bit 7 low and Driving pin 79 to logic 1
			Status word transmission if HIWd bit 7 low and SMWd bit 12 high
			Reset RT mode command and Driving pin 79 to logic 1
			Reset RT mode command and SMWd bit 12 high
			HCWd bit 0 low
3	BUSY	Set by one of the following	Driving pin 78 to logic 0 SMWd bit 13 low
		Reset by of the following	Driving pin 78 to logic 1 SMWd bit 13 high HCWd bit 0 low
4	BROADCAST COMMAND REC'VD	Set by	1553 Protocol device (see note 2)
		Reset by	Reception of any valid command except mode commands 02 or 12 (hex)
5	RESERVED	Set by	SMWd bit 5 low
		Reset by of the following	SMWd bit 5 high HCWd bit 0 low
6	RESERVED	Set by	SMWd bit 6 low
		Reset by of the following	SMWd bit 6 high HCWd bit 0 low
7	RESERVED	Set by	SMWd bit 7 low
		Reset by one of the following	SMWd bit 7 high HCWd bit 0 low

Table 13: 1553B Status Word

Bit	Name	Description	
8	SERVICE REQUEST	Set by one of the following	Driving pin 77 to logic 0
			SMWd bit 14 low
		Reset by one of the following	Driving pin 77 to logic 1
			SMWd bit 14 high
			HCWd bit 0 low
9	INSTRUMENTATION	Set by	SMWd bit 4 low
		Reset by one of the following	SMWd bit 4 high
			HCWd bit 0 low
10	MESSAGE ERROR	Set by one of the following	Driving pin 76 to logic 0
			SMWd bit 15 low
			1553 Protocol device (see note 3)
		Reset by one of the following	Driving pin 76 to logic 1 and Reception of any valid command except mode commands 02 or 12 (hex).
			SMWd bit 15 high and Reception of any valid command except mode commands 02 or 12 (hex).
			HCWd bit 0 low
11-15	REMOTE TERMINAL ADDRESS BITS 0 - 4	These bits will be set to the RT Address value after reception of the first valid command after a low to high transition on HCWd bit 0	

Notes:

1: The Terminal Flag bit in the 83100 1553B Status Word is set by the 1553 protocol device under the following conditions:-
- i. If the 83100 fails to receive and validate a 1553B word that has transmitted: BIT Word bit 2 will also be set.
- ii. If the 83100 detects a failure in either of its transmission timeout circuits as a result of performing an Initialise Self Test mode command.
- iii. If either of the 83100 transmission timeout circuits goes active as a result of the device attempting to transmit for more than 800 microseconds.

2: The Broadcast Command Received bit in the 83100 1553B Status Word is set by 1553 protocol device upon reception of a valid Command Word that contains a RT Address of 1F (hex) under the following conditions:-
- i. Pin 14 was logic 0 and pin 10 was open-circuit at the time of the last low to high transition on HCWd bit 0.
- ii. HIWd bits 8 and 9 were low and pin 10 was logic 0 at the time of the last low to high transition on HCW bit 0.

3: The message error bit in the 83100 1553B Status Word is set by the 1553 protocol device if any of the following conditions occur on reception of a valid command word.
- i. Too few valid Data Words received after reception of a receive command: Status Word not transmitted and BITWd bit 5 is set.
- ii. An invalid data sync received during reception of the data portion of a message after reception of a receive command: Status Word not transmitted and BITWd bit 5 set.
- iii. An incorrect parity bit detected during reception of the data portion of a message after reception of a receive command: Status Word not transmitted and BITWd bit 5 is set.
- iv. A contiguity error detected during reception of the data portion of a message after reception of a receive command: Status Word not transmitted and BITWd bit 5 set.
- v. Too many Data Words received after reception of a receive command: Status Word not transmitted and BITWd bit 6 set.
- vi. Any word received after reception of a transmit command: Status Word not transmitted and BITWd bit 6 set.
- vii. Detection of an invalid RT-RT message format: Status Word not transmitted and either BITWd bit 5 or 6 set
- viii. Command Word decoded as illegal: Status Word transmitted and BITWd bit 4 is set.
- ix. Command Word decoded as illogical - eg broadcast transmit data command: Status Word not transmitted and BITWd bit 3 set.

Table 13: 1553B Status Word (continued)

6.8.4 Hybrid Control Word

The Hybrid Control Word (HCWd) is located at address 403 (hex). This word allows the processor further control over the operation of the device in areas such as interrupt generation and self test. In order to alter the state of the Hybrid Control Word location 403 (hex) must be updated with the appropriate value then 403 (hex) written into either of the Transfer Control Word locations. This word powers up in the all zero state. The bit allocation of the Hybrid Control Word is listed in Table 14.

Bit	Name	Description
0	RTON	When reset to zero this bit inhibits operation of the 1553B RT Interface device. The hybrid will still be capable of performing subsystem initiated self test as well as updating 1553B Transmit data buffers. This bit must be set to one in order to allow the hybrid to decode and respond to 1553B commands
1	WRAPENTX	Enables the device's subsystem initiated 'wrap around' self test feature
2	WRAPENRX	Enables the device's 1553B initiated 'wrap around' self test feature
3	INTENBIT	Enables the device's interrupt output after completion of either 'wrap around' self test
4	INTENRX	Enables device's interrupt output after completion of receive commands
5	INTENTX	Enables device's interrupt output after completion of transmit commands
6	INTENDBCA	Enables device's interrupt output after reception of Dynamic Bus Control mode commands
7	INTENSWO	Enables device's interrupt output after reception of Synchronise without Data Word mode commands
8	INTENST	Enables device's interrupt output after reception of Initiate Self Test mode commands
9	INTENRST	Enables device's interrupt output after reception of Reset Remote Terminal mode commands
10	INTENVW	Enables device's interrupt output after reception of Transmit Vector Word mode commands
11	INTENSWI	Enables device's interrupt output after reception of Synchronise with Data Word mode commands
12	INTENTBW	Enables device's interrupt output after reception of Transmit BIT Word mode command if bit 1 of the HIWd is set
13	INTENRSV	Enables device's interrupt output after reception of reserved mode commands
14	SYNCWIEN	Enables the device's SYNC output to go active after reception of Synchronise with Data Word mode commands
15	ZERO	Logic Zero

Table 14: Hybrid Control Word

6.8.5 Hybrid Built in Test Word

Location 404 (hex) will contain a copy of the current 1553 Interface device Built in Test Word (BITWd) which will be transmitted in response to a Transmit BIT Word mode command. This word is updated after every valid Command Word is received by the device, If bit 1 of HIWd is set then the BIT word contents will be taken from RAM location 7F3 (hex), the bit allocation is then defined by the host CPU, otherwise the bit allocation is as listed in Table 15. In either case location 404 (hex) will contain the 1553 Interface device BITWd.

Bit	Name	Description
0*	TIMEOUT	Transmitter timeout
1*	HSF	SS Handshake Failure
2	LTF	Loop test fail ie device detects error in its own transmission
3	TRW	T/R Wrong in mode command
4	IM	Illegal mode command
5	WCL	Word count low
6	WCH	Word count high
7	BTD	Broadcast transmit data
8*	SHUT0	Bus 0 is shutdown
9*	SHUT1	Bus 1 is shutdown
10*	SSFINH	Subsystem flag inhibited by the subsystem
11*	TFINF	Terminal flag inhibited by the subsystem
12	TIME0	Transmitter timeout on bus 0
13	TIME1	Transmitter timeout on bus 1
14*	BCSTINH0	Broadcast recognition inhibited (bus 0)
15*	BCSTINH1	Broadcast recognition inhibited (bus 1)

* These bits will continue to be set until appropriate action is taken to clear them ie Reset RT mode command or clear RTON bit in HCWd.

Table 15: Hybrid Built in Test Word

6.8.6 Receive Access Control Word

The Receive Access Control Word (RACWd) is located at address 405 (hex), By setting the bits of this word to a subaddress value, the host CPU is able to prevent the device from updating the Receive Data Buffer associated with that subaddress value. This word will be set to zero on power up, The bit allocation of this word is listed in Table 16.

Bit	Name	Description
0	Zero	Logic Zero
1	Zero	Logic Zero
2	Zero	Logic Zero
3	Zero	Logic Zero
4	Zero	Logic Zero
5	SA0	Subaddress bit 0
6	SA1	Subaddress bit 1
7	SA2	Subaddress bit 2
8	SA3	Subaddress bit 3
9	SA4	Subaddress bit 4
10	Zero	Logic Zero
11	BCST	Broadcast Data Buffer bit (Logic1 indicates broadcast area)
12	Zero	Logic Zero
13	Zero	Logic Zero
14	Zero	Logic Zero
15	Zero	Logic Zero

Note: No Transfer Control Word is required for the RACWd

Table 16: Receive Access Control Word

6.8.7 Transfer Control Words

The Transfer Control Words (TCWd0 and TCWd1) are located at address 406 (hex) 407 (hex) respectively. These words are used by the host CPU to instruct the gate array to transfer words stored in the 'Processor RAM' to the '1553B RAM'. The bit allocation of these words is listed in Table 17. These words can be used to transfer the following:-

1. Transmit data words: by outputing a TCWd containing the base address of a Transmit Data Buffer and the number of words it wishes transferred ie, T/R, Subaddress and Word Count of expected transmit command, the host CPU can instruct the gate array to update a Transmit Data Buffer.

Note: A Word Count of 00 will ensure the entire contents of the buffer are transmitted.

2. Miscellaneous Words: by writing a TCWd containing a subaddress value of either 00 or 1F (hex) and a T/R bit of one, the host CPU can instruct the on-chip controller to update the single word whose address is contained in the TCWd, eg:

TCWd = 0400 SMWd transferred

TCWd = 0401 HIWd transferred

TCWd = 0403 HCWd transferred

TCWd = 07F0 1553B Vector Word transferred

The host CPU must ensure that a TCWd is clear before writing to it. The gate array will clear the TCWd upon completion of the transfer and upon power up.

Bit	Name	Description
0	WC0	Word Count bit 0
1	WC1	Word Count bit 1
2	WC2	Word Count bit 2
3	WC3	Word Count bit 3
4	WC4	Word Count bit 4
5	SA0	Subaddress bit 0
6	SA1	Subaddress bit 1
7	SA2	Subaddress bit 2
8	SA3	Subaddress bit 3
9	SA4	Subaddress bit 4
10	T/$\overline{R}$	Transmit/Receive bit
11*	Zero	Remote Terminal Address bit 0
12*	Zero	Remote Terminal Address bit 1
13*	Zero	Remote Terminal Address bit 2
14*	Zero	Remote Terminal Address bit 3
15*	Zero	Remote Terminal Address bit 4

*Note: TCWd bits 11-15 are only used during self test.

Table 17: Transfer Control Word

6.8.8 Last 1553B Command Word

Location 408 (hex) contains the latest valid 1553B Command Word (with the exception of Transmit Last Command Word mode command) received by the device.

6.8.9 Command Word Stack Pointer

Location 409 (hex) contains the Command Word Stack Pointer (CWSP). This word will be the stack address of the latest Command Word Stack location to be updated by the device. This word will be reset to zero on power up.

7. POWER UP

On power up the MCT83100 requires the $\overline{RSIP}$ input be held low for at least 1.0µs after VCC reaches 4.5V. Upon this input going to a logic 1 the device will perform a reset routine which will result in:-

1. Command Word Stack Locations 000-01F set to 0000
2. RACWd set to 0000
3. TCWd0 and TCWd1 set to 0000
4. CWSP set to 0000

The reset routine results in reseting all of the 'status' information and disabling the devices from decoding and responding to 1553B Command Words. It is the responsibility of the host CPU to set up the following before setting the RTON bit in the HCWd:-

1. SMWd - if applicable - powers up random in the memory but in the gate array powers up to FFFF (hex)
2. HIWd - if applicable
3. Hybrid BITWd - if applicable
4. Transmit Data Buffers
5. Transmit Mode Data Buffers
6. HCWd - ie at minimum set RTON bit

Note: All of the above need to be transferred out of the "Processor RAM" using the Transfer Control Words.

8. INTERRUPTS

There are four interrupt signals that can be used by the host CPU as prompts regarding messages that have been received. Use of these signals is optional.

1. $\overline{SYNC}$ - This output will pulse low upon reception of valid Synchronise without Data mode commands unconditionally and valid Synchronise with Data mode commands if bit 14 of the HCWd has been set previously.
2. $\overline{RSOP}$ - This output will pulse low upon reception of valid Reset RT mode commands.
3. $\overline{VECT}$ - This output will pulse low upon reception of valid Transmit Vector Word mode commands.
4. $\overline{INT}$ - After reception of a valid command - if the relevant HCWd bit has been set previously - this output will go low until the input $\overline{INTACK}$ is taken low in response. If $\overline{INTACK}$ is connected to $\overline{INT}$ then this input will pulse low for nominally 300ns.

9. BUILT IN TEST

The device has four Built in Test (BIT) features:-

1. Upon reception of a valid Initiate Self Test mode command the device will test the 1553B transmission timeout circuit associated with the data bus on which the command was received. This test will take nominally 27.5µs after the Status Word is transmitted.
2. The device will monitor and validate every word it transmits on each of the 1553B data buses. If the device detects an error it will set the Terminal Flag bit and bit 2 in the BITWd
3. Whenever bit 1 of HCWd is set, the device will, upon reception of a new TCWd0 value:-

   a. Transfer the number of Data Words from the Transmit Data Buffer indicated by the TCWd in the "Processor RAM" to the equivalent Receive Data Buffer i n the "1553B RAM".

   b. Transfer the Data Words from the Receive Data Buffer in the "1553B RAM" to the equivalent Receive Data Buffer in the "Processor RAM".

   c. Write the TCWd into the next Command Word Stack location and increment the CWSP.

   d. Take the $\overline{INT}$ line active low if bit 4 of the HCWd is set.

      It is the responsibility of the host CPU to check that the data contained in the Receive and Transmit Data Buffers is identical in order to ascertain the success or failure of the BIT. A 32 word self test sequence will take nominally 50µs. Note: The RTON bit in the Hybrid Control Word must be zero during this type of self test.

4. Whenever bit 2 of the HCWd is set the device will upon reception of a receive command containing a subaddress value of 1E (hex):-

   a. Transfer the associated Data Words to the "Processor RAM" Receive Data Buffer 1E (hex).

   b. Transfer the contents of "Processor RAM" Receive Data Buffer 1E (hex) to Transmit Data Buffer 1E (hex) in the "1553 RAM".

   c. Write the Command Word into the next Command Word Stack location and increment the CWSP.

   d. Take the $\overline{INT}$ line active low if bit 3 of the HCWd is set.

   e. Update the HIWd, 1553SWd, BITWd and 1553CWd locations in the "Processor RAM".

10. MODE COMMANDS (RX DATA)

Upon reception of a valid receive mode command with an associated Data Word, the device will :-

1. Load the Command Word Latches with the received Command Word.
2. Store the associated Data Word in the Receive Mode Data Buffer in the "1553B RAM" area indicated by the mode code field of the received Command Word.
3. Modify the 1553B Status Word using the SMWd and the 6 hard wired lines, then Transmit its 1553B Status Word .
4. Transfer the mode Data Word into the equivalent location in the "Processor RAM".
5. Write the Command Word into the next Command Word Stack location and increment the CWSP.
6. Take the $\overline{INT}$ line active low if the relevant HCWd bit is set.
7. In the case of a Synchronise With Data Word mode command, also pulse the $\overline{SYNC}$ line active low if the bit 11 of the HCWd is set.
8. Update the HIWd, 1553SWd, BITWd and 1553CWd "Processor RAM" locations.

A typical Synchronise With Data mode command sequence is shown in Figure 6.

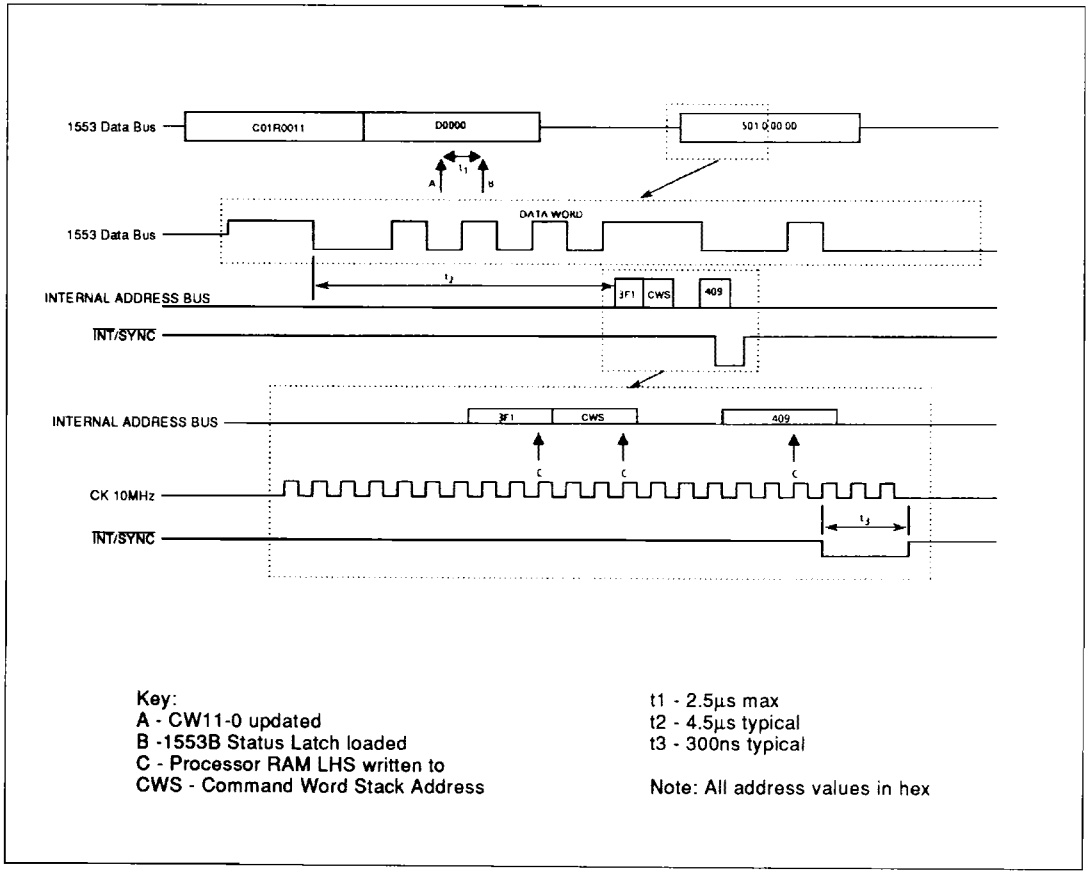


Figure 6: Synchronise with Data Word Mode Command

11. RECEIVE COMMANDS

Upon reception of a valid non-mode receive command, the device will:-

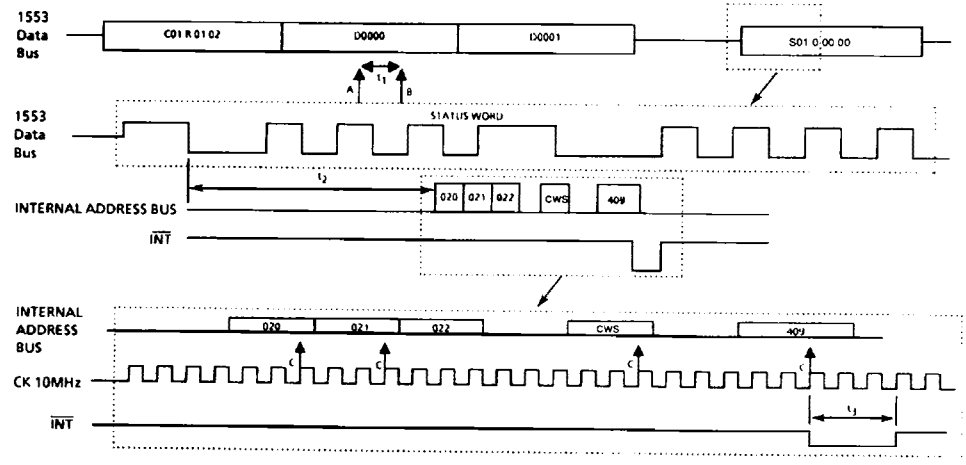
1. Load the Command Word Latches with the received Command Word.
2. Store the associated Data Words in the Receive Data Buffer in the "1553B RAM" area indicated by the subaddress value of the Command Word.
3. If the correct number of contiguous valid Data Words are received the device will modify the 1553B Status Word using SMWd and 6 hard wired status lines, transmit the 1553B Status Word, then inspect the RACWd .
4. If the subaddress value in the RACWd matches that of the Command Word the device will wait until the host CPU alters the contents of the RACWd before continuing, but will service any valid 1553B Command Words arriving in the meantime.
5. If the subaddress values do not match, the gate array will transfer the Data Words into the equivalent locations in the "Processor RAM".
6. Write the Command Word into the next Command Word Stack location and increment the CWSP.
7. Take the $\overline{INT}$ line active low if bit 4 of the HCWd is set.
8. Finally update the HIWd, 1553SWd, BITWd and 1553CWd locations in the "Processor RAM". Note: These locations may not always be updated if a further valid command is receivedwwith an inter-message gap less than 20µs after reception of a broadcast command.

Host CPU Actions:- Whenever the host CPU wants to read a Receive Data Buffer and wants to avoid reception of a 'part message' it must:-

1. Write the subaddress of the buffer into the RACWd. Note: No Transfer Control Word required for RACWd.
2. Wait for 600ns.
3. Read the Data Words out of the buffer in numerical order starting at the first location in the buffer.
4. Clear the RACWd on completion.

Error detection - if an error is detected in the incoming message the device will not transmit the 1553B Status Word, but the appropriate status word bits will be set and all further operations will be aborted, ie. the following RAM locations will not be updated, Command Word Stack and the CWSP. Also, the $\overline{INT}$ line will not go active and the invalid message will not be transferred into the "Processor RAM". However HIWd, 1553SWd, BITWd, 1553CWd will be updated as normal.

Figure 7 shows a 2 word receive command to subaddress 01. This figure identifies the gate array's accesses to the left hand side of the "Processor RAM". It can be seen that the first location in the Receive Data Buffer 020 (hex) is written, followed by location 021 (hex). Address 022 (hex) is then accessed without being written to. Finally one of the Command Word Stack locations is updated, the address of which is then written into location 409 (hex).



Key:
A - CW11-0 updated
B -1553B Status Latch loaded
C - Processor RAM LHS written to
CWS - Command Word Stack Address

t1 - 2.5µs max
t2 - 4.5µs typical
t3 - 300ns typical

Note: All address values in hex

Figure 7: Receive Command - 2 Words to Subaddress 01

12. TRANSMIT COMMANDS

Upon reception of a valid non-mode transmit command the device will:-

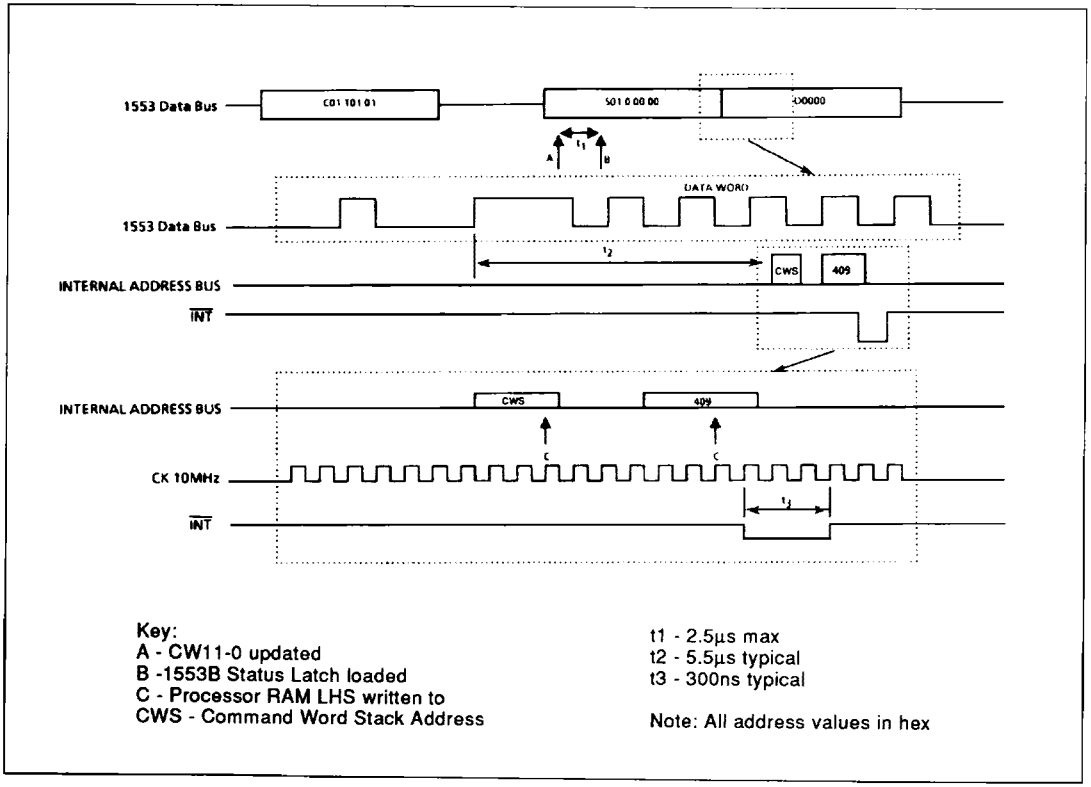
1. Load the Command Word Latches with the received Command Word.
2. Modify the 1553B Status Word using the SMWd and the 6 hard wired status lines, then transmit the 1553B Status Word.
3. Transmit the appropriate number of Data Words contained in the Transmit Data Buffer indicated by the Command Word Subaddress bits.
4. Write the Command Word into the next Command Word Stack location and increment the CWSP.
5. Take the $\overline{INT}$ line active low if bit 5 of the HCWd is set.
6. Update the HIWd, 1553SWd, BITWd and 1553CWd "Processor RAM" locations.

Host CPU Actions - Whenever a host CPU wishes to update a Transmit Data Buffer, it must:-

1. If the appropriate Transmit Data Buffer has been updated within the last 800µs - check that neither TCWd contains the appropriate subaddress value.
2. Write the Data Words into the appropriate Transmit Data Buffer.
3. Interrogate the TCWd locations in order to ascertain which is zero.
4. Write the appropriate subaddress value and word count into the TCWd containing zero. A word count of 00 will ensure that all of the 32 words in the buffer are transferred.

When the gate array detects the TCWd being updated, it will transfer the indicated number of Data Words to the indicated buffer in the "1553B RAM". This transfer may be delayed if that buffer is being accessed in order to service a Transmit Command. Upon completion of the data transfer the device will clear the relevant TCWd.

Figure 8 shows a one word transmit command to a subaddress 01. This figure identifies the gate array's accesses to the LHS of the "Processor RAM". It can be seen that one of the Command Word Stack locations is written to the address, which is then written into address 409 (hex).



Key:
A - CW11-0 updated
B -1553B Status Latch loaded
C - Processor RAM LHS written to
CWS - Command Word Stack Address

t1 - 2.5µs max
t2 - 5.5µs typical
t3 - 300ns typical

Note: All address values in hex

Figure 8: Transmit Command - 1 Word from Subaddress 01

13. MODE COMMANDS (NO DATA)

Upon reception of a valid mode command (no data) the device will:-

1. Load the Command Word Latches with the received Command Word.
2. Modify the 1553B Status Word using the SMWd and the 6 hard wired status lines, then transmit the 1553B Status Word.
3. Write the Command Word into the next Command Word Stack location and increment the CWSP.
4. Take the $\overline{INT}$ line active low if the relevant HCWd bit is set.
5. In the case of Reset RT mode command also pulse the $\overline{RSOP}$ line active low.
6. In the case of Synchronise Without Data mode command also pulse the $\overline{SYNC}$ line active low.
7. Update the HIWd, 1553SWd, BITWd and 1553CWd "Processor RAM" locations.

Typical Synchronise Without Data and Reset RT mode command sequences are shown in Figures 9 and 10 respectively.

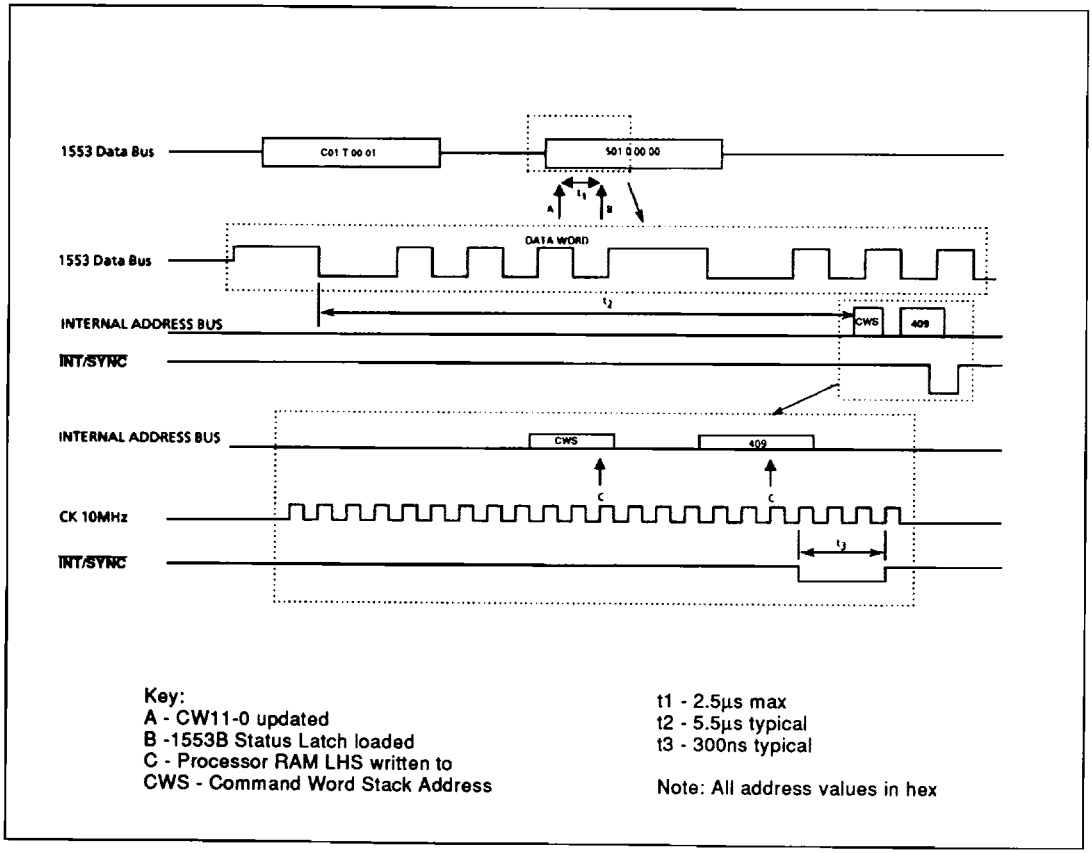
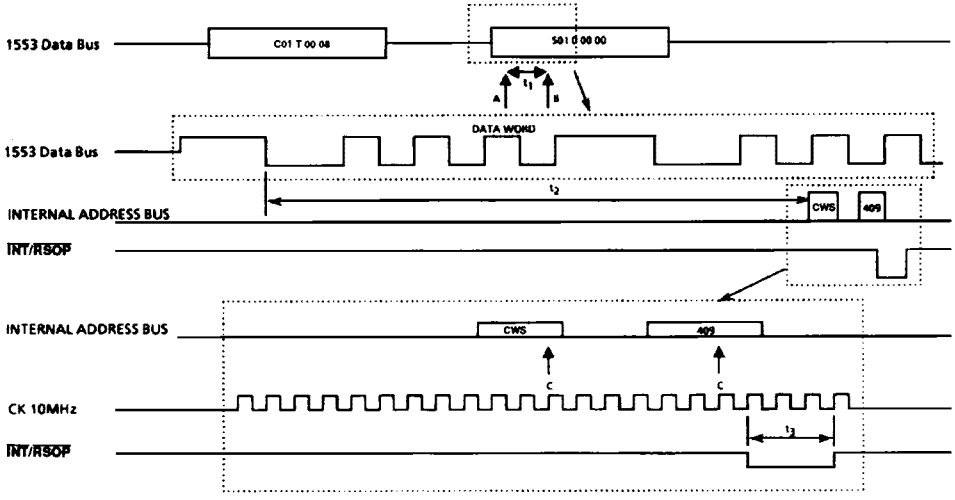


Figure 9: Synchronise without Data Word Mode Command



Key:
A - CW11-0 updated
B -1553B Status Latch loaded
C - Processor RAM LHS written to
CWS - Command Word Stack Address

t1 - 2.5µs max
t2 - 5.5µs typical
t3 - 300ns typical

Note: All address values in hex

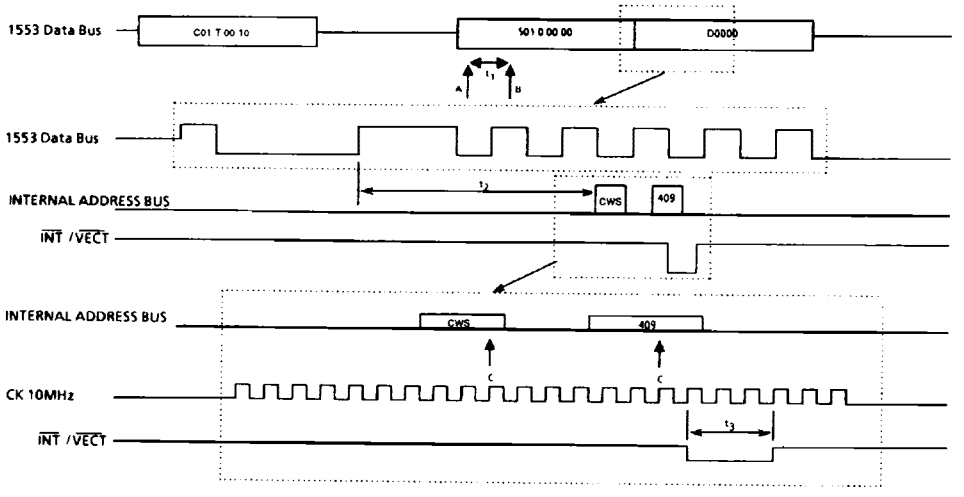
Figure 10: Reset Remote Terminal Mode Command

14. MODE COMMANDS (TX DATA)

Upon reception of a valid transmit mode command with an associated Data Word, the device will :-

1. Load the Command Word Latches with the received Command Word.
2. Modify the 1553B Status Word using the SMWd and the 6 hard wired lines, then transmit its 1553B Status Word followed contiguously by the contents of the RAM location indicated by the mode code field of the Command Word.
3. Write the Command Word into the next Command Word Stack location and increment the CWSP.
4. Take the $\overline{INT}$ line active low if the relevant HCWd bit is set.
5 In the case of a Transmit Vector Word mode command, also pulse the $\overline{VECT}$ line active low.
6. Update the HIWd, 1553SWd, BITWd and 1553CWd "Processor RAM" locations.

A typical Transmit Vector Word mode command sequence is shown in Figure 11.



Key:
A - CW11-0 updated
B -1553B Status Latch loaded
C - Processor RAM LHS written to
CWS - Command Word Stack Address

t1 - 2.5µs max
t2 - 5.5µs typical
t3 - 300ns typical

Note: All address values in hex

Figure 11: Transmit Vector Word Mode Command

15. ILLEGAL COMMANDS

The MCT83100 implements the illegal command option of 1553B and sets the message error bit in the Status Word as appropriate in response to illegal mode commands. The mode commands that the MCT83100 deems legal are listed in Table 19. The host CPU is given the option of illegalising any broadcast-T/R-subaddress-word count combination by driving $\overline{ME}$ input low within 2.5µs of the CW11-0 output pins being updated. It is also possible to make all of the reserved mode commands legal by setting bit 3 of the SMWd low, and any of these may then be illegalised using the $\overline{ME}$ input.

Note: The $\overline{ME}$ input is strobed 2.5µs after the Command Word outputs change.

Label	Parameter	min	max	unit
t	CW11-0 Valid to $\overline{ME}$	-	2.5	µs

Table 18: Message Error Timing

16. BROADCAST COMMANDS

Upon reception of a valid Broadcast Command the device will load any associated Data Words into the Broadcast Receive Data Buffer indicated by the subaddress value. By setting bits 8 & 9 of the HIWd to zero the device can be prevented from acting upon broadcast commands - should a broadcast command be received it will be completely ignored.

Transmit/ Receive Bit	Mode Code	Function	Associated Data Word	Broadcast Command Allowed
1	00000	Dynamic Bus Control	no	no
1	00001	Synchronise	no	yes
1	00010	Transmit Status Word	no	no
1	00011	Initiate Self Test	no	yes
1	00100	Transmitter Shutdown	no	yes
1	00101	Override Transmitter Shutdown	no	yes
1	00110	Inhibit Terminal Flag Bit	no	yes
1	00111	Override Inhibit Terminal Flag Bit	no	yes
1	01000	Reset Remote Terminal	no	yes
1	10000	Transmit Vector Word	yes	no
0	10001	Synchronise	yes	yes
1	10010	Transmit Last Command	yes	no
1	10011	Transmit BIT Word	yes	no
0	10100	Selected Transmitter Shutdown	yes	yes
0	10101	Override Selected Transmitter Shutdown	yes	yes

Table 19: Legal Mode Commands

17. RESPONSE TIME

The response time of the MCT83100 when measured from the mid-point of the parity bit to the mid-point of the sync bit is 10.5 ±0.5µs.

Label	Parameter	Typ	Max	Unit
t_{INT}	$\overline{INT}$ Pulse Width with $\overline{INTACK}$ Low	300	385	ns
t_{SYNC}	$\overline{SYNC}$ Pulse Width	300	360	ns
t_{VECT}	$\overline{VECT}$ Pulse Width	300	360	ns
t_{RSOP}	$\overline{RSOP}$ Pulse Width	300	360	ns
t_{ILH}	$\overline{INTACK}$ falling edge to $\overline{INT}$ rising edge	-	30	ns

Table 20: Interrupt Timing

18. COMMAND WORD BITS 11-0

The twelve hard wired Command Word lines are updated by the device 60ns (max) after the rising edge of the 10MHz clock signal. The least significant eleven bits (CW10-0) follow the Command Word bits exactly. Bit 11 will be high for broadcast commands and low for non-broadcast commands.

19. RAM ACCESS

Whenever a host CPU attempts to access the same location as the on-board gate array the $\overline{RAMBUSY}$ signal will go active. The host CPU must not access the on-board RAM whilst $\overline{RAMBUSY}$ signal is active. The gate array accesses to the LHS of the "Processor RAM" are nominally 300ns for all 'receive' locations ie 000-3FF and 800-BFF (hex) and 400ns for all 'transmit' locations ie 400-7FF (hex). Hence the absolute maximum time that $\overline{RAMBUSY}$ will be active is 475 ns - ie gate array access (400ns) plus $\overline{RAMBUSY}$ delay (70ns) + 5ns to allow for clock skew.

Note: In the majority of system designs it is unlikely that both the gate array and the host CPU will attempt to access the same location at exactly the same time.

20. RECEIVE DATA BUFFER

In order to prevent reception of incomplete 1553 messages, a host CPU must write a RACWd containing the relevant subaddress value into location 405 (hex) before reading the Receive Data Buffer contents. The Data Buffer must be read in ascending numerical order starting at the first location of the Receive Data Buffer.

The on-board gate array inspects its internal copy of the RACWd contents immediately prior to initiating the transfer of a received message between the "1553 RAM" and the "Processor RAM". This transfer is carried out in ascending numerical order starting at the first location in the Receive Data Buffer. If the internal RACWd contains the same subaddress value as that contained in the received Command Word, then the transfer will be delayed until the RACWd contents are changed. If the subaddress values do not match, the transfer will go ahead.

Figures 13 shows when the data transfers occur after reception of a seven word receive command. Three situations are highlighted:-

a) During a 'normal' sequence when the host CPU accesses the Receive Data Buffer after the gate array has completed loading it.

b) If the RACWd is written to by the host CPU immediately after the internal RACWd has been interrogated by the gate array then the host CPU is held off from reading the former contents of the "Processor RAM" by the $\overline{RAMBUSY}$ signal.

c) When the RACWd is written to by the host CPU immediately before the gate array has interrogated it. In this situation the gate array 'C' transfer, (see Figure 12), is held up until the host CPU alters the contents of the RACWd .

The gate array accesses will take 300ns each therefore the maximum delay incurred on the host CPU attempting to read a Receive Data Buffer will be 475ns minus the time difference between it writing the RACWd and then attempting to read the data location.

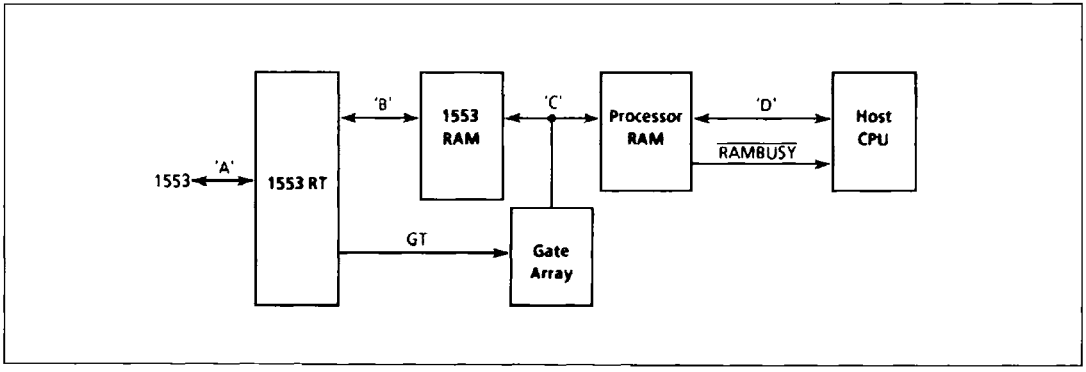


Figure 12: MCT83100 Data Flow Diagram (read in conjunction with Figures 13 and 14)

21. RECEIVE DATA TRANSFERS

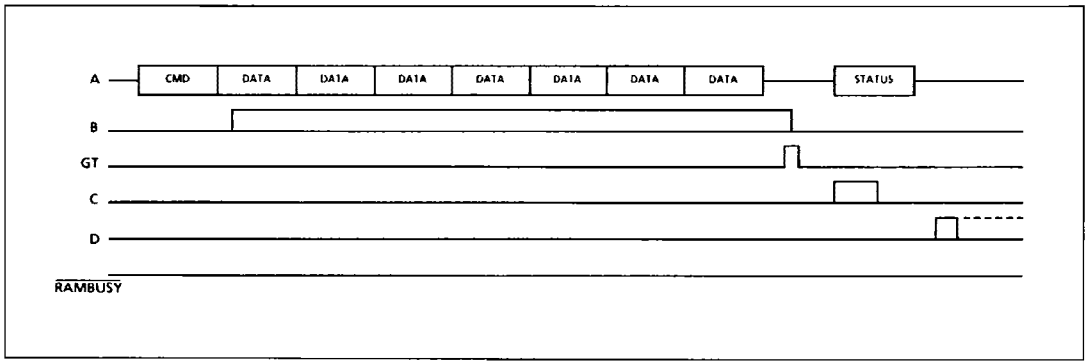


Figure 13a: Normal Sequence

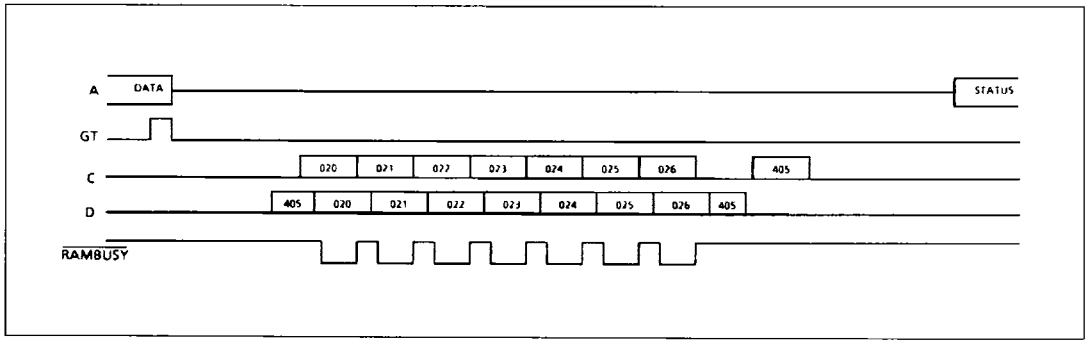


Figure 13b: RACWd Updated After Being Interrogated by The Gate Array

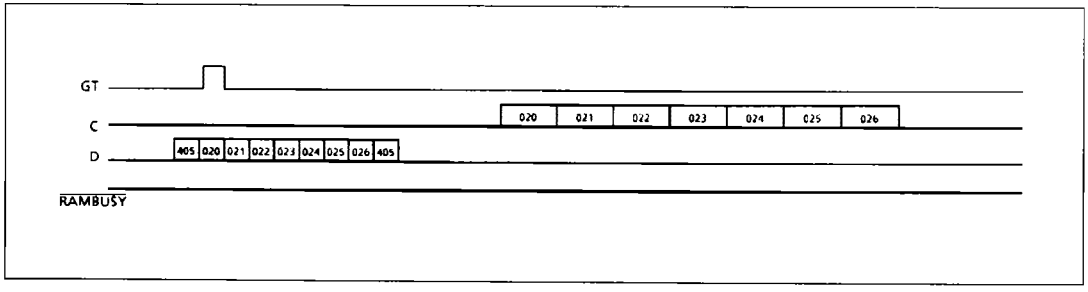


Figure 13c: RACWd Updated Before Being Interrogated By The Gate Array

Note: A,B,C and D refer to the data transfers indicated in Figure 12. Host CPU memory access time is shown considerably less than 300ns for diagramatic purposes. Normally processor access would be slower and less $\overline{\text{RAMBUSY}}$ pulses would be generated.

22. TRANSMIT DATA BUFFER

In order to prevent transmission of incomplete 1553 messages, the host CPU must ensure that neither TCWd contains the appropriate subaddress value, before updating a Transmit Data Buffer. Once the Data Buffer has been updated, the host CPU must then interrogate the TCWd locations in order to ascertain which is zero, then write the appropriate subaddress value and word count into the TCWd containing zero. When the gate array detects the TCWd being updated, it will transfer the indicated number of Data Words to the indicated buffer in the "1553 RAM". This transfer may be delayed if that buffer is being accessed in order to service a Transmit Command. Upon completion of the data transfer the device will clear the relevant TCWd. Figure 8 details the transmit data transfers.

The host CPU may encounter two delays in updating a Transmit Data Buffer.

(i) If the host CPU instructs the gate array to transfer a 32 word message immediately after reception of a transmit command containing the relevant subaddress value, then the gate array will not clear the TCWd for 736µs assuming a second 32 word transfer is requested using the other TCWd.

(ii) If the gate array is instructed to transfer two 32 word messages simultaneously then both TCWds will be non zero for a maximum of 82µs, assuming simultaneous reception of a 32 word receive command. (The internal transfers interleave.)

Figure 14b shows how an internal transmit data transfer is delayed by the transfer being initiated just after reception of a transmit command to that subaddress.

Figure 14c shows that an internal transmit data transfer, once started, will procede in parallel with the much slower 1553 data transfer.

Note: A 32 word Transmit Data Buffer update will take typically 40µs.

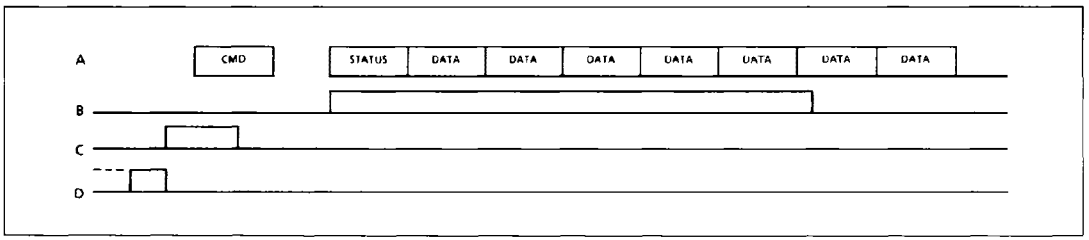


Figure 14a: Normal Sequence

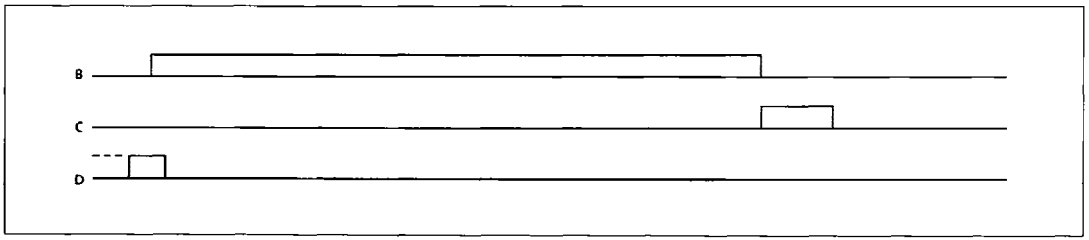


Figure 14b: Transmit Command Received Before TCWd is Updated

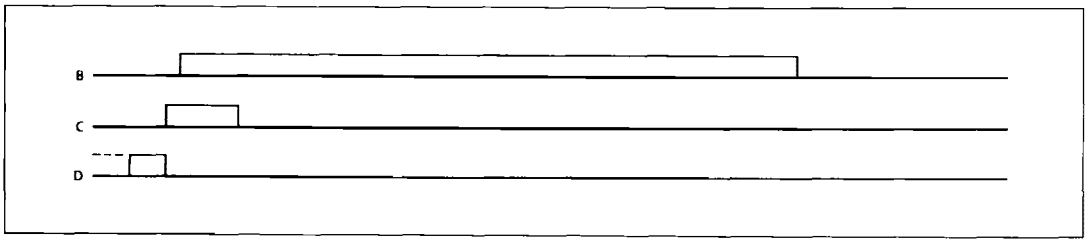


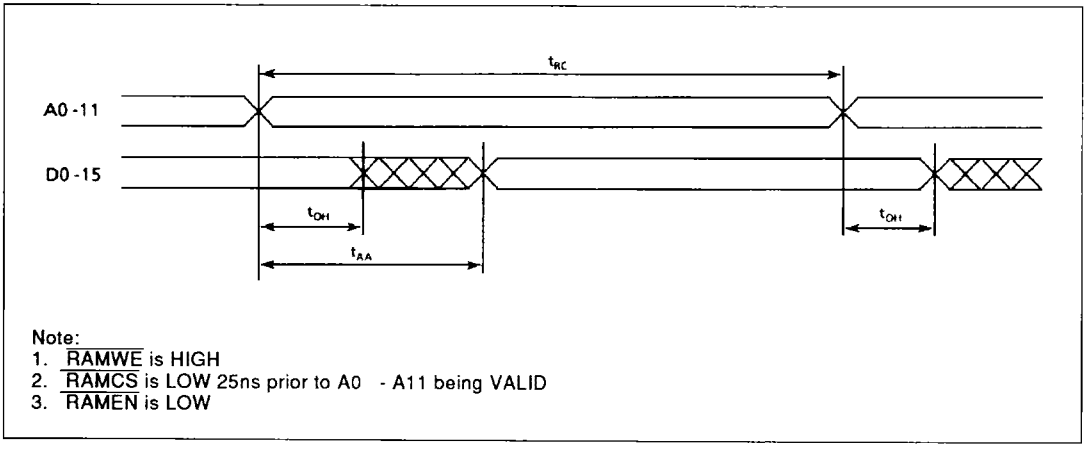
Figure 14c: Transmit Command Received After TCWd is Updated

Note: A,B,C and D refer to the data transfers indicated in Figure 12.

23. MEMORY ACCESS SIGNAL TIMINGS

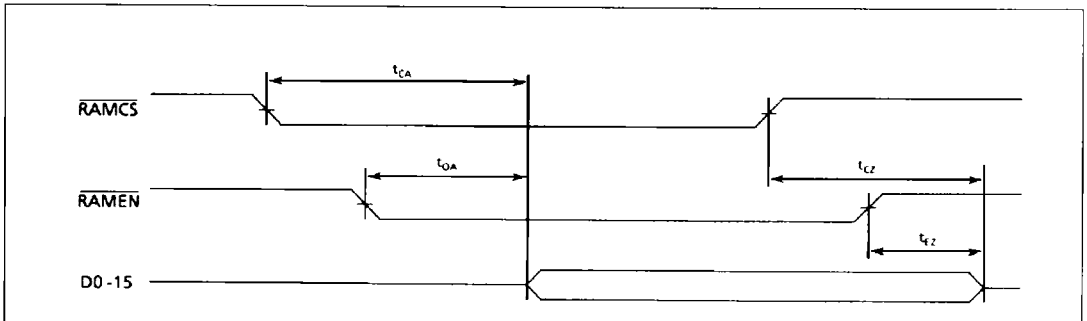
Label	Parameter	Min.	Max.	Units
t_{RC}	Read Cycle Time	90	2400	ns
t_{AA}	Address Access Time	-	90	ns
t_{CA}	$\overline{\text{RAMCS}}$ Access Time	-	115	ns
t_{OA}	$\overline{\text{RAMEN}}$ Access Time	-	40	ns
t_{OH}	Output hold from address change	10	-	ns
t_{EZ}	$\overline{\text{RAMEN}}$ rising edge to Data in High Z	-	40	ns
t_{CZ}	$\overline{\text{RAMCS}}$ rising edge to Data in High Z	-	65	ns

Table 21: Read Cycle - Figures 15 and 16 apply



Note:
1. $\overline{\text{RAMWE}}$ is HIGH
2. $\overline{\text{RAMCS}}$ is LOW 25ns prior to A0 - A11 being VALID
3. $\overline{\text{RAMEN}}$ is LOW

Figure 15: Timing Waveform of Read Cycle 1

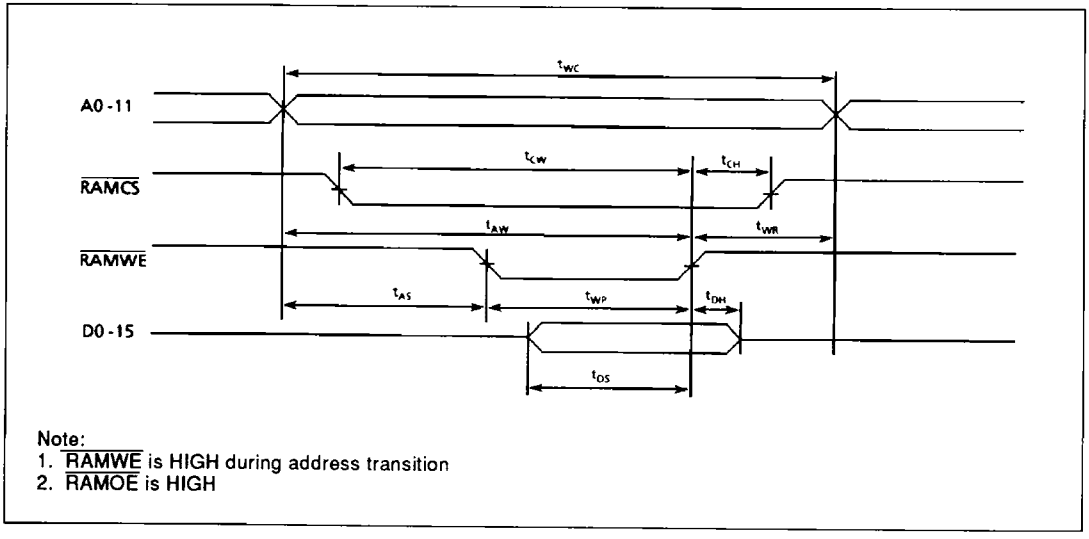


Note:
1. $\overline{\text{RAMWE}}$ is HIGH
2. A0 - A11 VALID prior to $\overline{\text{RAMCS}}$ going LOW

Figure 16: Timing Waveform of Read Cycle 2

Label	Parameter	Min	Max	Unit
t_{WC}	Write Cycle Time	115	2400	ns
t_{CW}	$\overline{RAMCS}$ Active to $\overline{RAMWE}$ rising time	110	-	ns
t_{AW}	Address Valid to $\overline{RAMWE}$ rising edge	85	-	ns
t_{AS}	Address Set Up Time	0	-	ns
t_{WP}	$\overline{RAMWE}$ pulse Width	55	-	ns
t_{WR}	Address Hold Time after $\overline{RAMWE}$ rising edge	0	-	ns
t_{CH}	$\overline{RAMCS}$ hold time after $\overline{RAMWE}$ rising edge	0	-	ns
t_{DS}	Data Set Up time	30	-	ns
t_{DH}	Data Hold Time	0	-	ns

Table 22: Write Cycle - Figure 17 Applies



Note:
1. $\overline{RAMWE}$ is HIGH during address transition
2. $\overline{RAMOE}$ is HIGH

Figure 17: Timing Waveform of Write Cycle

Label	Parameter	Min	Max	Unit
t_{CBL}	$\overline{RAMCS}$ to $\overline{RAMBUSY}$ active	-	70	ns
t_{CBH}	$\overline{RAMCS}$ to $\overline{RAMBUSY}$ inactive	-	70	ns
t_{ABL}	Address Valid to $\overline{RAMBUSY}$ active	-	55	ns
t_{ABH}	Address Valid to $\overline{RAMBUSY}$ inactive	-	45	ns
t_{ICS}	Internal $\overline{RAMCS}$ Pulse	-	400	ns

Table 23: $\overline{RAMBUSY}$ Timing - Figures 18 and 19 Apply

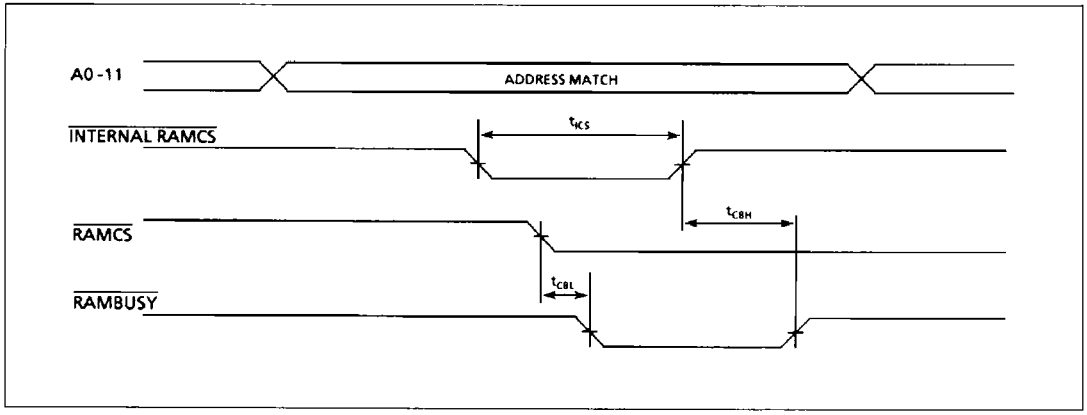


Figure 18: Timing Waveform of Contention Cycle - CS Arbitration

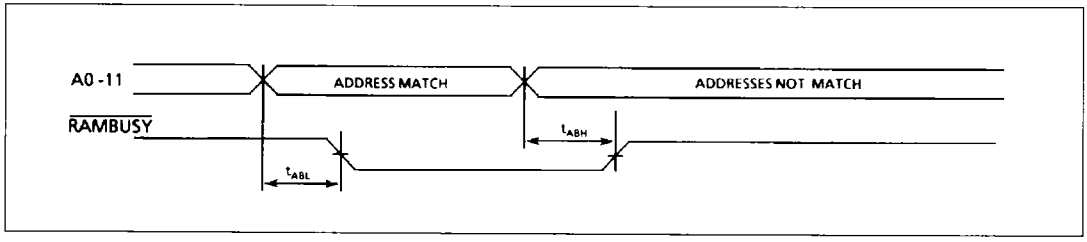


Figure 19: Timing Waveform of Contention Cycle - Address Arbitration

24. TYPICAL INTERFACE CONNECTIONS

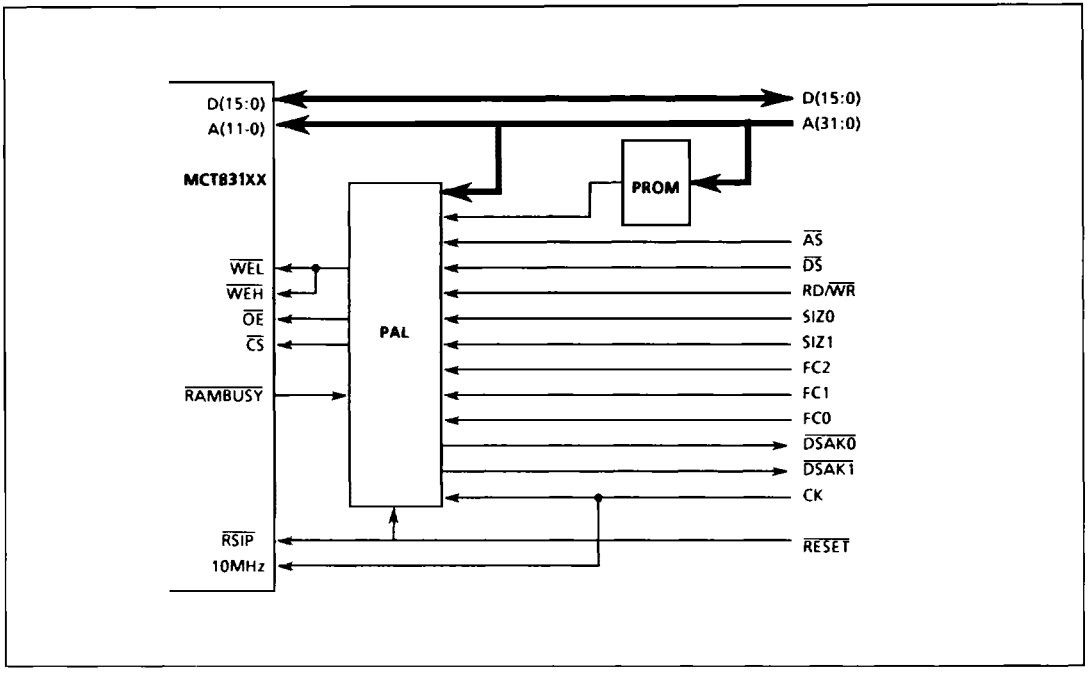


Figure 20: Typical 16-Bit Interface

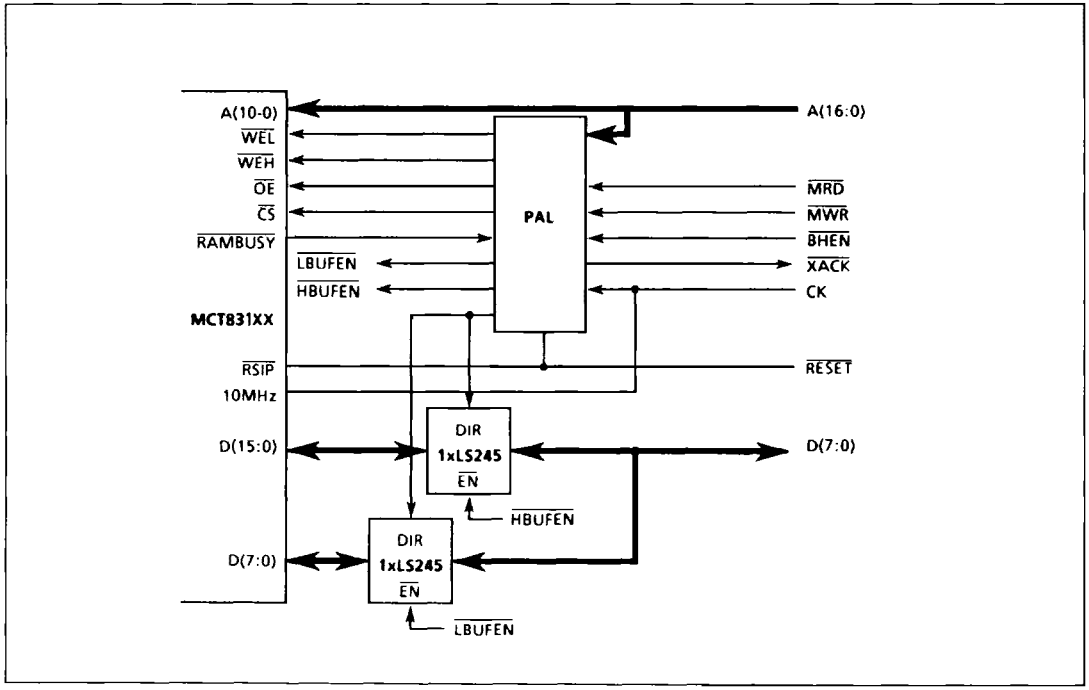


Figure 21: Typical 8-Bit Interface

25. PACKAGE OUTLINES

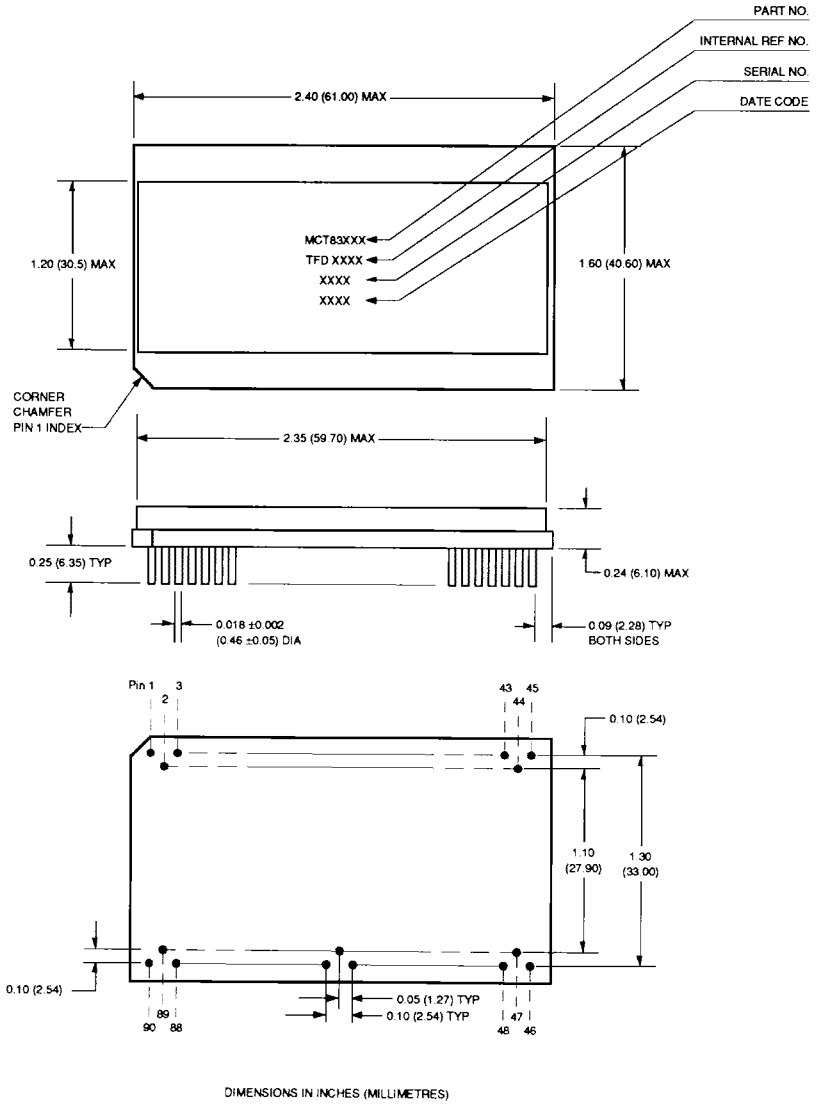


Figure 22: Package Outline - Plug-In

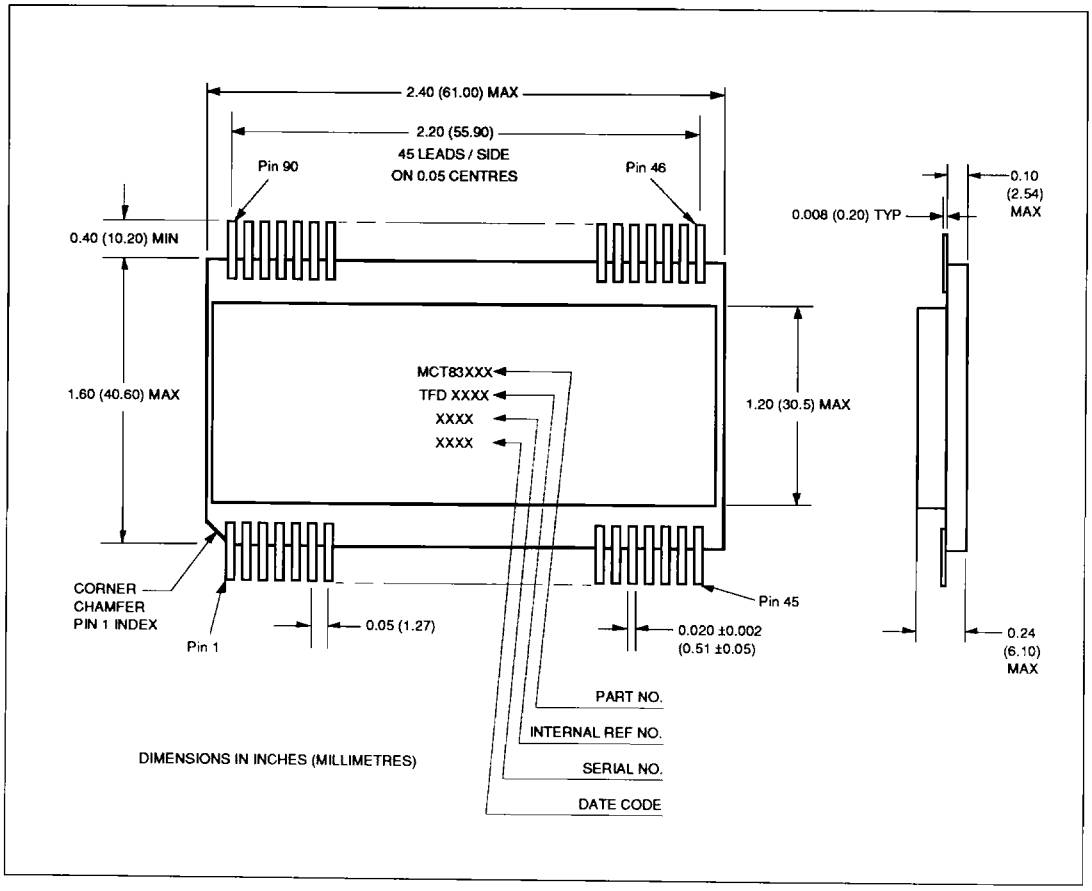


Figure 23: Package Outline - Flat-Pack

APPENDIX A - MCT83910/1/2 OPERATION

The MCT83910 version of the MCT83100 series of hybrids has been designed to provide the STANAG 3838 Remote Terminal port of a STANAG 3910/STANAG 3838 interface.

A typical interface is shown in Figure 24.

The MCT83910 is similar to the MCT83102 but differs in the following areas:

1. The 'hard' Hybrid Initialise Word is no longer buffered within the device and if required must be buffered externally. A $\overline{\text{HIWDEN}}$ output is provided to enable the contents of such a buffer onto the 'HD' bus (see below).

2. The 12 bit latched Command Word is no longer available on dedicated pins but can be latched off the 'HD' bus (see below). A CWLD output is provided to latch the Command Word.

3. The 16 bit data bus between the MIL-STD-1553B interface device and the left hand side of the "1553 RAM" is made available to the STANAG 3910 interface along with 6 control lines. This 16 bit 'HD' bus and its associated control lines (see Tables 26) are provided for the transfer of high speed action and status words.

All commands/status/data transfers over the 'HD' bus are preceded by the transfer of a control word. This control word is available on both edges of the $\overline{\text{CLE}}$ output and provides a description of the following word. Details of the bit allocation of the control word are given in Table 25. The control words for both receive and transmit commands along with an indication of the timing relationships between the STANAG 3910 interface control signals is given in Figures 25 and 26.

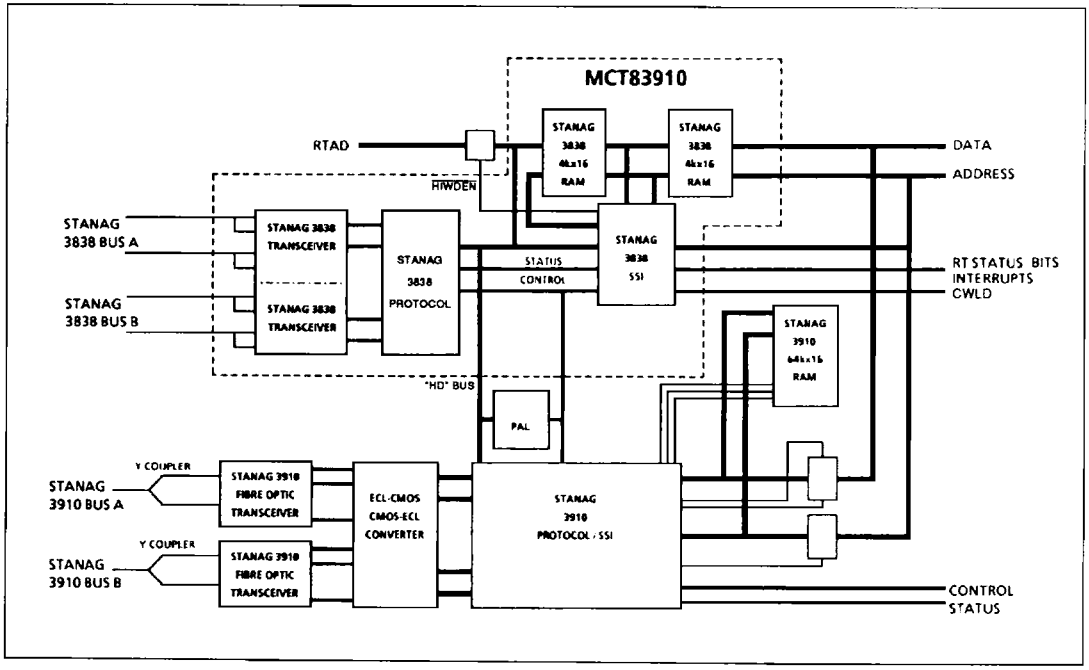


Figure 24: STANAG 3910 / STANAG 3838 Interface Example

MCT83910/1/2 PIN-OUT

1	BUS1(+)	24	*HD14*	47	RAMBUSY	70	*GT*
2	BUS1(-)	25	*HIWDEN*	48	D15	71	*WE*
3	VEE(1)	26	*HD6*	49	D14	72	*HD3*
4	VDD(1)	27	*HD5*	50	D13	73	*HD2*
5	0V	28	*HD4*	51	D 12	74	*HD1*
6	VCC	29	RAMWEH	52	D11	75	*HD0*
7	TP1	30	RAMWEL	53	D10	76	ME
8	TP2	31	RAMOE	54	D9	77	SR
9	TXINH1	32	RAMCS	55	D8	78	BUSY
10	H/S	33	A11	56	D7	79	SSF
11	10MHZ	34	A10	57	D6	80	*CSIN*
12	RSIP	35	A9	58	D5	81	TF
13	RSOP	36	A8	59	D4	82	TXINH0
14	VECT	37	A7	60	D3	83	TP4
15	SYNC	38	A6	61	D2	84	TP3
16	INT	39	A5	62	D1	85	VCC
17	INTACK	40	A4	63	D0	86	0V
18	*HD12*	41	A3	64	*RD*	87	VDD(0)
19	*HD8*	42	A2	65	*CLE*	88	VEE(0)
20	*HD10*	43	A1	66	*HD9*	89	BUS0(-)
21	*HD15*	44	A0	67	*CSOUT*	90	BUS0(+)
22	*HD11*	45	0V	68	*HD7*		
23	*HD13*	46	CASE	69	*CWLD*		

Notes:
1. Refer to Table 2 for description of power supply options.
2. For the 24 signals in italics refer to Tables 26 for description. Remainder of pins are described in Table 2.

Table 24: MCT83910 Series Pin Out

Bit	Name	Description
15	BCST	Command word had the broadcast address when high
14	RESMODE	Reserved mode code detected when high
13	SYNCVEC	Synchronise/Transmit Vector Word being transferred when high
12	CMDSTAT	Command/Status Word being transferred when high
11	NMD	Non Mode Data: 1=normal data transfers. 0=mode data transfers
10	TR	During data transfers the SA field contains the subaddress of the command word and the CWC field contains the Current word count. During command word, status modifier word and mode data transfers, the SA and CWC field are as described below:
9	SA4	
8	SA3	
7	SA2	
6	SA1	
5	SA0	
4	CWC4	
3	CWC3	
2	CWC2	
1	CWC1	
0	CWC0	Thus, command words, data words and data words associated with mode commands can be directly located in subsystem memory.

WE	RD	TR	SA	CWC	
0	1	0	00	00	Command word (Receive)
0	1	1	00	00	Command word (Transmit)
1	1	0	00	00	Status modifier word read (Receive)
0	1	0	01-1E	0-1F	Received data
1	0	1	01-1E	0-1F	Data to be transmitted
0	1	0	1F	0-1F	Mode data (to S/System)
1	0	1	1F	0-1F	Mode data (from S/System)

Table 25: MIL-STD-1553B Interface Control Word

Pin	Name	Dir	Logic	Description
21	HD15	I/O	C4	16 bit internal tri-state data bus ('HD' BUS) which allows subsystem to detect STANAG 3910 action words. The Hybrid Initialise Word is loaded by the device on power up via this data bus. The 1553B Command Word is available on this bus on both edges of CWLD.
24	HD14			
23	HD13			
18	HD12			
22	HD11			
20	HD10			
66	HD9			
19	HD8			
68	HD7			
26	HD6			
27	HD5			
28	HD4			
72	HD3			
73	HD2			
74	HD1			
75	HD0			

Table 26a: MCT83910 Pin Descriptions Internal Data Bus

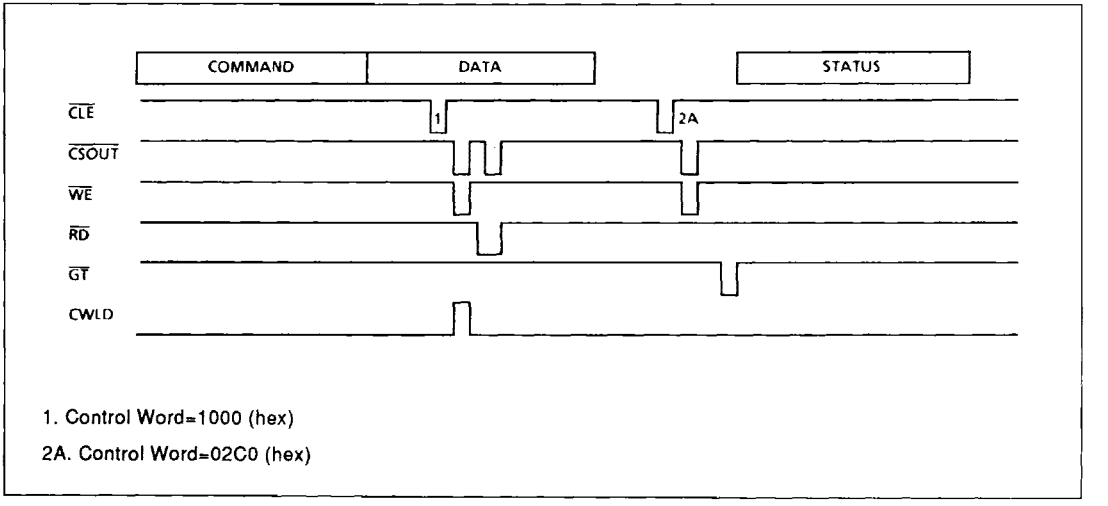
Pin	Name	Dir	Logic	Description
80	$\overline{CSIN}$	I/P	C4	Active low chip select input to the LHS of the 1553B dual port RAM.
67	$\overline{CSOUT}$	O/P		Active low internal chip select output which under normal operation should be connected to pin 80. Failure to make this connection allows the subsystem to connect external devices to the internal data bus.
25	$\overline{HIWDEN}$	O/P		Active low pulse which can be used to enable Hybrid Initialise Word onto the internal data bus.
69	CWLD	O/P		Active high pulse which can be used to load the 1553B Command Word off the internal data bus.
70	$\overline{GT}$	O/P		Active low pulse which indicates a valid 1553B transaction.
71	$\overline{WE}$	O/P		Active low write pulse to LHS of the 1553B dual port RAM
64	$\overline{RD}$	O/P		Active low read pulse to LHS of the 1553B dual port RAM
65	$\overline{CLE}$	O/P		Active low pulse which can be used to load internal control words off the internal data bus.

Table 26b: MCT83910 Pin Descriptions Internal Data Bus Control

Label	Description	Min	Typ	Max	Unit
VOH	Output High Level Voltage	2.5	-	-	V
VOL	Output Low Level Voltage	-	-	0.4	V
IOH	Output High Level Current	-	-	-0.8	mA
IOL	Output Low Level Current	-	-	2.0	mA
VIH	Input High Level Voltage	2.0	-	VCC	V
VIL	Input Low Level Voltage	0	-	0.7	V
IIH	Input High Level Current	-	-	10	µA
IIL	Input Low Level Current	-	-	-0.4	mA

Table 27: MCT83910 Electrical Characteristics - CMOS Input/Output - Type C4

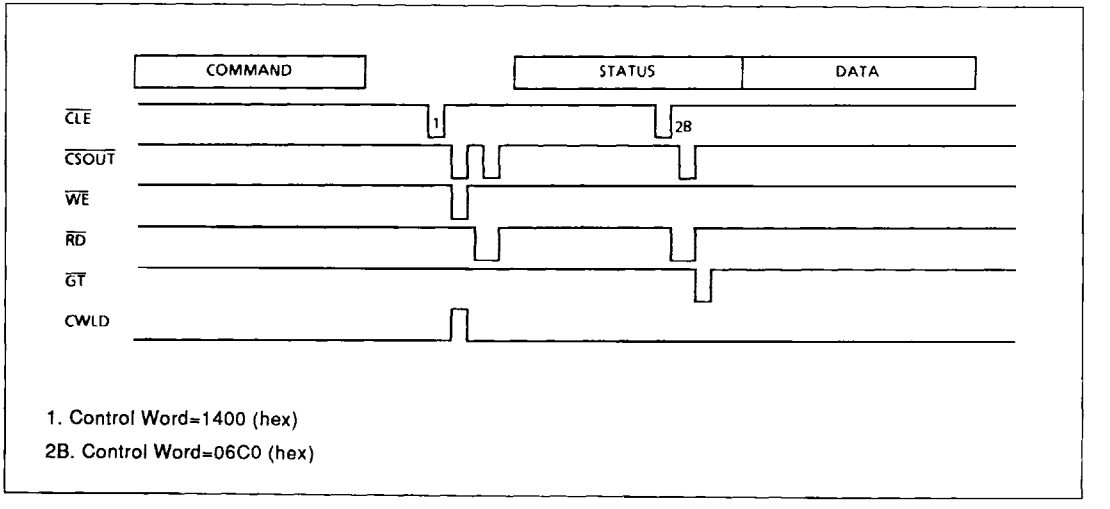
STANAG 3910 Interface Timing Diagrams



1. Control Word=1000 (hex)

2A. Control Word=02C0 (hex)

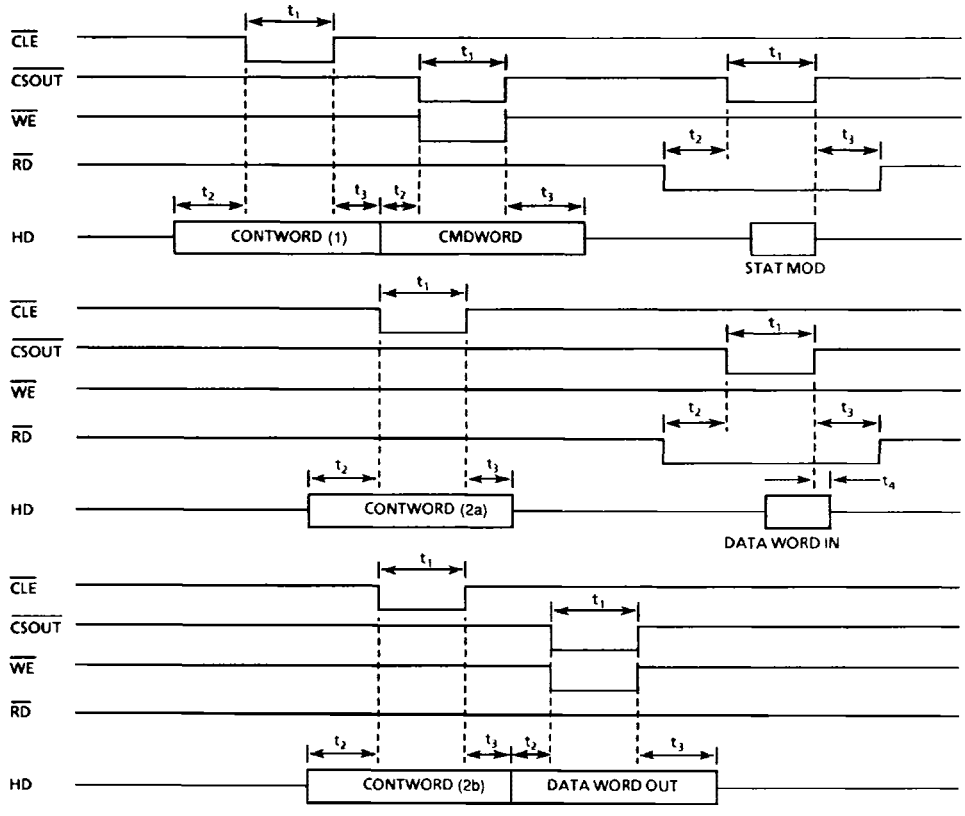
Figure 25a: Receive Command - 1 Word Subaddress 22



1. Control Word=1400 (hex)

2B. Control Word=06C0 (hex)

Figure 25b: Transmit Command - 1 Word Subaddress 22



Label	Timed from	Timed to	Min	Typ	Max	Unit
t1	Strobe↓	Strobe↑	-	1.0	-	µs
t2	Data Valid	Strobe↓	-	0.5	-	µs
t3	Strobe↑	Data Valid	-	0.5	-	µs
t4	Strobe↑	Data Valid	0	-	-	µs

Notes:
1. 'strobe' may be any of $\overline{CLE}$, $\overline{CSOUT}$ or $\overline{WE}$, whichever is relevent for the transfer.
2. '↑' represents a low to high transition.
3. '↓' represents a high to low transition.

Figure 26: STANAG 3910 Interface Timing Details (refer to Figures 25a and 25b for basic transfers)